



DESY - FEA P.Vetrov Tel: +49 / 40-8998 – 2538 petr.vetrov@desy.de	Hardware Design Description (HDD) of the DESY Double Advanced Mezzanine Card	
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Hardware Design Description (HDD) of the **Double Advanced Mezzanine Card, Version 00, DESY**

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1 Introduction

The purpose of this manual is to describe the functionality and contents of the first variant of Double AMC module, which was designed by FEA with input by MCS4, so called DESY Double AMC or DAMC2. This document includes instructions for operating the board and descriptions of the hardware features. For reference design documentation, see the PDF file included with the project files of the design.


1.1 Identification

The European XFEL will provide X-Rays with unique parameters to many research fields like material science, chemistry, biology, physics and others. Main components of the XFEL accelerator control system will be developed according to the standards xTCA, ATCA, AMC [1] and μ TCA. Advanced Mezzanine Card (AMC) is based on serial interfaces and supports different transport layers such as PCI Express, Gigabit Ethernet, 10 Gigabit Ethernet, Serial ATA and others. Its scalable modular architecture enables a number of applications, ranging from intelligent IO controllers for mixed signals up to high speed processing units.

The DESY Advanced Mezzanine Card (DAMC) is designed as a compact and economical solution aimed at several applications for control and Data Acquisition systems at the XFEL accelerator. The first generation of the DAMC is a single size board based on a Virtex-5 FPGA, equipped with DDR2 memory. It has a custom made interface to an I/O mezzanine card, supports PCI Express as well as 1G Ethernet and implements the Intelligent Platform Management Interface (IPMI).

Based on the experience obtained during operation at the FLASH accelerator at DESY a new version of the AMC board was developed – DAMC2, which will improve the versatility and overcome the limitations of the first generation by additional features. It is designed as a double size board with the possible extension by a rear transition Module (μ RTM) via a two high speed differential connectors. This approach increases the available PCB space by nearly a factor of four and allows to create the modular systems. The analog or digital rear transition Input/Output as well as signal conditioning measures can be separated from the FPGA based front module. Additionally the board can be extended by a VITA 57.1 compliant FPGA Mezzanine Card (FMC). Four multi-gigabit optical links are available at the front panel for fast external communication. The DDR2 memory size has been increased to 1 Gbit and in addition to the standard interfaces, the special MLVDS interfaces to the backplane and a more flexible clock distribution scheme has been added.

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1.2 DAMC2-00 Description

The DESYS Double Advanced Mezzanine Card – DAMC2-00 is a FPGA-based (VIRTEX-5), double width, normal size board, which can be used in MicroTCA (uTCA) or xTCA crates, Figure 1 and 2.



Figure 1 Top view of DAMC2-00

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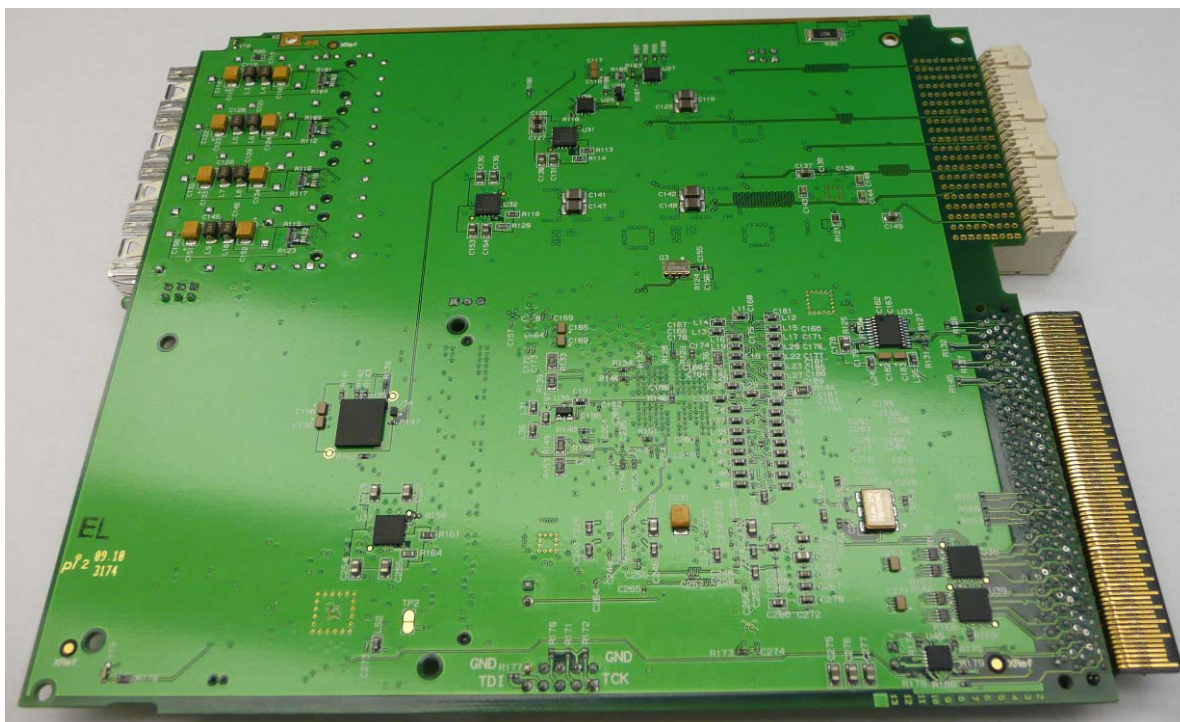



Figure 2 Bottom view of DAMC2-00

It was designed to test the xTCA standard of electronics, which is considered to be used in xFEL control system.

1.3 Board features

In accordance with specification of DAMC2-00 and system requirements, the board includes:

1. FPGA - VIRTEX-5, XC5VLX50T-1FF1136C
2. High-speed (up to 3.75 Gb/s) Rocket I/O interfaces with different protocols:
 - Three Lanes supplied on the three SFP connectors, for external High-speed optical interfaces
 - One Lane can be supplied to FMC board or to the fourth SFP connector
 - The four Lanes are provided high-speed interfaces to neighbours board in xTCA crate – point-to-point connection
 - The four Lanes are applied to PCI Express first generation add-in board interface (Four lanes @2.5 Gbps) – card edge connector J1
3. The IPMI compliant Module Management Controller (MMC) with temperature monitoring, payload power monitoring and hot-swap support – Atmega128L
4. The eight differential pairs MLVDS bus, which can be used for distribution triggers,

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interlocks and clocks signals via Backplane of xTCA

5. The Virtex-5 system monitor

6. Memory:

- The 1Gb DDR2 SDRAM is a high-speed CMOS, dynamic random-access memory
- The 32Mbit Platform Flash In-System Programmable Configuration PROM (ISP PROM)
- Two-wire Serial EEPROM (8Kbit) with e-Keying info, which is connected to the MMC.

7. Remote/Local Temperature Sensor with SMBus Serial Interface, which is connected to the MMC.

8. Communication: Intelligent Platform Management Interface – IPMB_L, supporting by MMC

9. The Hot Swap Controller (TPS2458RHBT), which provided Hot Swap regime for microRTM boards

10. Power:

- Management power voltage for MMC is +3V3, is obtained from the AMC slot or an external connector (Auxiliary power connector)
- Three on-board 10A, DC/DC step down power supply (LTM4600EV) for generation main powers of DAMC2-00: +3V3, +2V5 and 1V. The +12V payload supply is derived from the xTCA slot or from on-board (Auxiliary) power connector
- Four on-board 4A low-dropout linear regulators (MAX8556ETE) operate for powering of GTP transceivers and ispPROM, and produce +1V2, +1V0, +1V2 and +1V8 power
- One low drift, micro power, low-dropout precision voltage reference (REF3235AIDBVT), for powering Virtex-5 system monitor
- DDR-2 Termination Regulator (TPS51200DRCT) for termination of DDR-2 memory chip


11. I/O connectors:

- Four SFP connectors for High Speed Optical interfaces on Front panel
- Two Z-PACK (J30 and J31) high speed connectors, for interfaces to uRTM boards

12. Configuration:

- JTAG daisy chain Programming/Configuration of XILINX and ISP PROM via J2 connector or from the edge connector of AMC
- Implementation in the XILINX the JTAG Player for programming of the ISP PROM

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- JTAG daisy chain Programming/Configuration of XILINX and ISP PROM from the MMC
- JTAG Programming/Configuration of the MMC via J11 connector.

13. Auxiliary power connector – J3
14. Hot Swap switch and blue LED placed on front panel
15. Failure LED – Red, and User Define Led – Green placed on front panel
16. User defines LEDs on front panel: Red, Green and Yellow, and on the board
17. VIRTEX-5 reset button

2 Functional Description

The first generation of the DESYS AMC board (DAMC1) (Fig. 1), was designed as a demonstrator board to study and test the potential of the new μ TCA standard, for control applications with analogue I/O. μ TCA was originally developed for the Telecommunication industry as a standard for digital applications. The DAMC1 board is a single, midsize, FPGA-based board, equipped with 256 Mbit of DDR2 memory. It has a custom made interface to an I/O Mezzanine Card, supports 4 Lanes of PCIe to the Backplane as well as 1G Ethernet and implements the Intelligent Platform Management Interface (IPMI).

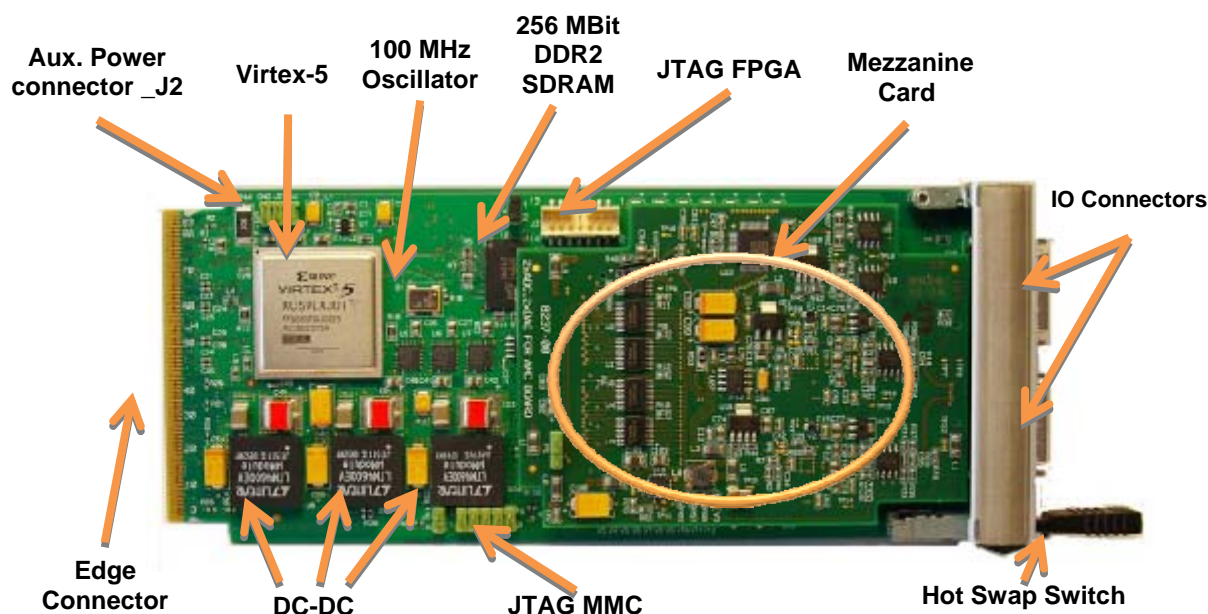


Figure 3 DAMC1 module with mezzanine card in place

The DAMC1 board is a single, midsize, FPGA-based board, equipped with 256 Mbit of DDR2 memory. It has a custom made interface to an I/O Mezzanine Card, supports 4 Lanes of PCIe to the Backplane as well as 1G Ethernet and implements the Intelligent Platform Management

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Interface (IPMI). Currently the DAMC1 boards are used in various fields in the control system of DESY's FLASH accelerator. Examples are Beam Position Monitoring, control applications for Toroid and Kicker-magnets as well as for the Machine-Protection-System (MPS). During the development and operation of the boards for the envisaged applications we found several limitations. Using the small form factor of a single size AMC module leaves only relatively small development space additional to the necessary TCA related infrastructure. Implementing a nonstandard mezzanine interface can simplify the development of dedicated I/O modules but excludes possible standardized commercial board extensions. The lack of standardized external interfaces additionally to the backplane turned out to be a disadvantage for the envisaged applications at the XFEL control system. We also encountered problems finding PCB-vendors, which were able to produce a PCB with the AMC printed edge connector.

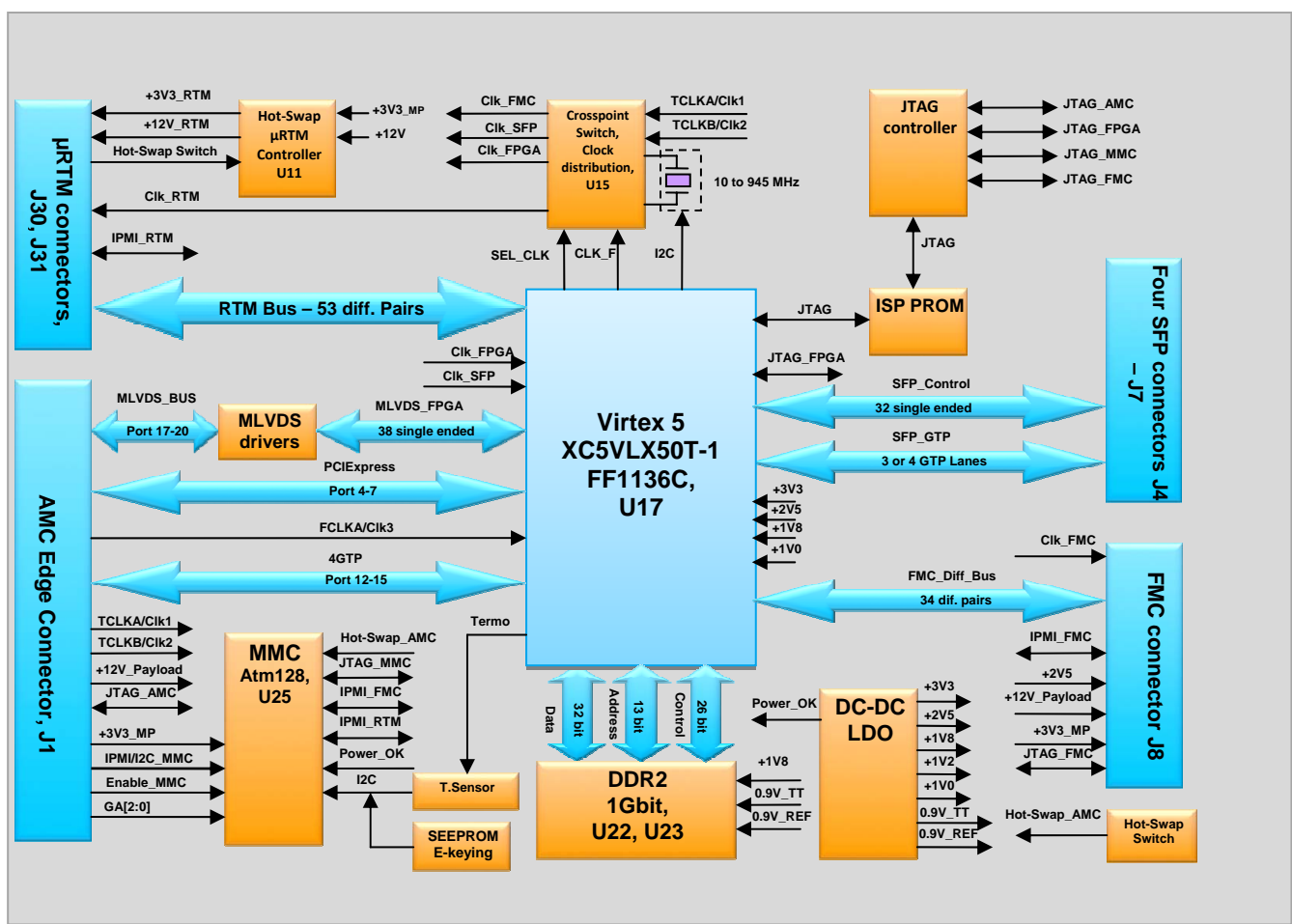



Figure 4 Block diagram of DAMC2-00

Based on the experience obtained during the operation at the FLASH accelerator at DESY and with input from future potential users a new set of requirements and extensions has been compiled. The new generation of the board, DAMC2-00 (Figure 4) improve the versatility and overcome the limitations of the first generation. The most obvious improvement is that the board is now developed according to the preliminary xTCA® for Physics specification by the PICMG

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consortium [10]. This extension to the μ TCA standard aims at applications for data acquisition and control systems for Physics instrumentation. Main ingredients are:


- a **bigger form factor** by restricting to double and mid or full size boards,
- a connector to a rear transition module (**μ RTM**)
- Plug in position for a VITA 57.1 compliant FPGA Mezzanine Card (**FMC**)
- Four optical links (**SFP**) at the front panel for external communication
- flexible **Clock distribution scheme**
- sophisticated **JTAG daisy chain**
- four Lane **PCIe interface (Backplane ports 4 -7)**
- the definition of a backplane, which now includes a LVDS bussed connections - **M-LVDS (Backplane ports 17 -20)**
- high speed point-to-point connections - **4 GTP, (Backplane ports 12 – 15))** between the modules in xTCA crate

The **μ RTM**, defined in the xTCA® for physics standard, has a comparable size to a double AMC module and is attached to the DAMC card via a high speed connector with 60 pairs, each with an additional ground pin. The new standard only defines a few signals for power (+12V and +3.3V) and board management and leaves up to 54 pairs for user defined purposes. This concept adds several advantages for the system designer. The development space is doubled and the rear module is decoupled from the front board and can be developed independently. Possible applications for μ RTMs range from simple signal adaptations and conditioning for I/O signals to complex designs with additional processing power. This approach simplifies the design of modular systems, where DAMC cards can be easily reused for different purposes.

Key benefits of **FMC implementation** [25] are:

- **Data throughput:** Individual signaling speeds up to 10 Gb/s are supported, with a potential overall bandwidth of 40 Gb/s between mezzanine and carrier card
- **Latency:** Elimination of protocol overhead removes latency and ensures deterministic data delivery
- **Design simplicity:** Expertise in protocol standards such as PCI, PCI Express®, or Serial RapidIO is not required
- **System overhead:** Simplifying the system design reduces power consumption, IP core costs, engineering time, and material costs
- **Design reuse:** Whether using a custom in-house board design or a commercial-off-the-shelf (COTS) mezzanine or carrier card, the FMC standard promotes the ability to retarget existing FPGA/carrier card designs to a new I/O. All that is required is swapping out the FMC module and slightly adjusting the FPGA design.

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Four optical links (SFP) are available at the front panel and allow realizing high-speed (~ 3Gbps) data transmission between DAMC2-00 and other parts of accelerator control system on long distance (~ 1 km) without exchange data with Host processor of xTCA crate. Different types of protocols can be used. The SFP links can be use for transmission Alarm signal to MPS.

Distributed control and data acquisition systems for accelerators depend on precise timing and need stable high quality clocks with low jitter. There is implemented a **Clock distribution scheme** for the DAMC2 with several sources and destinations and achieve a jitter in the range of a few picoseconds depending on the quality of the input clock. Different clock inputs can be routed simultaneously via a high precision cross point switch to the μ RTM, the FMC and to the FPGA. The following sources are implemented:

- The two high quality TCLKA and TCLKB clock lines from the μ TCA Backplane will typically distribute external signals like the precise accelerator timing information
- Locally a programmable oscillator can create frequencies in the range of 10 to 945 MHz
- and for debugging purposes the internal FPGA-clock can be used as source with lower quality

It is essential for a distributed control system, which spans along an accelerator with a length of a few kilometres, that firmware updates can be carried out remotely in a secure manner and the hardware is not malfunctioning by inconsistent firmware images. The **JTAG interface** of DAMC2-00 supports several ways to reload the PROM and/or the FPGA additionally to the standard procedure of upgrading via the local pin header. For security reasons the PROM contains several firmware versions, which are selectable by the MMC. Included is a verified basic revision as a fallback solution, which is not being modified during upgrades. Three possible remote update scenarios are implemented:

- The first one uses the AMC JTAG interface available from the xTCA backplane, which is defined in the μ TCA standard. This solution depends on general JTAG controller for the crate
- A more exotic but rather fast possibility is the update via the crate controller and its PCIe interface using the XILINX ACE Player
- If none of these two methods are working, the firmware still can be updated via IPMI / I2C using the MMC as JTAG controller, which is the slowest of all possibilities.

The PCIe interface accomplishes data transfer between the DAMC2-00 and Host CPU. The μ TCA system provides more then 400 MB/sec transfer speed over 4 lanes available in DAMC2-00. Further lines of ports 12 to 15 of backplane – **4GTP** can be used to combine ADC data of several boards via Giga-bit links to the DAMC2-00. This configuration can be implemented for calculation of vector sum of 32 cavities.

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The **M-LVDS** signals on backplane of xTCA are used for some clock, trigger and interlock distributions.

Additional improvements are an increased SDRAM size of 1 Gbit operating at a 32-bit wide bus, a plug in position, which is now compliant to a FPGA Mezzanine Card (FMC) and four optical links (SFP) at the front panel. Some of the new features are being presented in more detail in the following.

DESY has contributed to the xTCA specifications, which are now about to be released, and was therefore able to develop a compliant board at such an early stage.

2.1 Xilinx Virtex-5, XC5VLX50T-1FF1136C

The DAMC2-00 development is motivated as an efficient but also economical solution for several applications at the XFEL accelerator control system. In this respect also the choice of the FPGA tries to balance between cost effectiveness and performance. The VIRTEX-5 LXT platform of FPGAs (Xilinx) is optimized for high-performance logic with low-power serial connectivity. The relative cheap FPGA - XC5VLX50T-1FF1136C was selected for the DAMC2-00 as base element. Main parameters of the XC5VLX50T-1FF1136C [2] are:

- 1 One PCI Express Endpoint block [3]
- 2 Four Ethernet MAC Blocks [4]
- 3 Twelve RocketIO GTP Low-Power Transceivers [5]
- 4 Maximum of 480 user I/O [6]
- 5 48 DSP48E slices
- 6 60 Blocks RAM/FIFO, each has 36Kbit
- 7 Clock Management Tiles: twelve DCM and six PLL
- 8 Configuration Memory – 14.1 Mbits
- 9 Package – FF1136
- 10 Area – 35 x 35mm.

The usage I/O resources of selected FPGA is shown in Table 1

Table 1 FPGA I/O resources

INTERFACE	I/O PINS
DDR2 interface	120
MMC interface	7
FMC interface (VITA 57.1)	72

INTERFACE	I/O PINS
PCIe Interface to uTCA Backplane	4 GTP
User interface to uTCA Backplane	4 GTP
SFP interface at Front panel	28 + 4 GTP
uRTM interface	112
M-LVDS interface to uTCA Backplane	38
Clock, control, LEDs	23
Total Number of I/O pins	400 of 480

2.2 Virtex-5 system monitor

Every member of the Virtex®-5 FPGA families contains a single System Monitor, which is located in the centre of every die [7]. The System Monitor function is built around a 10-bit, 200-kSPS (kilosamples per second) Analog-to-Digital Converter (ADC). When combined with a number of on-chip sensors, the ADC is used to measure FPGA physical operating parameters like on-chip power supply voltages and die temperatures.

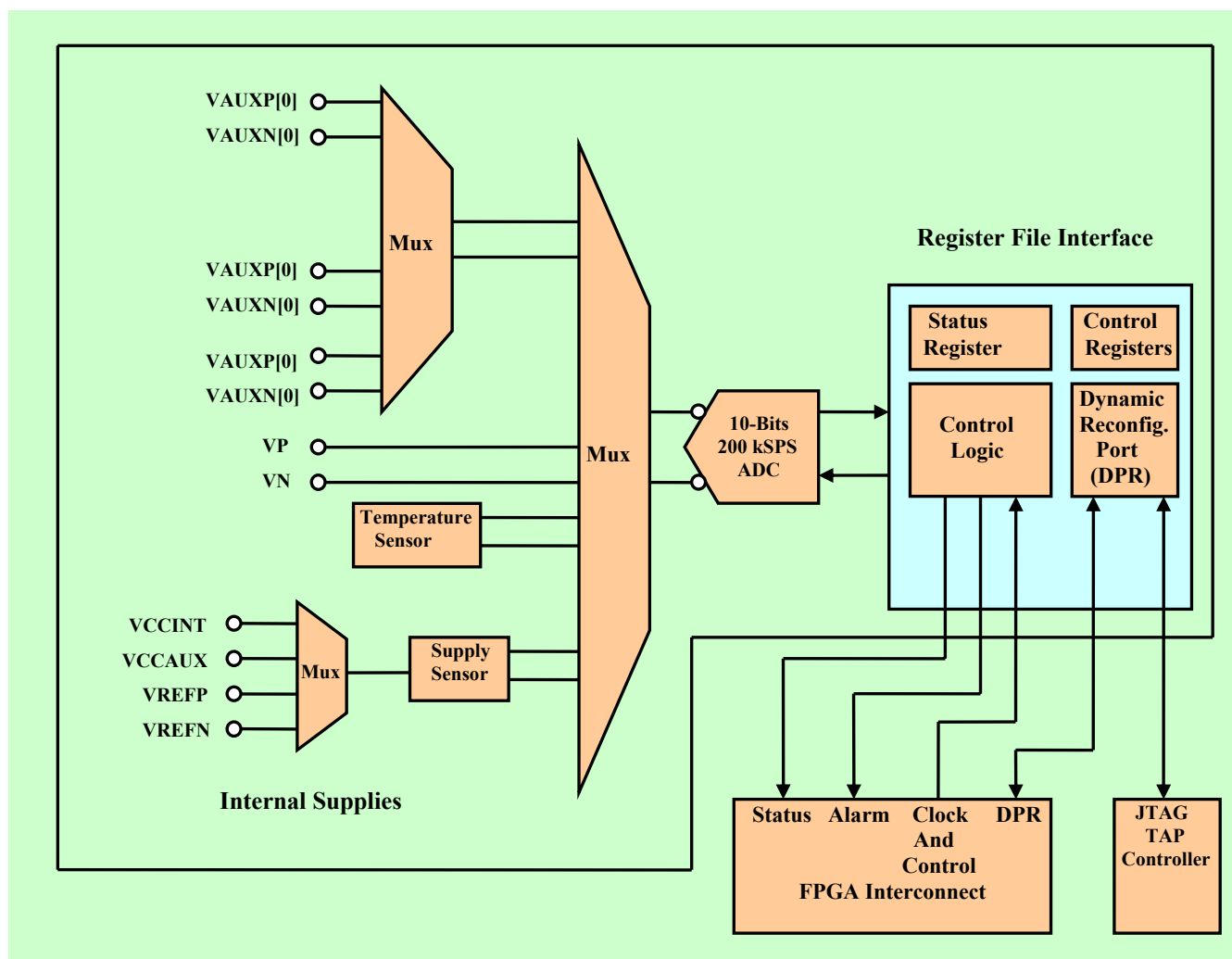


Figure 5 Block diagram of System monitor

Access to external voltages is provided through a dedicated analog-input pair (VP/VN) and 16 user selectable analog inputs, known as auxiliary analog inputs (VAUXP [15:0], VAUXN [15:0]). The external analog inputs allow the ADC to monitor the physical environment of the board or enclosure. System Monitor is fully functional on power up, and measurement data can be accessed via the JTAG port pre-configuration. Figure 5 shows the System Monitor block diagram. In DAMC2-00 the system monitor is used for measure temperature and power supply of FPGA only.

2.3 GTP interface

The RocketIO™ GTP Transceiver is a full-duplex serial transceiver for point-to-point transmission applications. Up to 24 transceivers are available on a single Virtex-5 LXT/SXT FPGA, depending on the part being selected. The transceiver block is designed to operate at any serial bit rate in the range of 100 Mb/s to 3.75 Gb/s per channel, including the specific bit rates used by the communications standards listed in the following table 2. Multiple channels can be bonded together for increased data throughput.

Table 2 Communication Standards Supported by the VIRTEX-5 GTP

STANDARDS	CHANNELS (# OF TRANSCEIVERS)	I/O BIT RATE (GB/S)
PCI EXPRESS	1, 2, 4, 8	2.5
SFI-5	1	2.488 – 3.125
OC-12	1	0.622
OC-48	1	2.488
Fibre Channel	1	1.06
		2.12
Gigabit Ethernet	1	1.25
XAUI (10-Gbit Ethernet)	4	3.125
10-Gbit Fibre Channel	4	3.1875
Infiniband	1, 4	2.5
HD-SDI	1	1.485
		1.4835
Serial ATA	1	1.5
		3.0
Serial Rapid I/O	1, 4	1.25
		2.5
		3.125
Aurora (Xilinx protocol)	1, 2, 3, 4, ...	0.100 – 3.75

The Virtex-5 transceivers are grouped into tiles with two transceivers per tile. The two transceivers in each tile share a single PLL and other resources involving the reset and power control.

Figure 6 shows the 12 RocketIO transceiver ports of XC5VLX50T-1FF1136C used on the DAMC2-00 board.

A trailing number '0' or '1' is used to distinguish between the two transceivers in the tile. These transceiver tiles are physically located into a single column on the die. Each tile has a placement name associated to its X-Y coordinate on the die. For example, GTP_Dual_X0Y0 is the first tile in the column.

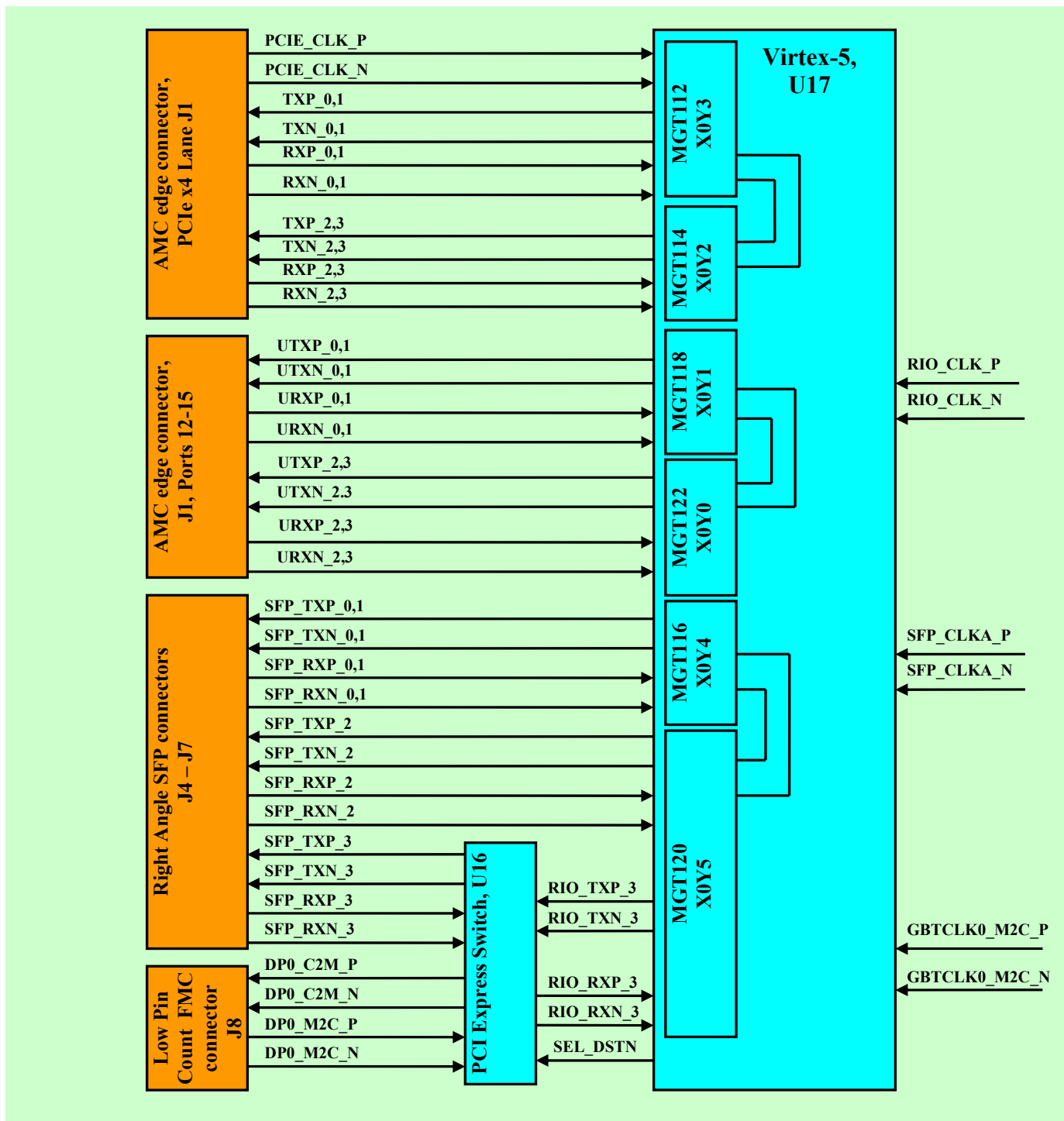


Figure 6 GTP ports of DAMC2-00

The GTP_Dual placement name is used in the User Constraint File (UCF) to map specific tiles on the device to those instantiated in a HDL design.

Each GTP_Dual tile has a reference clock input that can also be used by adjacent tiles up to three tiles away. Four reference clocks for different GTP_Dual tiles are used:

- PCIE_CLK_P/N – clock for PCI Express interface, which is described in **following chapters**
- RIO_CLK_P/N – clock for High Speed application specific edge interface, see **2.3.3, 2.8.1**
- SFP_CLKA_P/N – clock for high-speed optical links, see **2.3.4, 2.8.1, 2.8.2**
- GBTCLK0_M2C_P/N – clock for multi-gigabit interface between the DAMC2-00 and FMC mezzanine module, see **2.6.2**

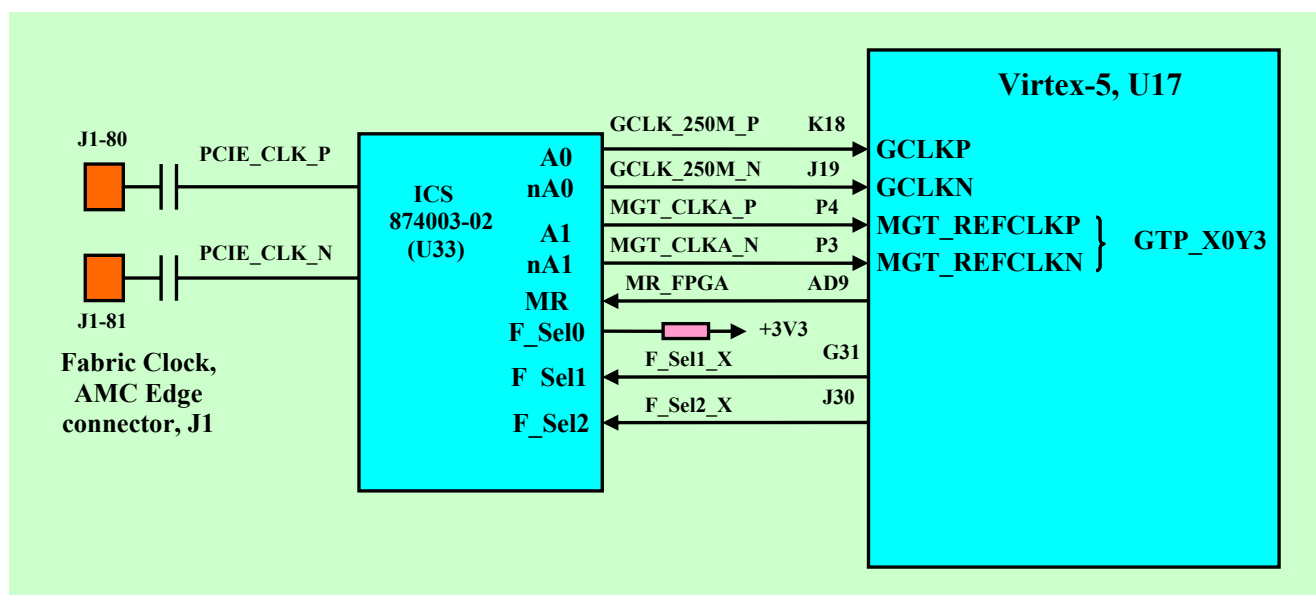


Figure 7 PCI Express clock and control

The DAMC2-00 board connects the AMC Fabric Clock A+ and A- to ICS874003-02 PCI Express Clock Jitter attenuator (U33). The ICS device has three LVDS outputs. One pair (QA0, QA0#) is connected to GTP tile X0Y3 MGT REFCLK pins P4 and P3 through two DC blocking capacitors. The second one (QA1, QA1#) is connected to the FPGA global clock inputs K18 and J19. The third output pairs (QB, QB#) is not used. Figure 7 shows the connection from the AMC Edge connector to the jitter attenuator and then to the FPGA.

2.3.1 ICS 874003-02 PCI Express jitter attenuator

The ICS874003-02 is a high performance Differential-to-LVDS Jitter Attenuator designed for the use in PCI Express systems. In some PCI Express systems, the PCI Express clocks are generated from a low bandwidth, high phase noise PLL frequency synthesizer. In these systems, a jitter attenuator may be required to attenuate high frequency random and deterministic jitter components from the PLL synthesizer and from the system board. The ICS874003-02 has a bandwidth of 400 kHz. The 400 kHz provide an intermediate bandwidth that can easily track triangular spread

Table 3 F_SEL [2:0] Function Table

Inputs			Outputs	
F_SEL2	F_SEL1	F_SEL0	QA0/nQA0, QA1/nQA1	QB0/nQB0
0	0	0 (*)	2	NU
1	0	0 (*)	5	NU
0	1	0 (*)	4	NU
1	1	0 (*)	2	NU
0 (**)	0 (**)	1 (**)	÷ 2 -> 250MHz	NU
1	0	1	÷ 5 -> 100MHz	NU
0	1	1	÷ 4 -> 125MHz	NU
1	1	1	÷ 4 -> 125MHz	NU

* - unused setting

** - default settings

NU – not used

The input frequency multiplies by 5 and then divided by coefficient, which is defined by F_SEL [2:0] inputs.

2.3.2 AMC PCI Express 4X edge interface

Four of the GTP transceivers (MGT112, MGT114) are connected to the Fat Pipe region of AMC edge connector and provide PCI Express interface to Backplane of xTCA crate. The PCI Express is an enhancement to the PCI architecture where the parallel bus has been replaced with a scalable, serial interface. The differences in the electrical interface are transparent to the software, so existing PCI software implementations are compatible. The usage of the DAMC2-00 board in a PCI Express application requires the implementation of the PCI Express protocol in the FPGA. The PCI Express Endpoint Block embedded in the Virtex-5 FPGA implements the PCI Express protocol and the physical layer interface to the GTP ports. This block must be instantiated in the user design. For more information, see the “Virtex-5 Endpoint Block for PCI Express Designs User Guide” on the Xilinx web site [3]. The PCI Express electrical interface on the DAMC2-00 board consists of four lanes, each of lanes having a unidirectional transmit and receive differential pair. Each lane supports the first generation data rate of 2.5 Gbps. In addition to the four serial lanes, there is a 100MHz reference clock – MGT_CLKA_P/N. In order to work correctly, add-in

cards must use the 100MHz reference clock provided over the DAMC2-00 edge connector to be frequency locked with the host system. The following Figure 9 shows the DAMC2-00 edge connector – Fat pipe region, and PCI Express interface to the Virtex-5 FPGA.

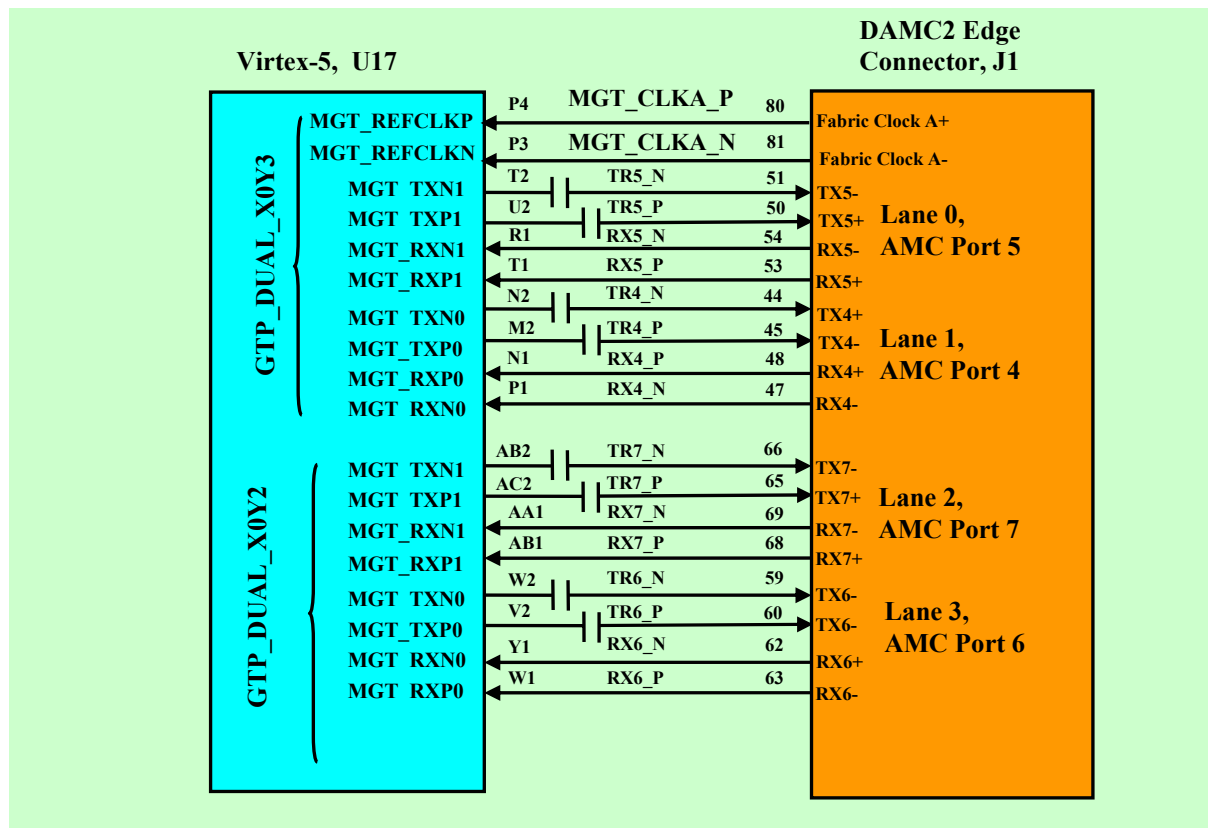


Figure 9 Four Lanes PCI Express Interface

The PCI Express transmit lanes are AC coupled (DC blocking capacitors are included in the signal path) on the DAMC2-00 board as required by the PCI Express specification. The Virtex-5 PCI Express interface takes advantage of the polarity inversion feature of the GTP transceivers. The “P” and “N” of all of the some PCI Express lanes are swapped on the board to improve the PCB routing. Each GTP has attributes that are used to enable polarity inversion on either the transmit or receive pairs, or both. The polarity inversion attributes are “TXPOLARITY” for the transmit pairs and “RXPOLARITY” for the receive pairs. Setting these attributes to logic 1 enables the inversion.

2.3.3 High Speed application specific edge interface

The four GTP transceivers are connected to Port 12 -15 of edge connectors, Figure 10. These interfaces use the wire-ring topology and will provide high speed connections to neighbours module in xTCA crate. The details usage of these interfaces should be defined latter by xTCA specification and depend from Backplane topology.

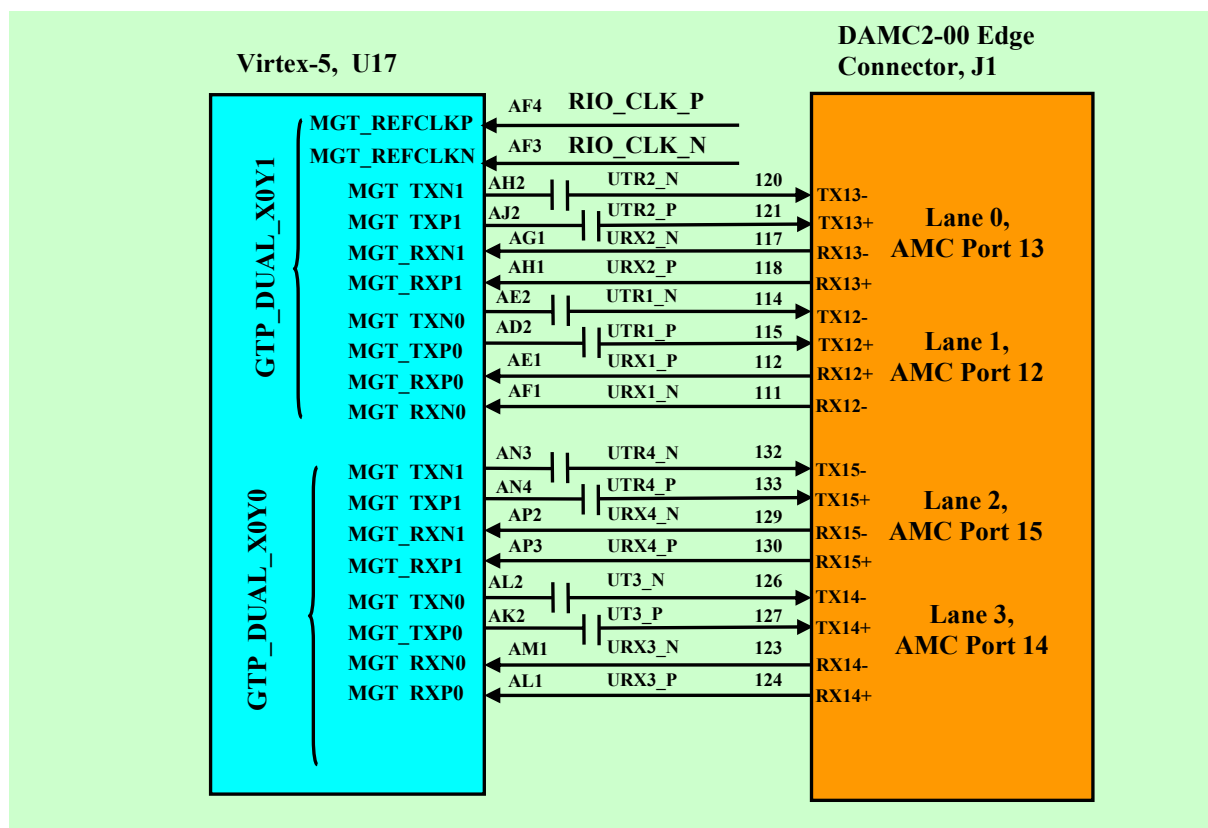


Figure 10 GTP interface to Edge Connector, Ports 12 -15

2.3.4 GTP interfaces to SFP

The DAMC2-00 board has four sockets (J4 - J7) for installation of compact hot-pluggable SFP transceiver. The Small Form-factor Pluggable (SFP) transceiver can support interfaces with data rate up to 4.25 Gbit/s. The SFP transceivers can be used for SONET, Gigabit Ethernet, Fibre Channel and other communication standards. The DAMC2-00 board provide up to four High Speed optical interfaces. Three GTP transceivers of Virtex-5 are connected to the SFP sockets directly and one of GTP is connected to SFP socket through PCI Express switch – TS2PCIE412, U16. The TS2PCIE412 is a 4-channel PCIe 2:1 multiplexer/demultiplexer switch that can be used to route one PCIe data lane between two possible destinations or two PCIe data lanes to one destination. Each channel consists of differential pairs of receive (RX) and transmit (TX) signals and operates at a signal-processing bandwidth speed, which supports the PCIe standard of 2.5 Gbps. One of destination for this switch is SFP socket, J7 and second one FMC connector, J8. SFP interface is shown on Figure 11.

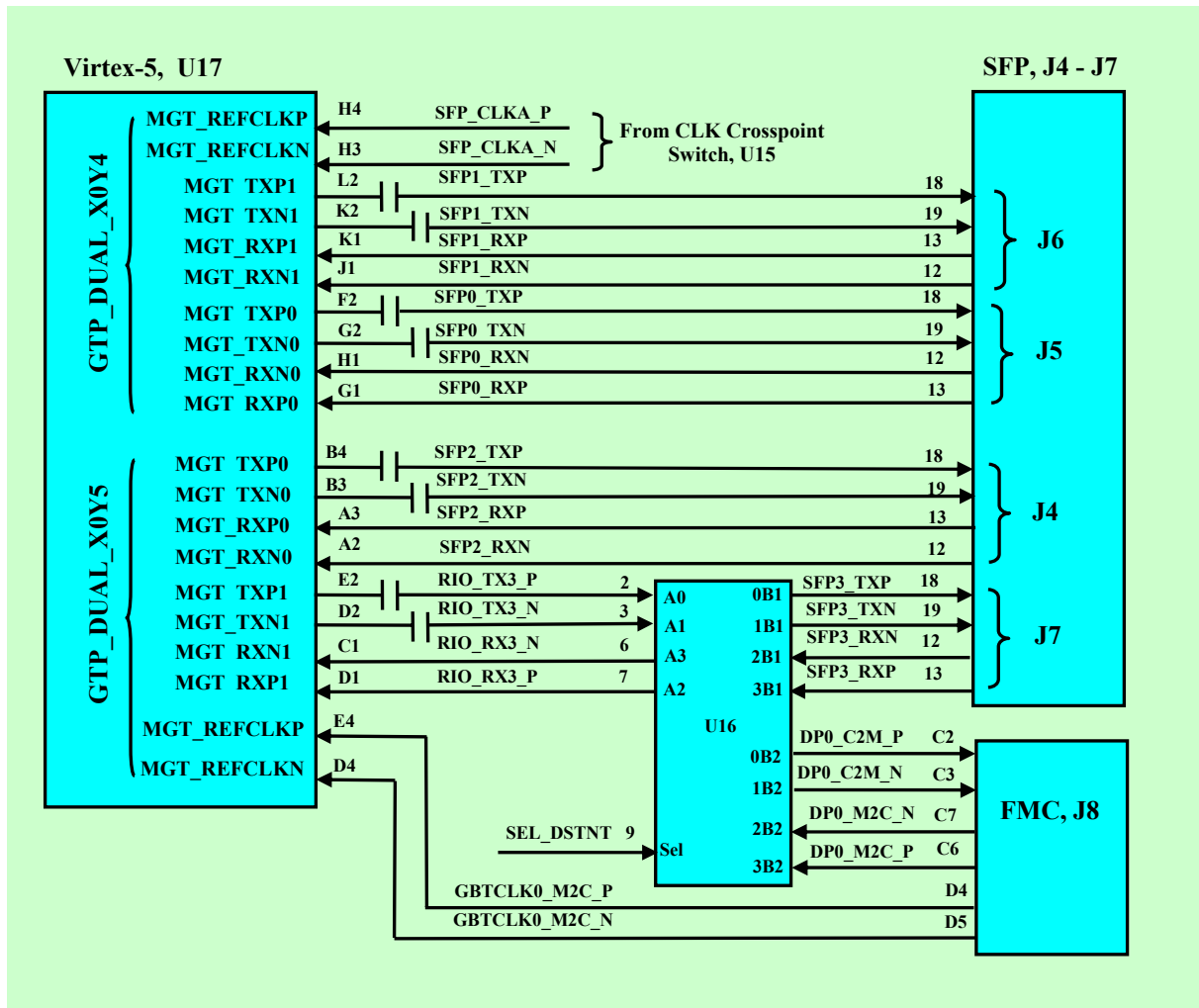


Figure 11 SFP&FMC High Speed Interfaces

Each channel consists of differential pairs of receive (RX) and transmit (TX) signals and operates at a signal-processing bandwidth speed, which supports the PCIe standard of 2.5 Gbps. One of destination for this switch is SFP socket, J7 and second one FMC connector, J8. SFP interface is shown on Figure 10.

2.3.5 4-channel 8:16 Multiplexer/Demultiplexer PCI Express Switch

The TS2PCIE412 is 4-channel PCIe 8:16 Multiplexer/Demultiplexer Passive FET Switch, Figure 12.

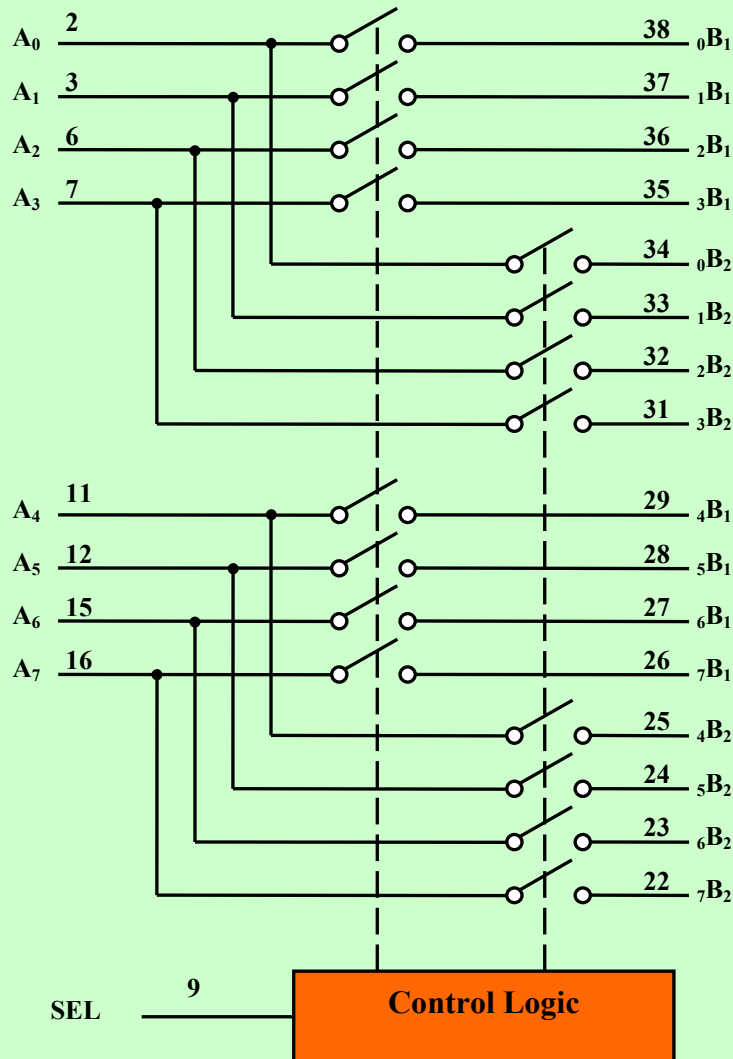


Figure 12 Functional Diagram TS2PCIE412

Main features of it are:

1. Compatible With PCI Express (PCIe) Standard
2. Wide Bandwidth of over 3 Gbps
3. Low Crosstalk (XTALK = -32 dB Typ at 1.25 GHz)
4. $O_{IRR} = -36.3\text{dB}$ Typical at 1.25 GHz
5. Low Bit-to-Bit Skew ($t_{sk(O)} = 0.06\text{ ns}$ Typical)
6. V_{DD} Operating Range: 1.5 V to 2 V
7. I_{off} Supports Partial Power-Down Mode Operation
8. Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II

9. ESD Performance Tested Per JESD 22 – 2000-V Human-Body Model

10. (A114-B, Class II) – 1000-V Charged-Device Model (C101)

The device is controlled with one select input (SEL) pin, where SEL controls the data path of the multiplexer/demultiplexer and can be connected to any GPIO in the system. The unselected channel is set in a high-impedance state, Table 4.

Table 4 TS2PCIE412 Function Table

SEL	FUNCTION
L	A_n to $_nB_1$
H	A_n to $_nB_2$

2.4 SFP Transceivers

The mechanical and electrical interfaces for all SFP transceivers can be found in [9]. Figure 13 below shows the pin names and numbering for the connector block on the host board. For EMI protection the signals to the 20-pin connector should be shut off when the transceiver is removed. Standard board layout practices such as connections to Vcc and GND with Vias, use of short and equal-length differential signal lines, use of microstrip-lines and 50Ω terminations are recommended.

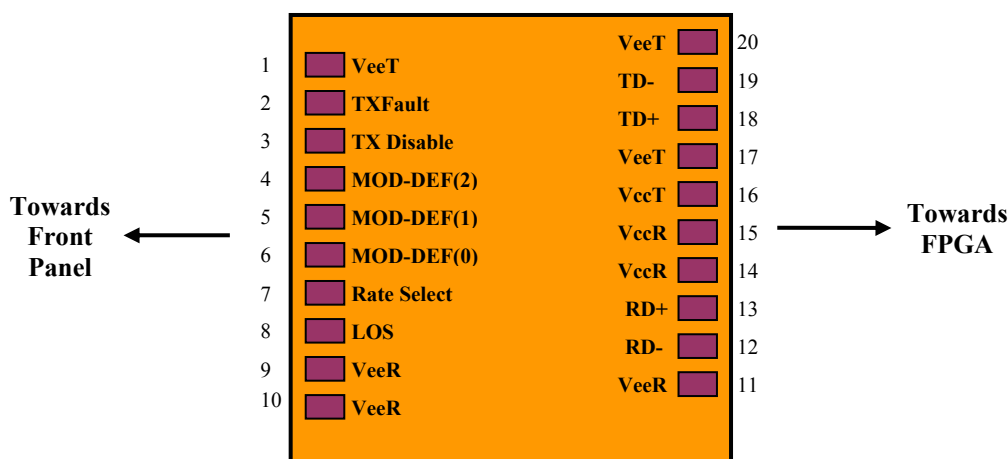


Figure 13 Diagram of Host Board SFP Connector Block

The pin functions are defined in Table 5 and the accompanying notes.

Table 5 SFP Pin Function Definition

PIN NUMBER	NAME	FUNCTION	PLUG SEQ.	NOTES
1	VeeT	Transmitter Ground	1	
2	TX Fault	Transmitter Fault Indication	3	Note 1
3	Tx Disable	Transmitter disable	3	Note2, Module disables on High or open
4	MOD-DEF2	Module Definition 2	3	Note 3, 2 wire serial ID interface
5	MOD-DEF1	Module Definition 1	3	Note 3, 2 wire serial ID interface
6	MOD-DEF0	Module Definition 0	3	Note 3, Grounded in Module
7	Rate Select	Select between full or reduced receiver bandwidth	3	Note 4, Low or Open – reduced bandwidth, High – full bandwidth
8	LOS	Loss of signal	3	Note 5
9	VeeR	Receiver Ground	1	Note 6
10	VeeR	Receiver Ground	1	Note 6
11	VeeR	Receiver Ground	1	Note 6
12	RD-	Inv. Received Data Out	3	Note 7
13	RD+	Received Data Out	3	Note 7
14	VeeR	Receiver Ground	1	Note 6
15	VccR	Receiver Power	2	3.3 ± 5%, Note 8
16	VccT	Transmitter Power	2	3.3 ± 5%, Note 8
17	VeeT	Transmitter Ground	1	Note 6
18	TD+	Transmit Data In	3	Note 9

PIN NUMBER	NAME	FUNCTION	PLUG SEQ.	NOTES
19	TD-	Inv. Transmit Data In	3	Note 9
20	VeeT	Transmitter Ground	1	Note 6

Plug Seq.: Pin engagement sequence during hot plugging.

Notes:

1) **TX Fault** is an open collector/drain output, which should be pulled up with a 4.7K – 10K Ω resistor on the host board. Pull up voltage between 2.0V and VccT, R+0.3V. When high, output indicates a laser fault of some kind. Low indicates normal operation. In the low state, the output will be pulled to < 0.8V.

2) **TX disable** is an input that is used to shut down the transmitter optical output. It is pulled up within the module with a 4.7 – 10 K Ω resistor. Its states are:

- Low (0 – 0.8V): Transmitter on
- (>0.8, < 2.0V): Undefined
- High (2.0 – 3.465V): Transmitter Disabled
- Open: Transmitter Disabled

3) **Mod-Def 0, 1, 2.** These are the module definition pins. They should be pulled up with a 4.7K – 10K Ω resistor on the host board. The pull-up voltage shall be VccT or VccR

Mod-Def 0 is grounded by the module to indicate that the module is present

Mod-Def 1 is the clock line of two wire serial interface for serial ID

Mod-Def 2 is the data line of two wire serial interface for serial ID

4) **Rate Select** is an optional input used to control the receiver bandwidth for compatibility with multiple data rates (most likely Fibre Channel 1x and 2x Rates). If implemented, the input will be internally pulled down with > 30k Ω resistor. The input states are:

- Low (0 – 0.8V): Reduced Bandwidth
- (>0.8 , < 2.0V): Undefined
- High (2.0 – 3.465V): Full Bandwidth
- Open: Reduced Bandwidth

5) **LOS** (Loss of Signal) is an open collector/drain output, which should be pulled up with a 4.7K – 10K Ω resistor. Pull up voltage between 2.0V and VccT, R+0.3V. When high, this output indicates the received optical power is below the worst-case receiver sensitivity (as defined by the

standard in use). Low indicates normal operation. In the low state, the output will be pulled to $< 0.8V$.

6) **VeeR and VeeT** may be internally connected within the SFP module.

7) **RD-/+** are the differential receiver outputs. They are AC coupled $100\ \Omega$ differential lines which should be terminated with $100\ \Omega$ (differential) at the user SERDES. The AC coupling is done inside the module and is thus not required on the host board. The voltage swing on these lines will be between 370 and 2000 mV differential (185 – 1000 mV single ended) when properly terminated.

8) **VccR and VccT** are the receiver and transmitter power supplies. They are defined as $3.3V \pm 5\%$ at the SFP connector pin. Maximum supply current is 300 mA. Recommended host board power supply filtering is shown below. Inductors with DC resistance of less than $1\ \Omega$ should be used in order to maintain the required voltage at the SFP input pin with 3.3V supply voltage. When the recommended supply filtering network is used, hot plugging of the SFP transceiver module will result in an inrush current of no more than 30 mA greater than the steady state value. VccR and VccT may be internally connected within the SFP transceiver module.

9) **TD-/+** are the differential transmitter inputs. They are AC-coupled, differential lines with $100\ \Omega$ differential termination inside the module. The AC coupling is done inside the module and is thus not required on the host board. The inputs will accept differential swings of 500 – 2400 mV (250 – 1200 mV single-ended), though it is recommended that values between 500 and 1200 mV differential (250 – 600 mV single-ended) be used for best EMI performance.

2.5 Telecom Clocks and MLVDS Interfaces

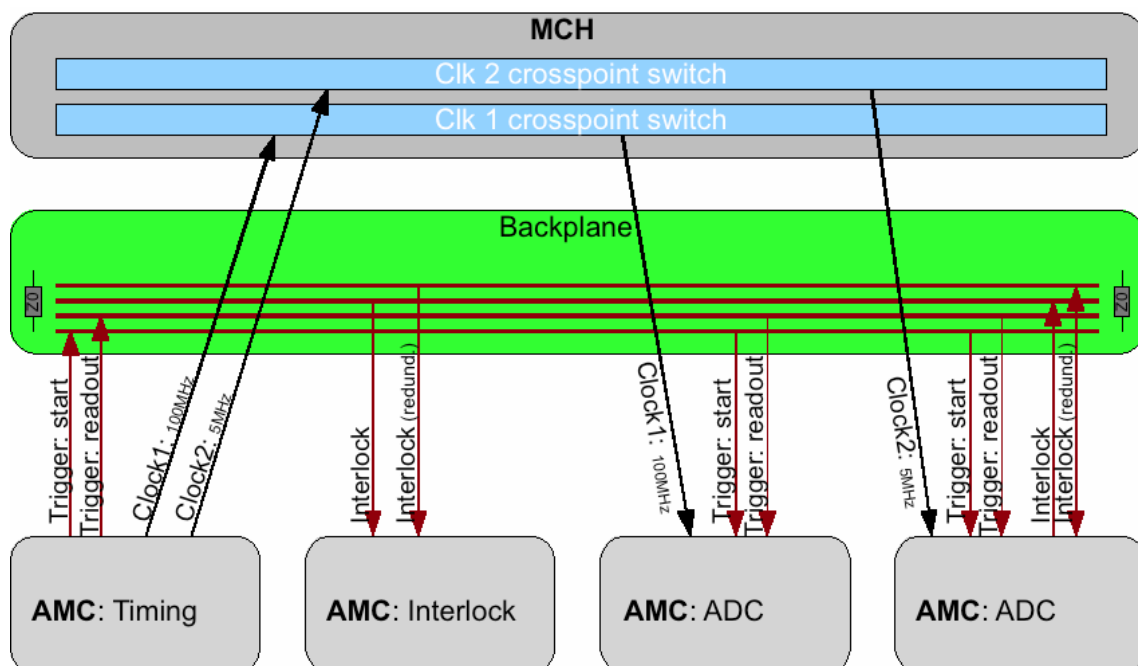


Figure 14 Example using radial clocks and bussed triggers

Figure 14 shows the general concept of xTCA specification for the clock, trigger and interlock signal connections [10]. Two radial clocks as defined in AMC.0 are used to distribute low jitter, high quality clocks by radial links from all AMC slots to the MCH. FCLKA is reserved and provided for PCIe usage. Ports 17 to 20 (Rx17/Tx17 to Rx20/Tx20) are used as a bus for trigger, clock and interlock signal distribution.

2.5.1 Radial clock circuitry

Two point-to-point lines from all AMC modules to the MCH implement the clocks as differential pairs (M-LVDS) as defined in AMC.0, Section 6.3.1. The lines are bidirectional – Figure 15.

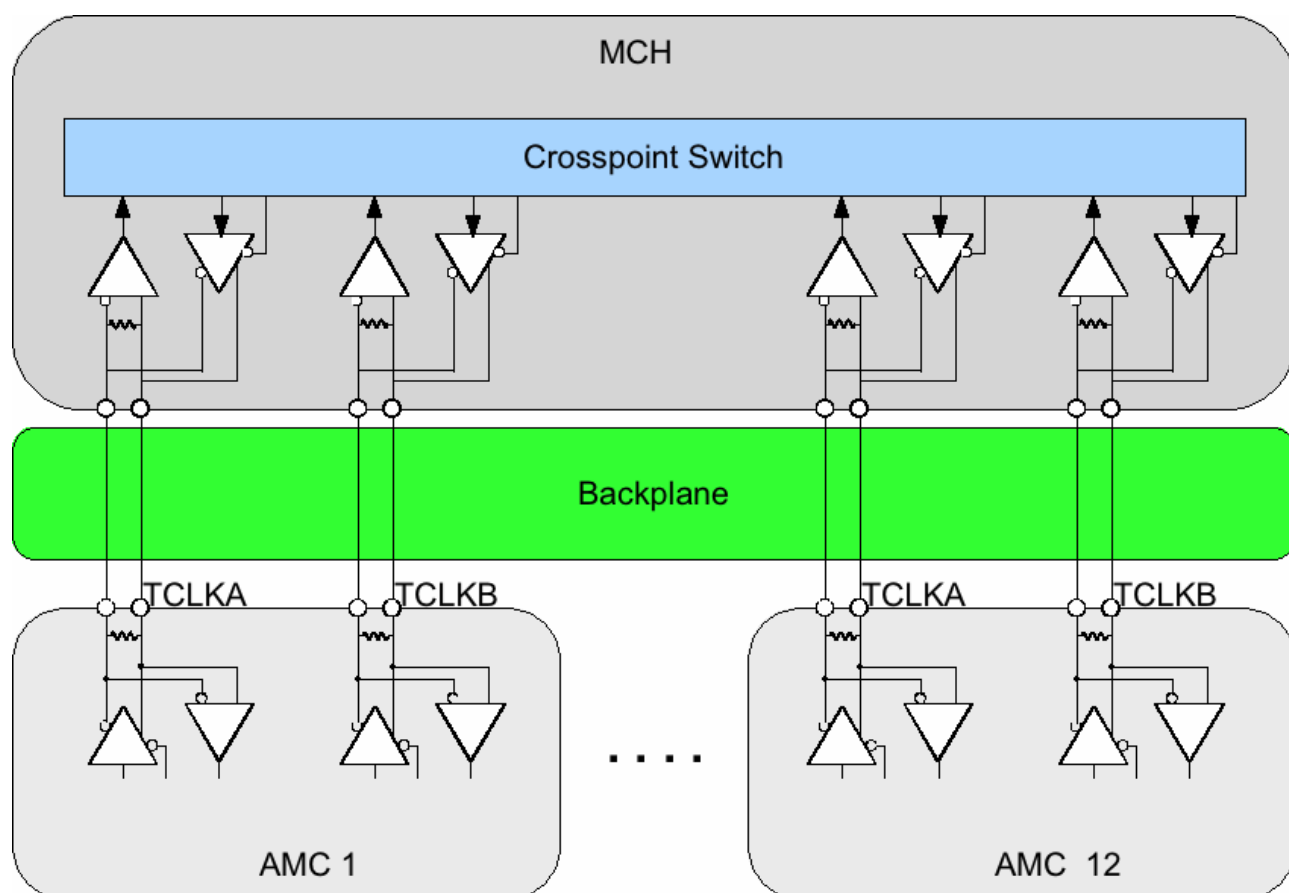


Figure 15 TCLKA&TCLKB are bidirectional.

Any AMC can be the source or the receiver of clock TCLKA or TCLKB. An AMC module may implement a receiver and may implement a transmitter or both. A 100 Ω line termination is required on both ends of the transmission line. These terminations are in both the MCH and the AMC module as shown in Figure 6-2. Any stubs in the PCB layout have to be avoided (see AMC.0, Section 6.3.1).

2.5.2 Ports 17 to 20 usage

The DAMC2-00 board uses ports 17 to 20 for trigger, clock and interlock signal distribution. The all of these signals are differential and **shall** be driven by M-LVDS, according to EIA/TIA-899. The DAMC2-00 module implements a receiver or a transmitter or both on every Rx and Tx pair of the ports 17 to 20. The differential lines on DAMC2-00 modules are shorter than 30 mm. The two Quad M-LVDS Transceivers (DS91M040) are used in DAMC2-00 for creation of M-LVDS interface – Figure 16.

The DS91M040 supports both M-LVDS type 1 and type 2 receiver inputs. The receiver inputs accept low voltage differential signals (LVDS, BLVDS, M-LVDS, LVPECL and CML)

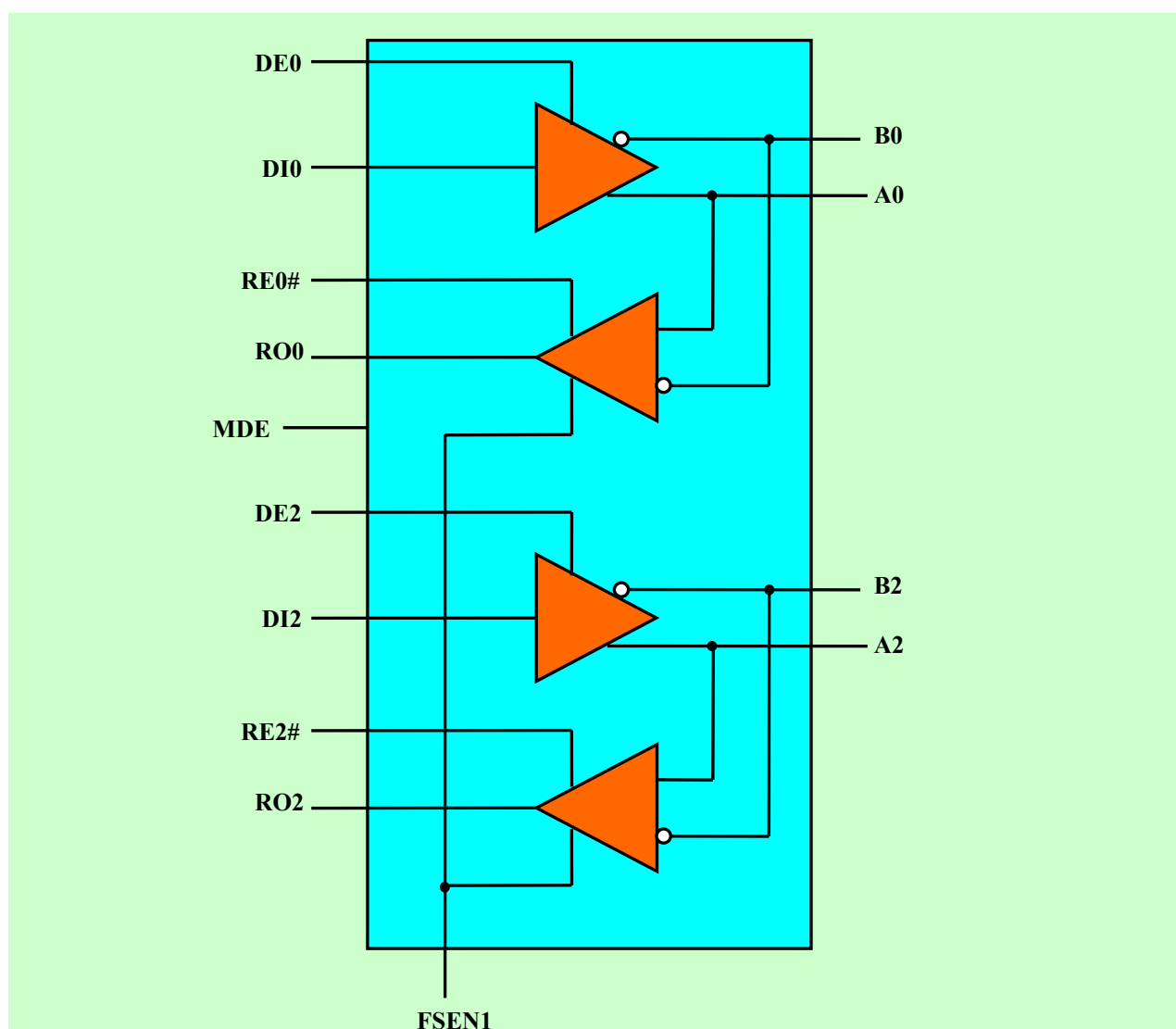


Figure 16 Block diagram of DS91M040 (half)

DE_x – Driver enable

DI_x – Driver Input

Rex# – Receiver enable pin. When RE# is high, the receiver is disabled. When RE# is low, the receiver is enabled

ROx – Receiver output

Ax – I/O, M-LVDS. Non-inverting driver output/Non-inverting receiver input

Bx - I/O, M-LVDS. Inverting driver output/Inverting receiver input

FSEN1 – Failsafe enable pin. **FSEN** = L -> Type 1 receiver Inputs

FSEN = H -> Type 2 receiver Inputs

MDE – Master enable. When MDE is H, the device is powered up. When MDE is L, the device overrides all other control and power down.

The tables 6, 7 and 8 show Truth Tables for different regimes of DS91M040

Table 6 DS91M040 Transmitting

INPUTS			OUTPUTS	
RE#	DE	DI	B	A
X	H	H	L	H
X	H	L	H	L
X	L	X	Z	Z

Table 7 DS91M040 as Type 1 Receiving

INPUTS				OUTPUTS
FSEN	RE#	DE	A - B	RO
L	L	X	$\geq +0.05V$	H
L	L	X	$\leq -0.05V$	L
L	L	X	$-0.05V \leq A-B \leq +0.05V$	Undefined
L	H	X	X	Z

Table 8 DS91M040 as Type 2 Receiving

INPUTS				OUTPUTS
FSEN	RE#	DE	A - B	RO
H	L	X	$\geq +0.15V$	H
H	L	X	$\leq +0.05V$	L
H	L	X	$+0.05V \leq A-B \leq +0.15V$	Undefined
H	H	X	X	Z

X – Don't care condition

Z – High impedance state

The different types of application can to use M-LVDS signals, one of variant shown in table 9

Table 9 Example usage of the eight bus lines for triggers, interlocks and clocks

AMC Port	Name	Description	Usage
Rx17	TrigStart	Start sampling data	Triggers
Tx17	TrigEnd	Stop sampling data	
Rx18	TrigReadOut	Start data transfer to CPU	
Tx18	ClkAux	Low performance clock	
Rx19	Reset	Reset of counter, dividers	
Tx19	Interlock 0	Interlock line 0	3 interlocks to provide 2 out of 3 redundancy
Rx20	Interlock 1	Interlock line 1	
Tx20	Interlock2	Interlock line 2	

2.6 FMC Interface

The DAMC2-00 has Plug in position for a VITA 57.1 compliant FPGA Mezzanine Card (FMC) – Figure 17.

The FPGA Mezzanine Card (FMC) standard [10], developed by a consortium of companies ranging from FPGA vendors to end users, specifically targets FPGAs, increasing I/O flexibility and lowering costs in a broad range of applications. The purpose of this standard is to create an I/O mezzanine module, which works intimately with an FPGA processing device.

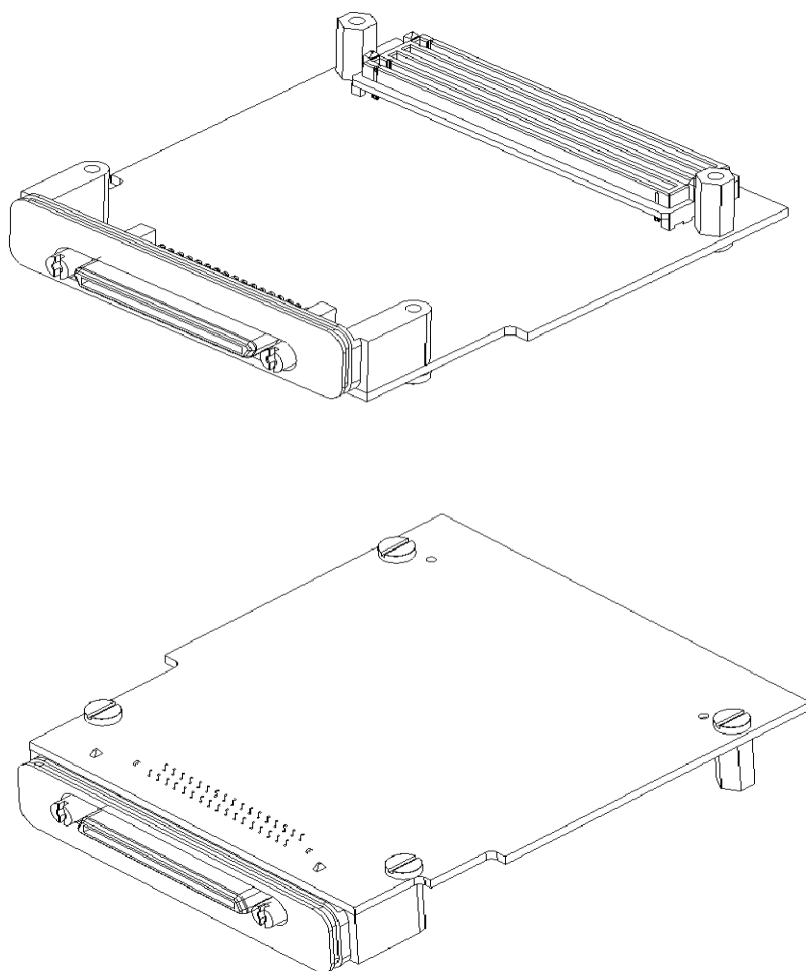


Figure 17 Single width FMC module

The focus is to create a mezzanine module that minimizes the handling and formatting of the transceived data.

The aims are to:

- Maximize data throughput

- Minimize latency
- Reduce FPGA design complexity
- Minimize system costs
- Reduce system overheads.


Table 10 Signal definition for Low Pin Count Connector

	K	J	H	G	F	E	D	C	B	A
1	NC	NC	VREF_A_M2C	GND	NC	NC	PG_C2M	GND	NC	NC
2	NC	NC	PRSNT_M2C_L	CLK0_C2M_P	NC	NC	GND	DP0_C2M_P	NC	NC
3	NC	NC	GND	CLK0_C2M_N	NC	NC	GND	DP0_C2M_N	NC	NC
4	NC	NC	CLK0_M2C_P	GND	NC	NC	GBTCLK0_M2C_P	GND	NC	NC
5	NC	NC	CLK0_M2C_N	GND	NC	NC	GBTCLK0_M2C_N	GND	NC	NC
6	NC	NC	GND	LA00_P_CC	NC	NC	GND	DP0_M2C_P	NC	NC
7	NC	NC	LA02_P	LA00_N_CC	NC	NC	GND	DP0_M2C_N	NC	NC
8	NC	NC	LA02_N	GND	NC	NC	LA01_P_CC	GND	NC	NC
9	NC	NC	GND	LA03_P	NC	NC	LA01_N_CC	GND	NC	NC
10	NC	NC	LA04_P	LA03_N	NC	NC	GND	LA06_P	NC	NC
11	NC	NC	LA04_N	GND	NC	NC	LA05_P	LA06_N	NC	NC
12	NC	NC	GND	LA08_P	NC	NC	LA05_N	GND	NC	NC
13	NC	NC	LA07_P	LA08_N	NC	NC	GND	GND	NC	NC
14	NC	NC	LA07_N	GND	NC	NC	LA09_P	LA10_P	NC	NC
15	NC	NC	GND	LA12_P	NC	NC	LA09_N	LA10_N	NC	NC
16	NC	NC	LA11_P	LA12_N	NC	NC	GND	GND	NC	NC
17	NC	NC	LA11_N	GND	NC	NC	LA13_P	GND	NC	NC
18	NC	NC	GND	LA16_P	NC	NC	LA13_N	LA14_P	NC	NC
19	NC	NC	LA15_P	LA16_N	NC	NC	GND	LA14_N	NC	NC
20	NC	NC	LA15_N	GND	NC	NC	LA17_P_CC	GND	NC	NC
21	NC	NC	GND	LA20_P	NC	NC	LA17_N_CC	GND	NC	NC
22	NC	NC	LA19_P	LA20_N	NC	NC	GND	LA18_P_CC	NC	NC
23	NC	NC	LA19_N	GND	NC	NC	LA23_P	LA18_N_CC	NC	NC
24	NC	NC	GND	LA22_P	NC	NC	LA23_N	GND	NC	NC
25	NC	NC	LA21_P	LA22_N	NC	NC	GND	GND	NC	NC
26	NC	NC	LA21_N	GND	NC	NC	LA26_P	LA27_P	NC	NC
27	NC	NC	GND	LA25_P	NC	NC	LA26_N	LA27_N	NC	NC
28	NC	NC	LA24_P	LA25_N	NC	NC	GND	GND	NC	NC
29	NC	NC	LA24_N	GND	NC	NC	TCK	GND	NC	NC
30	NC	NC	GND	LA29_P	NC	NC	TDI	SCL	NC	NC
31	NC	NC	LA28_P	LA29_N	NC	NC	TDO	SDA	NC	NC
32	NC	NC	LA28_N	GND	NC	NC	3P3V/AUX	GND	NC	NC
33	NC	NC	GND	LA31_P	NC	NC	TMS	GND	NC	NC
34	NC	NC	LA30_P	LA31_N	NC	NC	TRST_L	GA0	NC	NC
35	NC	NC	LA30_N	GND	NC	NC	GA1	12P0V	NC	NC
36	NC	NC	GND	LA33_P	NC	NC	3P3V	GND	NC	NC
37	NC	NC	LA32_P	LA33_N	NC	NC	GND	12P0V	NC	NC
38	NC	NC	LA32_N	GND	NC	NC	3P3V	GND	NC	NC
39	NC	NC	GND	VADJ	NC	NC	GND	3P3V	NC	NC
40	NC	NC	VADJ	GND	NC	NC	3P3V	GND	NC	NC
			LPC Connector	LPC Connector			LPC Connector	LPC Connector		

The standard defines two types of connectors for FMC High Pin Count Connector (HPC) – 400 pins, and Low Pin Count Connector (LPC) – 160 pins. The DAMC2-00 has one slot for FMC with LPC connector. The signal assignment for Low Pin Count connector shall be defined as shown in Table 10.

2.6.1 The LPC signal definitions

The Low Pin Count connector uses only rows C, D, G and H.

DESY - FEA P.Vetrov Tel: +49 / 40-8998 – 2538 petr.vetrov@desy.de	Hardware Design Description (HDD) of the DESY Double Advanced Mezzanine Card	
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- The signal names with “C2M” indicate that the signal is driven by carrier card and received by the FMC IO mezzanine module
- The signal names with “M2C” indicate that the signal is driven by IO mezzanine module and received by the carrier card
- The postfix “_P” on a differential signals pairs, indicates the positive component of a differential signal
- The postfix “_N” on a differential signals pairs, indicates the negative component of a differential signal
- The postfix “_L” on a single ended signal, “PRSNT_M2C_L” and “TRST_L” indicate that these are active low signals
- Signals with a “_CC” postfix should be used as the preferred signals for clocks in source synchronous applications and should be connected to pins on the FPGA, which are identified for this purpose.

2.6.2 The LPC Pin Assignment

The LA [0:33] _P, LA [0:33] _N are user defined signals on Bank A located on the LPC.

The CLK0_C2M_P, CLK0_C2M_N – A differential pair that is assigned for a clock signal, which is driven from the carrier card to the IO Mezzanine Module.

The CLK0_M2C_P, CLK0_M2C_N – A differential pair that is assigned for a clock signal, which is driven from the IO Mezzanine Module to the carrier card.

The GBTCLK0_M2C_P, GBTCLK0_M2C_N – A differential pair shall be used as a reference clock for the multi-gigabit transceiver data pairs (DP) data signals.

The DP0_M2C_P, DP0_M2C_N, DP0_C2M_P, and DP0_C2M_N – these signals form 1 multi-gigabit transceiver data pairs.

The GA [0:1] – these signals provide geographical addressed of the module and are used for I2C channel select.

VREF_A_M2C – this is the reference voltage associated with the signalling standard used by the bank A data pins, LAxx. *In DAMC2-00 these signals does not use and left unconnected.*


3P3VAUX – a 3.3V auxiliary power supply, max current 20 mA, it shall be used for IPMI only.

VADJ - these pins carry an adjustable voltage level power from the carrier to the IO Mezzanine module. *DAMC2-00 provides only 2.5V on these pins, not adjustable*, max current 2 Amps.

3P3V – these pins carry 3.3V power from the carrier to the IO Mezzanine module, max current 3Amps.

12P0V – these pins carry 12V power from the carrier to the IO Mezzanine module, max current 1 Amps.

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DESY - FEA P.Vetrov Tel: +49 / 40-8998 – 2538 petr.vetrov@desy.de	Hardware Design Description (HDD) of the DESY Double Advanced Mezzanine Card	
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TRST_L – JTAG Reset. This signal provides asynchronous initialization of the TAP controller on the IO Mezzanine module. *This signal does not used by DAMC2-00*

TCK - JTAG Clock.

TMS – JTAG Mode Select.

TDI – JTAG Data In.

TDO – JTAG Data Out.

PRSENT_M2C_L – Module present signal. This signal allows the carrier to determine whether an IO Mezzanine module is present.

PG_C2M – Power Good Carrier Card. This signal asserts high by the carrier card when power supplies, VADJ, 12POV, 3P3V, are within tolerance.

SCL – System Management I2C serial clock.

SDA – System Management I2C serial data.

GND – this is signal ground.

2.7 The microRTM Interface

The main advantage of DAMC2-00 board is the ability to extend the basic functionality of the front module by connecting low-cost and task-oriented Micro Rear Transition Module - uRTM. It means the opportunity to create different type of hardware, which will be based on the small numbers (1-2) of expensive and complicated front module and many the relative cheap, task-oriented uRTM. In corresponded to xTCA specification [11] DAMC2-00 has three connectors, which provide interface to uRTM: guide/key socket and two ADF connectors – J30 and J31. Each of them is 30 pair plug.

2.7.1 Key Socket

The DAMC2-00 module shall implement a keying similar in function to the K2 keying in PICMG 3.0 R3.0, Section 2.3. The Female Key receptacle connector J15 is installed on the DAMC2-00. It has keying “3”, which corresponded to level of data signals between ± 1 to ± 3.3 V on J30 and J31 connectors.

2.7.2 Connectors J30 and J31

The ADF J30 has data, power and system management assigned to pins as shown in Table 11.

Table 11 Power/Management Pin Assignments for J30

ROW 1			ROW 2		
Col	Name	Description	Col	Name	Description
A	RTM_PWR	+12 Volts	A	RTM_PWR	+12 Volts
B	RTM_PWR	+12 Volts	B	RTM_PWR	+12 Volts
GND	RTM_GND	Ground	GND	RTM_GND	Ground
C	RTM_PS#	RTM present	C	RTM_MP	+3.3 Volts
D	RTM_SDA	I ² C Data	D	RTM_SCL	I ² C Clock
GND	RTM_GND	Ground	GND	RTM_GND	Ground
E	RTM_TCK	Optional JTAG TCK	E	RTM_TDI	Optional JTAG TDI
F	RTM_TDO	Optional JTAG TDO	F	RTM_TMS	Optional JTAG TMS
GND	RTM_GND	Ground	GND	RTM_GND	Ground

Table 12 has the pin assignment for the J30 connectors.

Table 12 J30 Pin Assignments

COL → ROW ↓	GND	F	E	GND	D	C	GND	B	A
10	GND[7]	F[7]	E[7]	GND[7]	D[7]	C[7]	GND[7]	B[7]	A[7]
9	GND[6]	F[6]	E[6]	GND[6]	D[6]	C[6]	GND[6]	B[6]	A[6]
8	GND[5]	F[5]	E[5]	GND[5]	D[5]	C[5]	GND[5]	B[5]	A[5]
7	GND[4]	F[4]	E[4]	GND[4]	D[4]	C[4]	GND[4]	B[4]	A[4]
6	GND[3]	F[3]	E[3]	GND[3]	D[3]	C[3]	GND[3]	B[3]	A[3]
5	GND[2]	F[2]	E[2]	GND[2]	D[2]	C[2]	GND[2]	B[2]	A[2]
4	GND[1]	F[1]	E[1]	GND[1]	D[1]	C[1]	GND[1]	B[1]	A[1]

COL → ROW ↓	GND	F	E	GND	D	C	GND	B	A
3	GND[0]	F[0]	E[0]	GND[0]	CLK2* AMC#	CLK2 *AMC	GND[0]	CLK2 RTM#	CLK2 RTM
2	GND	JTAG TMS	JTAG TDI	GND	SCL	MP	GND	PWR	PWR
1	GND	JTAG TDO	JTAG TCK	GND	SDA	PS#	GND	PWR	PWR

CLK2AMC, CLK2AMC# - is differential pair, which can be used for clock signals from uRTM to DAMC2-00 or for any user-defined differential signals. These signals are connected to Global Clock inputs of Virtex-5. These signals corresponded to **RTM1_S24_P/N** in electrical schematic of DAMC2-00

CLK2RTM, CLK2RTM# - is differential pair, which used ONLY for clock signals from DAMC2-00 to uRTM. These signals are going from of Crosspoint switch – U15. These signals corresponded to **CLK_EC_RTM_P/N** in electrical schematic of DAMC2-00

E/F3 – is user-defined signals, which are connected to Clock Capable pins of Virtex-5. These pins become regular user I/Os when not needed for clocks. If a single-ended clock is connected to the differential CC pair of pins, it must be connected to the positive (P) side of the pair.

The J31 connector is entirely user-defined usage, Table 13

Table 13 J31 Pin assignment

COL → ROW ↓	GND	F	E	GND	D	C	GND	B	A
10	GND[17]	F[17]	E[17]	GND[17]	D[17]	C[17]	GND[17]	B[17]	A[17]
9	GND[16]	F[16]	E[16]	GND[16]	D[16]	C[16]	GND[16]	B[16]	A[16]
8	GND[15]	F[15]	E[15]	GND[15]	D[15]	C[15]	GND[15]	B[15]	A[15]
7	GND[14]	F[14]	E[14]	GND[14]	D[14]	C[14]	GND[14]	B[14]	A[14]
6	GND[13]	F[13]	E[13]	GND[13]	D[13]	C[13]	GND[13]	B[13]	A[13]
5	GND[12]	F[12]	E[12]	GND[12]	D[12]	C[12]	GND[12]	B[12]	A[12]
4	GND[11]	F[11]	E[11]	GND[11]	D[11]	C[11]	GND[11]	B[11]	A[11]
3	GND[10]	F[10]	E[10]	GND[10]	D[10]	C[10]	GND[10]	B[10]	A[10]

COL → ROW ↓	GND	F	E	GND	D	C	GND	B	A
2	GND[9]	F[9]	E[9]	GND[9]	D[9]	C[9]	GND[9]	B[9]	A[9]
1	GND[8]	F[8]	E[8]	GND[8]	D[8]	C[8]	GND[8]	B[8]	A[8]

E/F17, E/F16, D/C10, D/C9, D/C8, B/A10, B/A9, B/A8 – are user-defined signals, which are connected to Clock Capable pins of Virtex-5. These pins become regular user I/Os when not needed for clocks. If a single-ended clock is connected to the differential CC pair of pins, it must be connected to the positive (P) side of the pair.

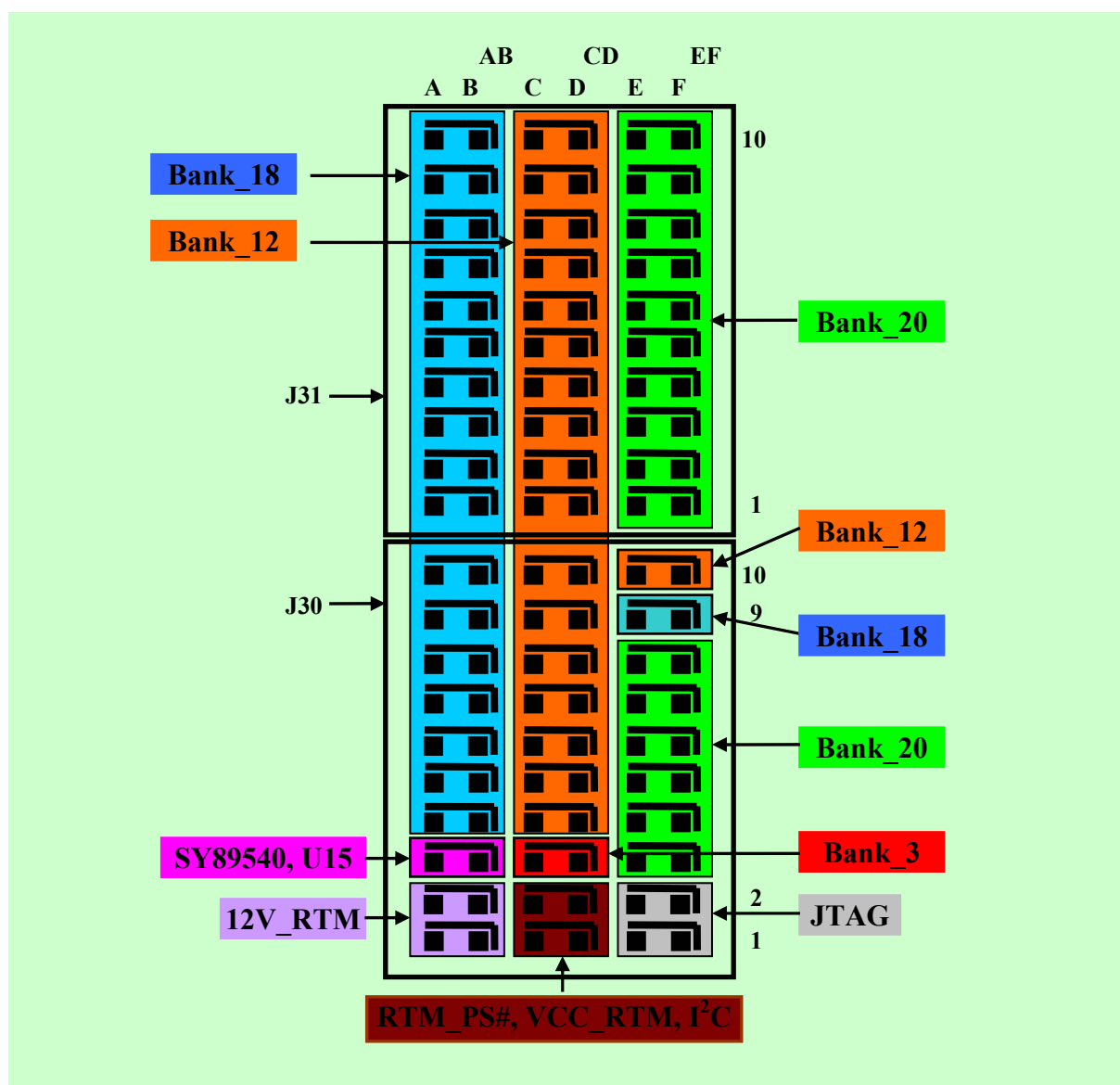



Figure 18 Connectors J30 and J31

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The user-defined pins are named by column 0 to 17 and row name A to F. Each pair A/B, C/D and E/F may be used as a differential pair or as two individual single-ended signals. If used as a differential signal pair A, C and E should be used as positive and B, D and F as negative signals. The uRTM interface is implemented on banks 12, 18, 20 of Virtex-5 – Figure 18, all of them use output drive voltage (Vcco) – 2.5 Volts, that is only I/O standards, which used Vcco = 2.5 Volts can be used. For example: LVDS_25, LVPECL_25, LVDCI_25 etc.

2.8 Clock signals

The DAMC2-00 board implements all necessary clocks for high-speed logic and RocketIO GTP transceiver designs but also provides the flexibility for the user to supply their own application specific clocks. The clock sources described in this section are used to derive the required clocks for the FPGA, μ RTM, FMC, SFP and the general system clocks for the logic design. For a description of the GTP reference clock sources and PCI Express clock, see Section 2.3.

DAMC2-00 has eleven clock sources:

- Differential Fabric Clock FCLKA (100MHz), sourced from AMC Edge connector
- Differential Telecom Clocks A+/A- (TCLKA) and B+/B- (TCLKB), sourced from AMC Edge connector
- Two differential clock – RIO_CLK_P/N and OSC_CLKA_P/N, sourced from two oscillators (Si570) – Q1 and Q4
- The differential SFP0_CLKA_P, SFP0_CLKA_N, sourced from Crosspoint Switch – U15, for GTP transceiver of FPGA, Banks 116 and 120
- FOXElectronics FXO-LC535R-200, 3.3V, 200-MHz, LVDS oscillator (Q3) for FPGA
- ABRACON's AWSCR-3.58MGD-T, 3.58 MHz single-ended quartz resonator (Q2) for MMC
- Differential clock GBTCLK0_M2C_P/N sourced by FMC Mezzanine Board for GTP transceiver of FPGA, Bank 120
- Differential clock CLK0_M2C_P/N, which is driven from FMC to FPGA
- Optional differential clock – RTM1_S24_P/N, which is driven from uRTM board to FPGA

2.8.1 RIO clocks

The four GTP transceivers, which are connected to Port 12 -15 of edge connectors use clock signal RIO_CLK_N/P. Si570 oscillator (Q4), which is produced by Silicon LABS, generates it. Main parameters of Si579 are:

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- Any-rate programmable output frequencies from 10 to 945 MHz and select frequencies to 1.4 GHz
- I²C serial interface
- 3rd generation DSPLL® with superior jitter performance
- Internal fixed crystal frequency ensures high reliability and low aging

The Si570 XO utilizes Silicon Laboratories' advanced DSPLL® circuitry to provide a low-jitter clock at any frequency. The Si570 is user-programmable to any output frequency from 10 to 945 MHz and select frequencies to 1400 MHz with <1 ppb resolution. The device is programmed via an I²C serial interface. Unlike traditional XO where a different crystal is required for each output frequency, the Si570 uses one fixed frequency crystal and a DSPLL clock synthesis IC to provide any-rate frequency operation. This IC-based approach allows the crystal resonator to provide exceptional frequency stability and reliability.

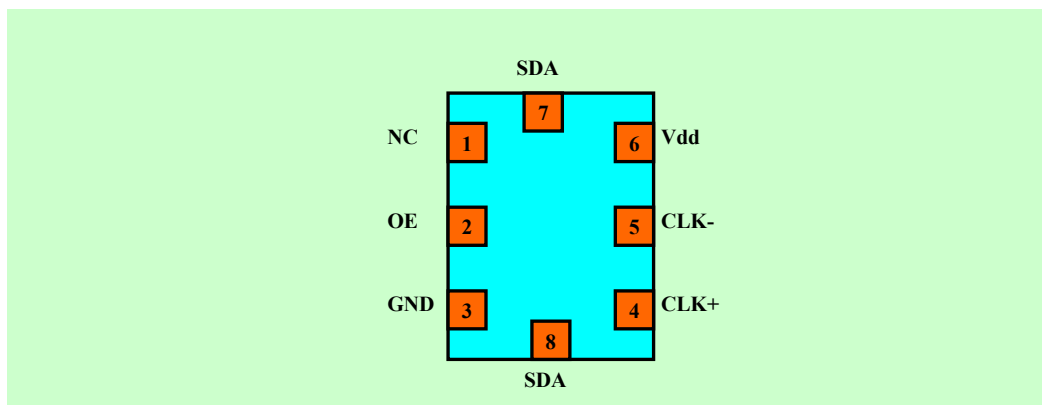


Figure 19 Si570 Pinout

In addition, DSPLL clock synthesis provides superior supply noise rejection, simplifying the task of generating low jitter clocks in noisy environments typically found in communication systems. Pinout of Si570 is shown on Figure 19, pin's definitions is done in Table 14

Table 14 Pin Description

PIN	NAME	TYPE	FUNCTION
1	NC	N/A	No connect.
2	OE	Input	Output Enable
3	GND	Ground	Electrical and case Ground
4	CLK+	Output	Oscillator output

PIN	NAME	TYPE	FUNCTION
5	CLK-	Output	Complementary Output
6	Vdd	Power	Power Supply Voltage
7	SDA	Bidirectional Open Drain	I ² C Serial Data
8	SCL	Input	I ² C Serial Clock

2.8.2 SFP and FMC clocks

The four SFP high-speed optical links uses the 116 and 120 GTP banks of Virtex-5. The bank 120 is shared between SFP and FMC interfaces. The SFP0_CLKA_P, SFP0_CLKA_N used as GTP Reference Clock, when both banks apply to SFP interfaces. The source of SFP0_CLKA_P/N differential clock is clock distribution scheme, which is based on the Crosspoint Switch – SY89540U, U15. The FMC interface of DAMC2-00 can support only one Lane of Gigabit Interface and uses the GBTCLKM2C_P/N differential clock as GTP Reference clock for bank 120.

2.8.3 Clock distribution

Different clocks can be routed simultaneously via a high precision cross point switch – SY89540U, to the μ RTM, the FMC, the SFP and to the FPGA. The following sources of clocks are implemented:

- The two high quality TCLKA and TCLKB clock lines from the μ TCA Backplane will typically distribute external signals like the precise accelerator timing information.
- Locally a programmable oscillator – Q1, can create frequencies in the range of 10 to 945 MHz
- The internal FPGA-clock can be used as source with relative lower quality for debugging purposes

The SY89540U is low-jitter, low skew, high-speed 4x4 crosspoint switch optimized for precision distribution application. The SY89540U guarantees data-rates up to 3.2Gbps over temperature and voltage. The SY89540U differential input can directly interfaces to any differential signal (AC or DC-coupled) as small as 100mV (200mVpp). The LVDS compatible outputs maintain extremely fast rise/fall times guaranteed to be less than 120ps.

The functional Block Diagram of SY89540U is shown on Figure 20.

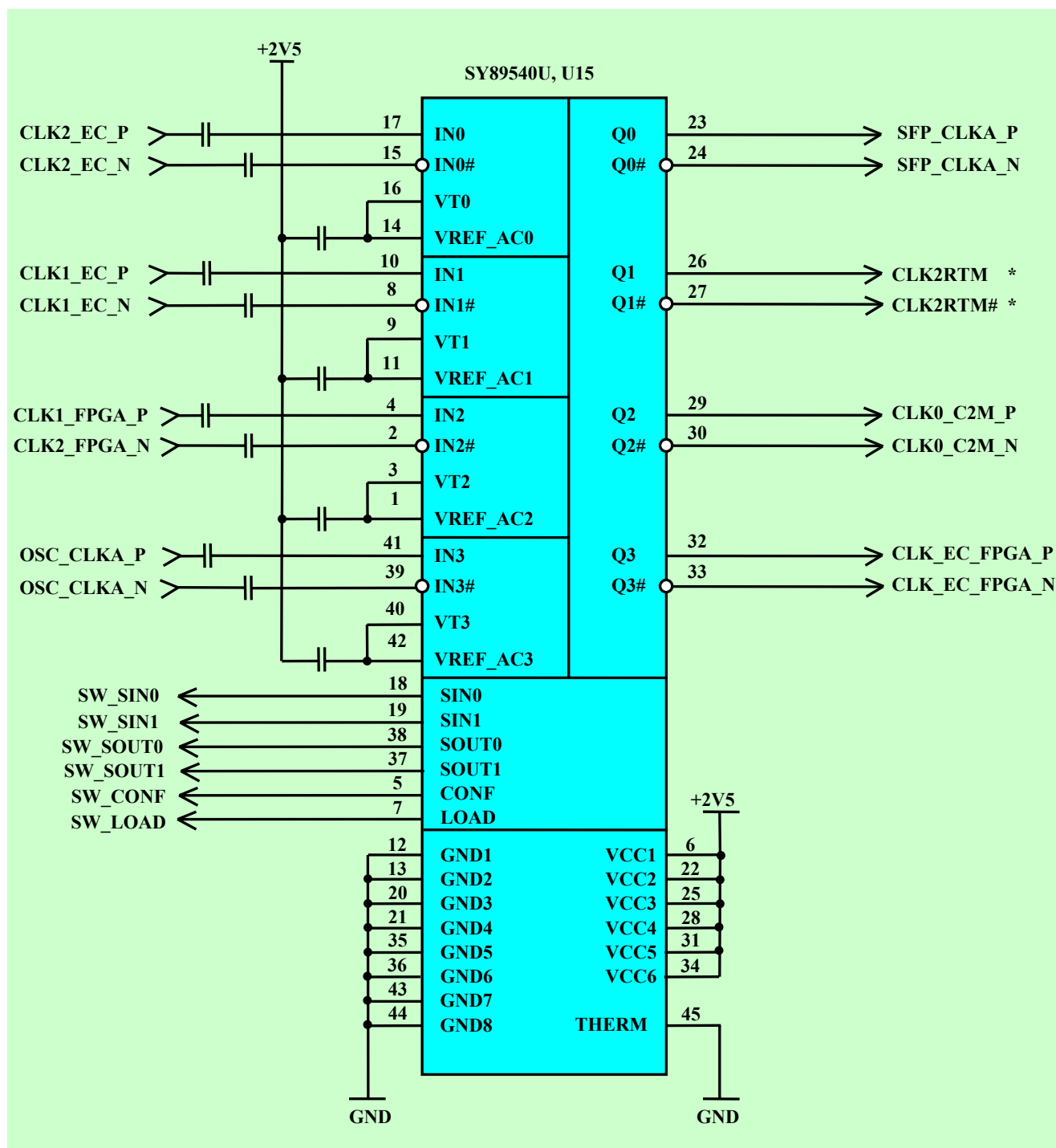


Figure 20 Low Jitter Clock Crosspoint Switch

* Signals **CLK2RTM** and **CLK2RTM#** corresponded to clock signals **CLK_EC_RTM_P** and **CLK_EC_RTM_N** in the electrical schematic of DAMC2-00.

CLK2_EC_P/N is **TCLKB** differential input signal from edge connector – J1

CLK1_EC_P/N is **TCLKA** differential input signal from edge connector – J1

CLK1_FPGA_P/N is differential input signal, which is provided by Virtex-5 – U17

OSC_CLKA_P/N is differential input signal, which is provided by second Si570 oscillator – Q1

SFP_CLKA_P/N is differential output signal, which is applied to SFP interfaces, bank 116 of FPGA

CLK2RTM and CLK2RTM# is differential output signal, which is applied to uRTM interface – J30

CLK_EC_FPGA_P/N is differential output signal, which is applied to Global Clock Input of FPGA, bank 3

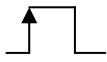
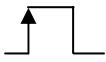
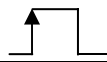
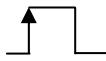
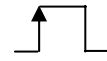
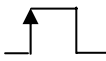

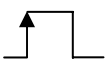
Pin assignments of SY89540U are shown in Table 15, Truth Table in Table16

Table 15 Pin Description of SY89540U

PIN NUMBER	PIN NAME	PIN FUNCTION
17, 15 10, 8 4, 2 41,39	IN0, IN0# IN1, IN1# IN2, IN2# IN3, IN3#	Differential Inputs: These input pairs are the differential signal inputs to the device. Inputs accept AC- or DC-coupled signals as small as 100mV. Each pin of pair internally terminates to a VT pin through 50Ω.
16, 9, 3, 40	VT0, VT1, VT2, VT3	Input Termination Center-Tap: Each side of the differential input pair terminates to a VT pin.
14, 11, 1, 42	VREF_AC0, VREF_AC1, VREF_AC2, VREF_AC3	Reference Voltage: These outputs biases to Vcc-1.2V. Each of VREF-AC pin has bypass low ESR capacitor – 100 nF
18, 19	SIN0, SIN1	These single-ended TTL/CMOS-compatible inputs address the data inputs, each of them is connected to a 25KΩ pull-up resistor.
38, 37	SOUT0, SOUT1	These single-ended TTL/CMOS-compatible inputs address the data outputs, each of them is connected to a 25KΩ pull-up resistor.
5, 7	CONF, LOAD	<p>These single-ended TTL/CMOS-compatible inputs control the transfer of the addresses to the internal multiplexers, each of them is connected to a 25KΩ pull-up resistor.</p> <p><u>Configuration Sequence</u></p> <ol style="list-style-type: none"> 1. Load: Loads configuration into buffer, while Configuration Buffer holds existing switch configuration. 2. Configuration: Loads new configuration into the Configuration Buffer and updates switch configuration.


PIN NUMBER	PIN NAME	PIN FUNCTION
		<u>Buffer Mode</u> The SY89540U defaults to buffer mode (IN to Q) if the load and configuration control signals are not exercised.
23, 24 26, 27 29, 30 32, 33	Q0, Q0# Q1, Q1# Q2, Q2# Q3, Q3#	Differential Outputs: These LVDS output pairs are the outputs of the device. Look on the truth table 15 below for details. Each output is designed to drive 350 mV into 100Ω across the pair.
6, 22, 25, 28, 31, 34	VCC	Positive power supply
12, 13, 20, 21, 35, 36, 43, 44	GND, Exposed pad	Ground. GND and EPad both are connected to the same ground.

Table 16 4:4 Buffer Truth Table

INPUT	SIN1	SIN0	SOUT1	SOUT0	LOAD	CONFIG.	OUTPUT
IN0	0	0	1	1		0	Q3
					0		
IN1	0	1	1	0		0	Q2
					0		
IN2	1	0	0	1		0	Q1
					0		
IN3	1	1	0	0		0	Q0
					0		

2.8.4 FPGA clocks

The FPGA has some of clock signals, which can be used for different applications and regimes. Most of them are connected to Global Clock I/O pins, Bank 3, FPGA. Besides, some clock signals,

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which were described above, are connected directly to GTP transceivers. List of FPGA clock signals, Bank 3:

- **RTM1_S24_P/N** – input/output differential clock, which is connected to J30 (C3, D3)
- **CLK0_M2C_P/N** – input differential clock , which is driven by FMC
- **GCLK_250M_P/N** - input differential clock , which is driven by PCI Express Jitter attenuator, Figure 6
- **CLK1_FPGA_P/N** - output differential signal, which is provided by Virtex-5
- **200MHz_P/N** - input differential clock, which is driven by LVDS oscillator – Q3. This clock is Reference CLKOCK for IODELAYCTRL
- **CLK_EC_FPGA_P/N** – input differential clock, which is driven by Crosspoint Switch – U15.

The clock signals for interface to DDR2 memory will be described below.

2.9 Memory

The DAMC2-00 board is populated with two chips 64MByte DDR2 SDRAM, a 32Mbit Platform Flash In-System Programmable Configuration PROM (ISP PROM) and a two-wire Serial EEPROM (8Kbit) with e-Keying info, which is connected to the MMC.

2.9.1 DDR2 SDRAM Interface

The FPGA on the DAMC2-00 is connected to Micron DDR2 SDRAM memory – MT47H32M16HR-25E (U22, U23). The 512Mb DDR2 SDRAM is a high-speed CMOS, dynamic random-access memory containing 536,870,912 bits. It is internally configured as a 4-bank DRAM. The DDR2 SDRAM uses a double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a $4n$ -prefetch architecture, with an interface designed to transfer two data words per clock cycle at the I/O balls. A single read or write access for the DDR2 SDRAM effectively consists of a single $4n$ -bit-wide, one-clock-cycle data transfer at the internal DRAM core and four corresponding n -bit-wide, one-half-clock-cycle data transfers at the I/O balls.

A bidirectional data strobe (DQS, DQS#) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR2 SDRAM during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and centre aligned with data for WRITEs. The x16 offering has two data strobes, one for the lower byte (LDQS, LDQS#) and one for the upper byte (UDQS, UDQS#).

The DDR2 SDRAM operates from a differential clock (CK and CK#). The crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS as well as to both edges of CK

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[12]. All inputs are compatible with the JEDEC standard for SSTL_18. All full drive-strength outputs are SSTL_18-compatible.

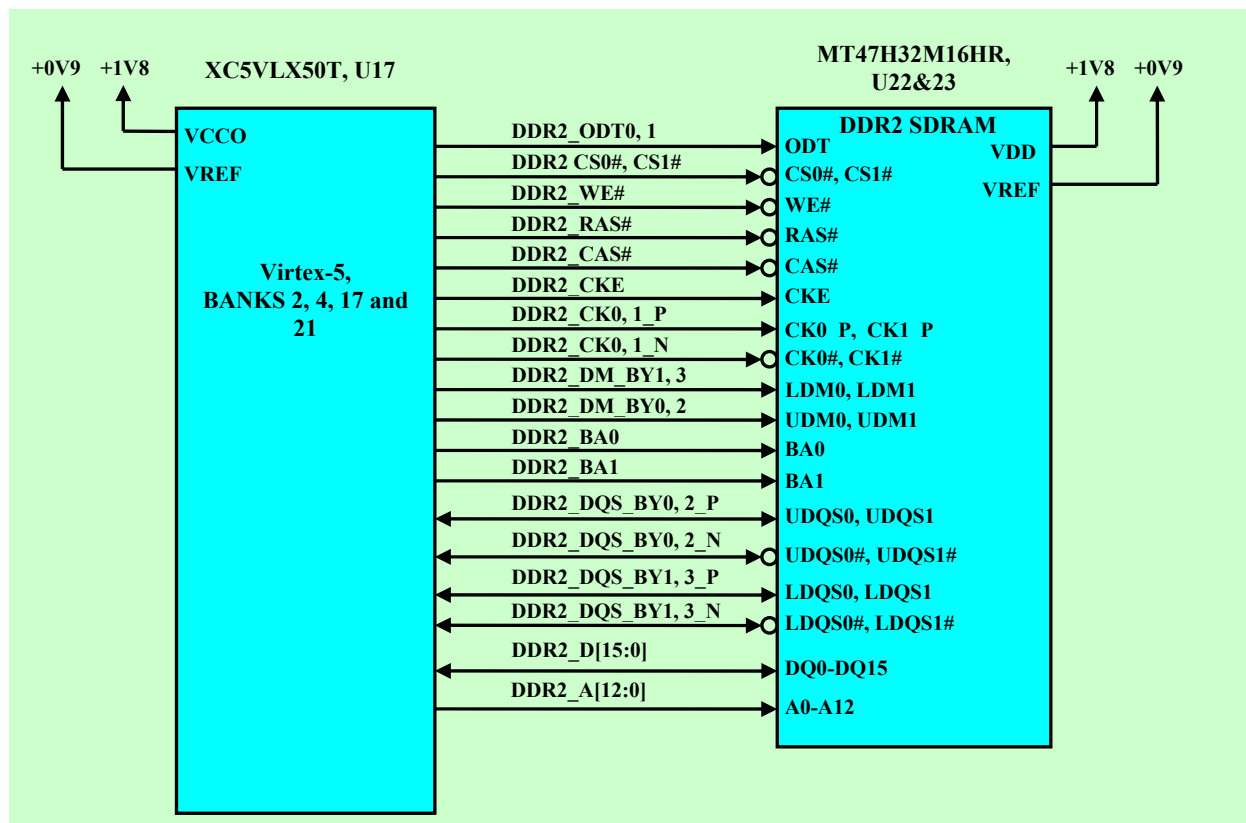


Figure 21 DDR2 SDRAM Interface

The DDR2 SDRAM devices are the next generation devices in the DDR SDRAM family. DDR2 SDRAM devices use the SSTL +1V8 I/O standard. The DDR2 SDRAM uses a source synchronous interface for transmission and reception of data. To capture this transmitted data using Virtex-5 FPGAs, either the strobe and/or data can be delayed [13]. Block diagram of interface FPGA to DDR2 SDRAM is shown on Figure 21.

2.9.2 Platform Flash Memory configuration interface

The Platform Flash series of in-system programmable configuration PROMs available in 1 to 32 Megabit (Mbit) densities, these PROMs provide an easy-to-use, cost-effective, and reprogrammable method for storing large Xilinx FPGA configuration bit streams. The Platform Flash PROM series includes both the 3.3V XCFxxS PROM and the 1.8V XCFxxP PROM [14]. The XCFxxP version includes 32-Mbit, 16-Mbit, and 8-Mbit PROMs that support Master Serial, Slave Serial, Master SelectMAP, and Slave SelectMAP FPGA configuration modes – Figure 22. In DAMC2-00 the Platform Flash memories – U35, XCF32PFSG48C, is used to program the FPGA in Master Serial configuration modes. A Platform Flash memory can hold minimum two

configuration images, which are selectable by MMC. The Platform Flash memory is programmed using Xilinx iMPACT software through the board's JTAG chain [15].

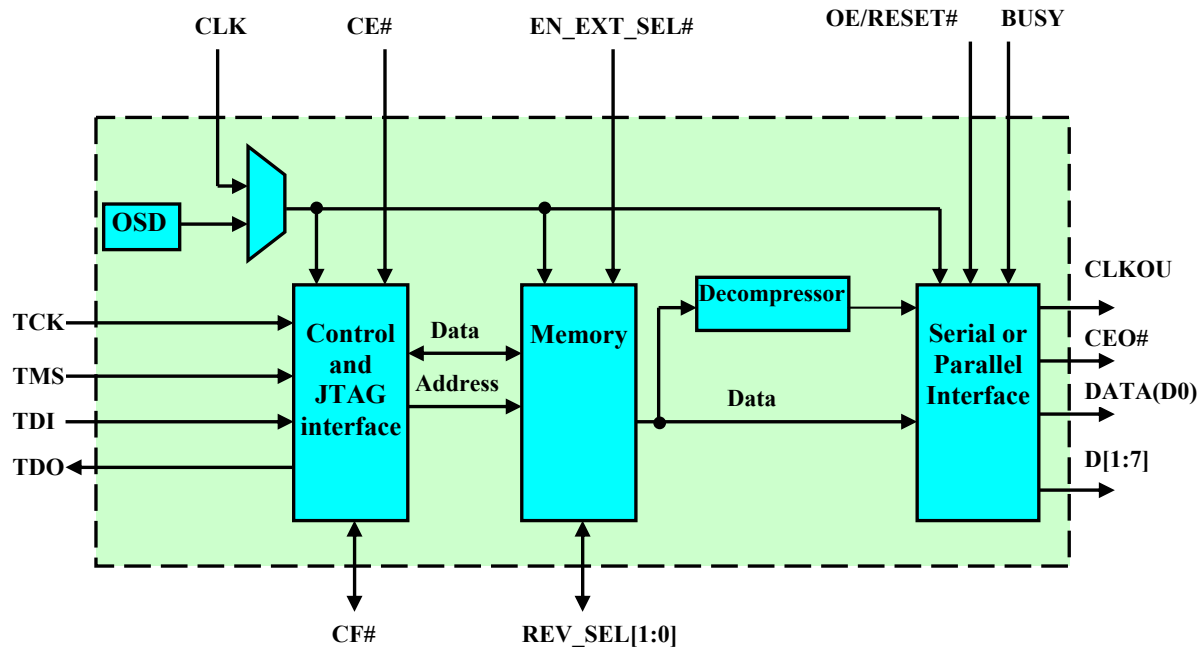


Figure 22 XCFxxP Platform Flash PROM Block Diagram

2.9.3 Serial EEPROM

The AT24C08AN (U24) provides 8192 bits of serial electrically erasable and programmable read-only memory (EEPROM) organized as 1024 words of 8 bits each. The device is used in many industrial and commercial applications where low power and low-voltage operations are essential. On the DAMC2-00 board E-Keying information are stored in this EEPROM.

E-Keying defines the process in which a Carrier determines if the Control and Fabric interfaces on a Module are compatible with the Carrier interconnects [1].

2.10 Module Management Controller

The DAMC2-00 includes a Module Management Controller (MMC) based on the ATMEL ATMEGA128L-8MU microcontroller [16], which interfaces to the IPMI (Intelligent Platform Management Interface) bus. It provides a Serial Peripheral Interface (SPI) interfaces and is IPMI compliant. The MMC monitors and controls the subsystems, and performs remote diagnostics for functionality of DAMC2-00, FMC and uRTM. The critical input/output signals of the MMC are connected to payload electronics via special buffer (U21) and switch (U18).

The MMC monitors the sensors of DAMC2-00, FMC and uRTM for system management events, such as over temperature, out-of-range voltages, revision, power consumption etc. All interfaces to the MMC are shown on Figure 23.

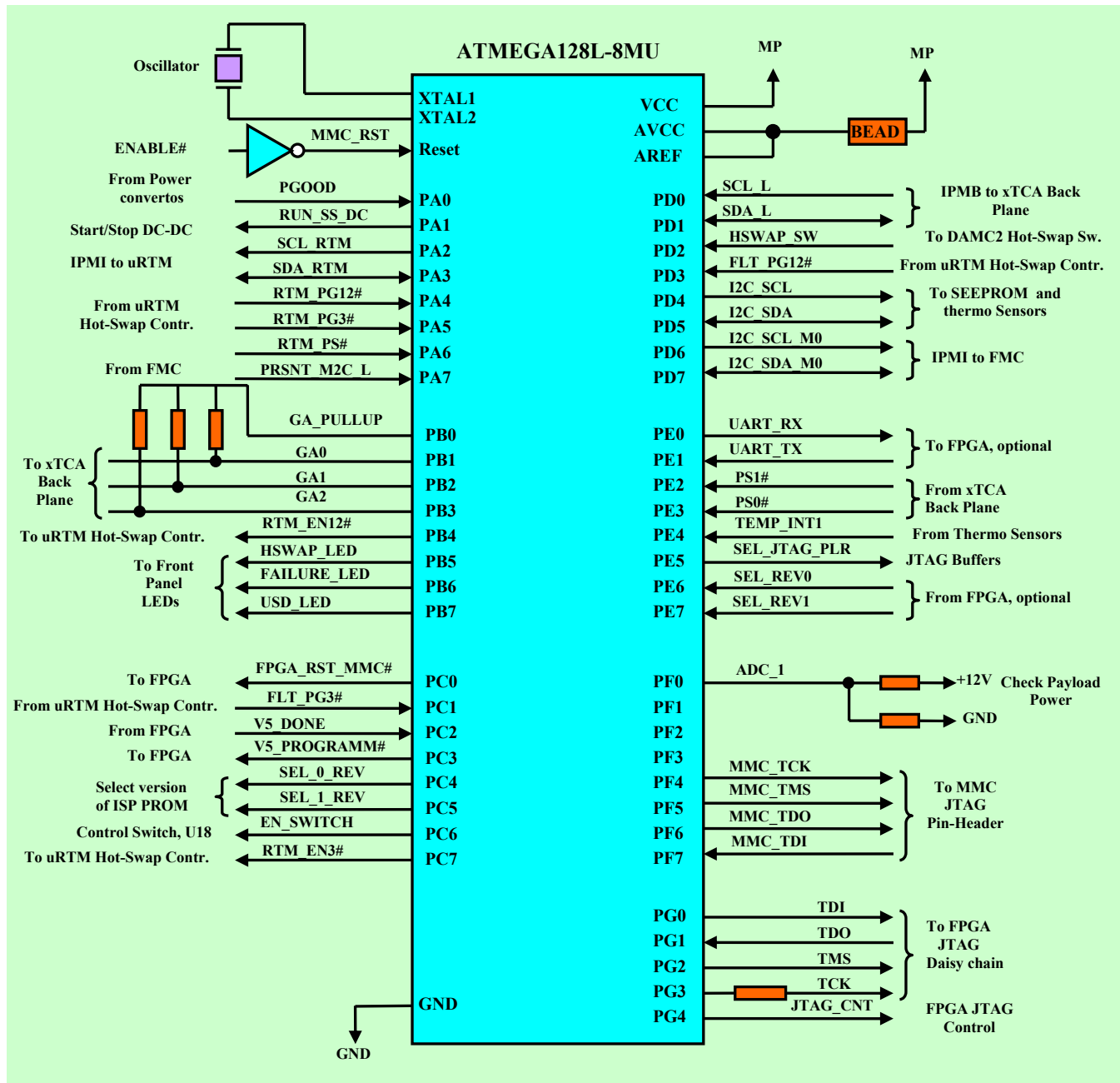



Figure 23 MMC

Additionally the JTAG Daisy Chain for the FPGA and PROM reconfiguration is managed, board temperatures are supervised and the board payload power is controlled and monitored.

2.10.1 Pin functionality of MMC

MMC (Atmega128L) has:

- Reset input - Reset
- Two pins for external clock oscillator – XTAL1 and XTAL2
- The 53 programmable I/O lines, which are divided in seven ports – A, B, C, D, E, F and G

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- The supply voltage pin the A/D Converter – AVCC
- The analog reference pin for the A/D Converter - AREF
- Power pins – GND and VCC.

Each MMC port consists of bi-directional and multifunctional pins. The functionality of different ports is shown below.

Port A:


- PA0 is an input signal PGOOD, which shows that all payload powers in DAMC2-00 are OK
- PA1 is an output signal RUN/SS, which run or shut down the payload power of the DAMC2-00
- PA2 and PA3 provide IPMI (I²C) interface to uRTM board
- PA4, PA5 are the inputs signals RTM_PG12# and RTM_PG3#, which are provided by uRTM Hot-Swap controller
- PA6 is an input signal RTM_PS#, which allow the DAMC2-00 to detect the presence of an uRTM board
- PA7 is an input signal PRSNT_M2C_L#, which allows the DAMC2-00 to determine whether an IO FMC Mezzanine board is present

Port B:

- PB0, PB1, PB2, PB3 are geographic address signals – GA_PULLUP, GA0, GA1, GA2. Below one can find more details about these signals.
- PB4 is an input signal RTM_EN12#, which control turn-on/off 12 Volts channel of uRTM Hot-Swap controller
- PB5 is an output signal - HSWAP_LED. The MMC activates this signal in case of a Hot Swap operation of DAMC2-00. If this signal is activated, then the front panel's blue LED(V19) is lit;
- PB6 is an output signal FAILURE_LED. MMC activates this signal if some failures happen and the front panel's red LED(V1) will be lit;
- PB7 is an output signal USD_LED – user defined LED. The MMC activates this signal for some special reasons, also FPGA can activate this signal by FUNC_LED signal. If this signal is activated, then front panel's green LED (V18) is lit.

Port C:

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- PC0 is an output signal FPGA_RST_MMC#, which allows to reset internal registers of the FPGA
- PC1 is an input FLT_PG3# signal, which comes from uRTM Hot-Swap Controller and asserted when 3Volts fault happens
- PC2 is an input signal V5_DONE, which indicates the completion of the FPGA configuration process
- PC3 is an output signal V5_PROGRAMM#, which allows reprogramming of the FPGA
- PC4, PC5 are output signals SEL0 and SEL1, which allow to select one of two FPGA configuration images in Platform Flash Memory
- PC6 is an output signal EN_SWITCH, which enables or disables the low-Voltage 10-bit FET bus switch – U18. The usage of this switch allows to disconnect control signals of MMC from rest parts of DAMC2-00, when payload power is not applied
- PC7 is an input signal RTM_EN3#, which control turn-on/off 3 Volts channel of uRTM Hot-Swap controller

Port D:

- PD0, PD1 are two bidirectional open-drain lines, Serial Clock (SCL_L) and Serial Data (SDA_L) for the xTCA IPMB (I²C) serial bus
- PD2 is an input signal from the Hot-Swap Switch – HAWAP_SW. The level of this signal proactively generate events (Module Handle Closed, Module Handle Opened and Quiesced) to enable the HUB to perform Hot Swap management for the DAMC2-00
- PD3 is an input FLT_PG12# signal, which comes from uRTM Hot-Swap Controller and asserted when 12Volts fault happens
- PD4, PD5 are two bidirectional open-drain lines, Serial Data (I2C_SCL) and Serial Clock (I2C_SDA) for the I²C serial bus, which connected to the digital thermometer (U7) and the FPGA thermo outputs, and to the SEEPRO (U24)
- PD6, PD7 are two bidirectional open-drain lines, Serial Clock (I2C_SCL_M0) and Serial Data (I2C_SDA_M0) for the FMC System Management (I²C) serial bus

Port E:

- PE0, PE1 are signals of the UART serial interface - UART_TX, UART_RX. MMC can to use this interface for the connection to the FPGA
- PE2 and PE3 are PS0# and PS1# signals, which detect the presence of an DAMC2-00 in the xTCA crate;

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- PE4 is an input interrupt signal - TEMP_INT1, which generated by thermo sensor (U7). If either measured temperature equals or exceeds the corresponding alarm threshold value, a TEMP_INT1 interrupt is asserted.
- PE5 is SEL_JTAG_PLR output signal, which allowed FPGA to load data in the Platform Flash via JTAG interface;
- PE6 and PE7 are the optional output/input signals – SEL_REV0 and SEL_REV1, which are connected to FPGA. **In next revision of DAMC2, these pins shall be connected to pins AE13 and AE13 of FPGA!**

Port F:

- PF0 is an input of internal ADC, which is used for control of Payload Power (+12V);
- PF1, PF2 and PF3 are not used in current version of DAMC2-00.
- PF4, PF5, PF6, PF7 are input/output of MMC JTAG interface - MMC_TCK, MMC_TMS, MMC_TDO and MMC_TDI, which are connected to the MMC_JTAG pin-header – J11.

Port G:

- PG0, PG1, PG2, PG3 are the input/output signals (TDI, TDO, TMS, and TCK) for the FPGA JTAG daisy chain. These signals are valid if the PG4 output is activated;
- PG4 is an output signal JTAG_CNT. When JTAG_CNT is at high level, the MMC becomes the JTAG controller for the FPGA JTAG daisy chain.

2.11 DAMC2-00 Hot-Plug, Module removal

An operator can initiate a module removal by opening the module handle, which deactivates the hot-swap switch. When this switch opens or closes it sends a request via the MMC to the HUB for a hot swap extraction or insertion. Its function and behaviour is defined by the PICMG AMC.0 specification [1]. The hot swap blue LED (HSWAP_LED) indicates the state of the module during extraction and insertion.

2.12 Module Management and xTCA Backplane interconnection

Figure 24 shows the management interconnects between an DAMC2-00 board and backplane of xTCA - IPMI. Note that active low signals are denoted with a trailing #. All logic levels are assumed +3V3 compatible unless otherwise noted.

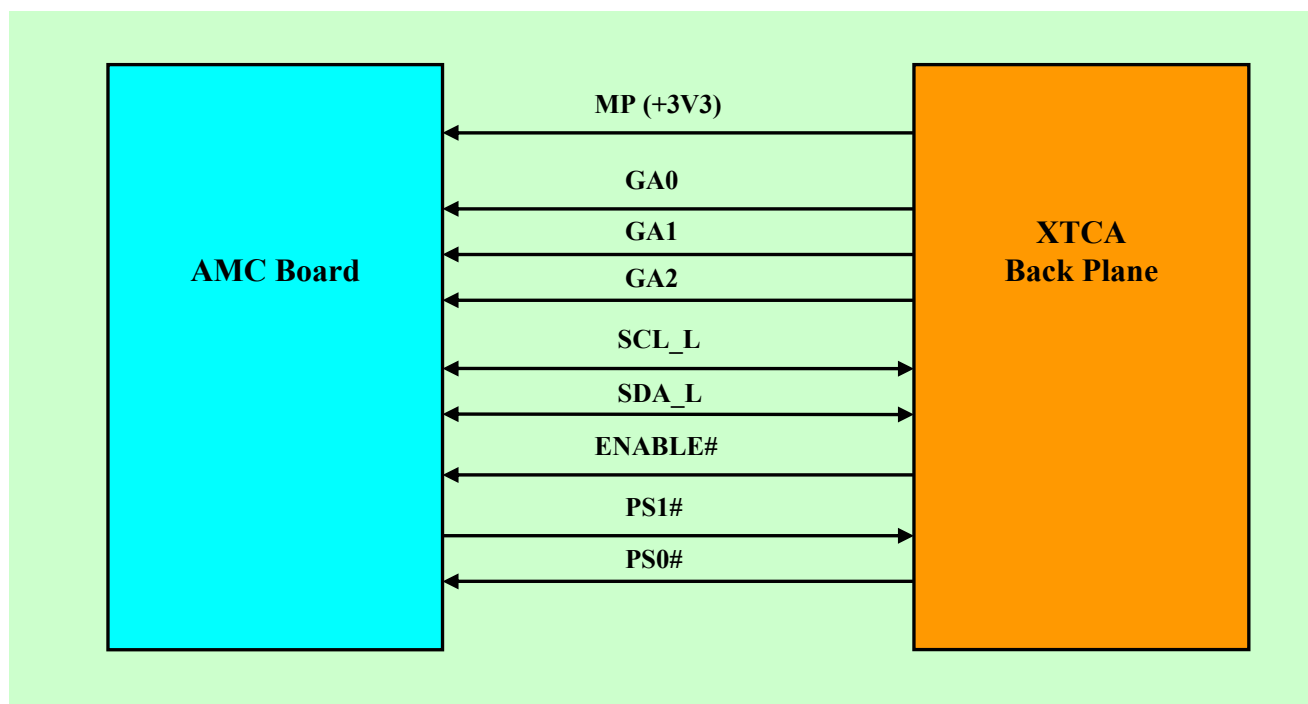



Figure 24 Management interconnection

2.12.1 PS0# and PS1#

The PS0# and PS1# pins are used to detect the presence of a DAMC2-00 in the xTCA crate. The PS0# and PS1# pins are last mate connections located on opposite ends of the edge connector – J1. These pins are used to compensate for any skew on the Module during insertion and provide confirmation that all pins of the AdvancedMC Edge Connector have mated (with a complementary role on extraction). The Backplane connects PS0# to Logic Ground and pulls up PS1# to the 3.3V Management Power. The DAMC2-00 board connects PS1# to PS0# through a diode, providing a low voltage drop path from PS1# to PS0#. The Backplane (HUB) can detect the presence of a DAMC2-00 by an active PS1# signal. The DAMC2-00 can determine the insertion into a crate by the HUB's feedback of PS1# on ENABLE# as well as by a current flowing through the PS0# - PS1# connection.

2.12.2 Enable#

The ENABLE# pin is an active low input, which is pulled up on the DAMC2-00 to Management Power (MP). This signal is inverted on the board to create a RESET# signal toward the MMC. The negated state of this ENABLE# indicates to the MMC that the board is fully inserted and valid states exist on all inputs of the Module. The MMC is not allowed to read the GA inputs or use the IPMB-L while ENABLE# is inactive.

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2.12.3 IPMB_L

The Inter-Integrated Circuit bus (I2C) is a multi-master, 2-wire serial bus used as the basis for current IPMBs. IPMB_L is made up of clock (SCL_L) and data (SDA_L) signals.

Some of the functions available on the DAMC2-00 board through the IPMB_L interface include:

- Monitoring of the FPGA and board temperatures
- Monitoring of the payload voltage rails on the DAMC2-00, uRTM and FMC
- Remote reset and shutdown of the board
- Monitoring of the ejector switches for the hot swap functionality
- Monitoring and event recording of critical errors
- Board power up and power down

2.12.4 Geographical address lines

Three Geographic Address (GA) pins are used to assign the address of a DAMC2-00 on IPMB-L. Each of the GA pins can encode three different levels; they can be connected to Logic Ground, to Management Power, or left unconnected on the Backplane to define the Geographic Address of the DAMC2-00. This scheme requires that the board be able to distinguish among three states. The state of the GA lines on the DAMC2-00 can be determined if each of the GA lines is connected to a MMC output (GA_PULLUP) through a resistor. The MMC drives GA_PULLUP low and reads the GA lines. The MMC then drives GA_PULLUP high and reads the GA lines. Any lines that change state between the two reads indicate an unconnected (U) pin.

2.12.5 Management Power (MP)

The Module Management Power (MP) powers the DAMC2-00 management subsystem. It is ensured via requirements to the Backplane (HUB) that Payload Power is only available the board if Management Power is available.

2.13 uRTM Management Hardware

In corresponding to xTCA specification, the DAMC2-00 support an uRTM interface via Zone 3 connectors [11]. The uRTM is managed by the MMC of DAMC2-00 board. In order to detect a mismatched uRTM, a standardized management interface between the DAMC2-00 and the uRTM is implemented.

The management interface between the DAMC2-00 and the uRTM includes the following:

- Ground
- uRTM-PS
- Management Power

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- I²C bus
- Payload power

Figure 25 shows a block diagram of the DAMC2-00 and uRTM management circuitry

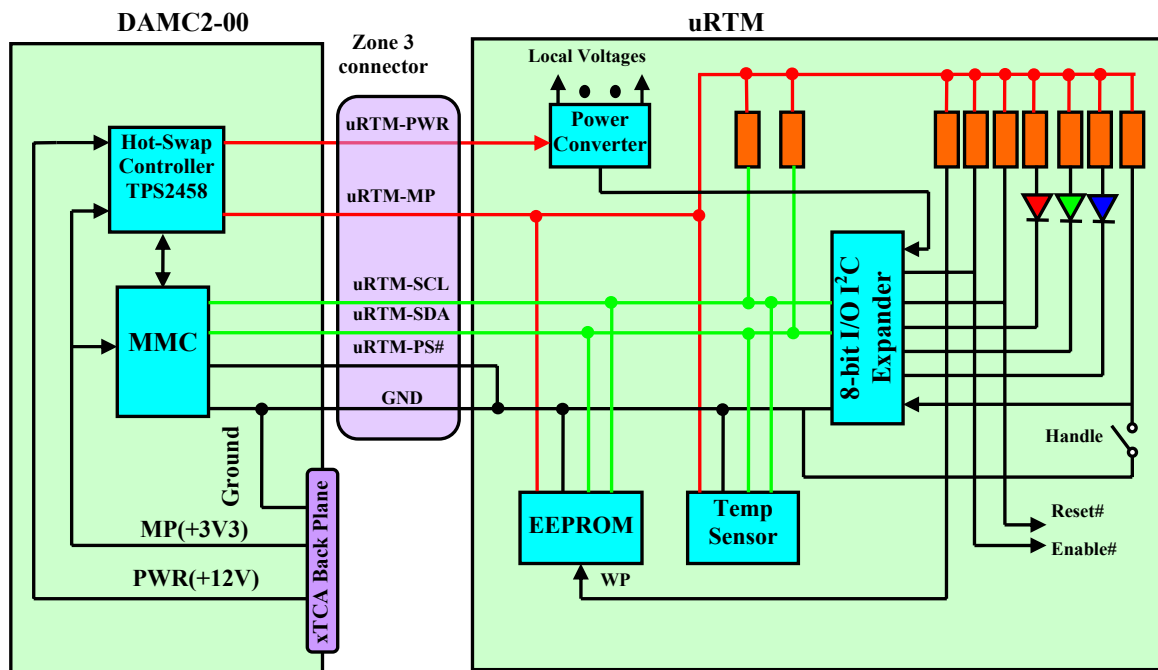


Figure 25 uRTM management

The Hot-swap controller, which is controlled by MMC, provides proper of power sequence to uRTM.

2.13.1 uRTM Hot-Swap Controller

The DAMC2-00 provides management power for uRTM by TPS2458 - Hot-Swap Controller with Load Current Monitor for AdvancedMC™. The TPS2458 is an extremely flexible solution that protects both the power supply and the load by limiting the maximum current into the load, shutting off in case of a fault. If a severe fault occurs, the current shuts off immediately. The 3.3 Volt management channel is internal and requires only one external resistor for load monitoring and one external capacitor to set fault time. To comply with the AdvancedMC™ requirements, the 12 Volt output is disabled unless the 3.3 Volt Power Good signal is asserted. Load current monitors are provided for both the 12 Volt and 3.3 Volt channels. Status outputs include Power Good and Fault indicators for each channel. Figure 26 shows the implementation of TPS2458 in DAMC2-00.

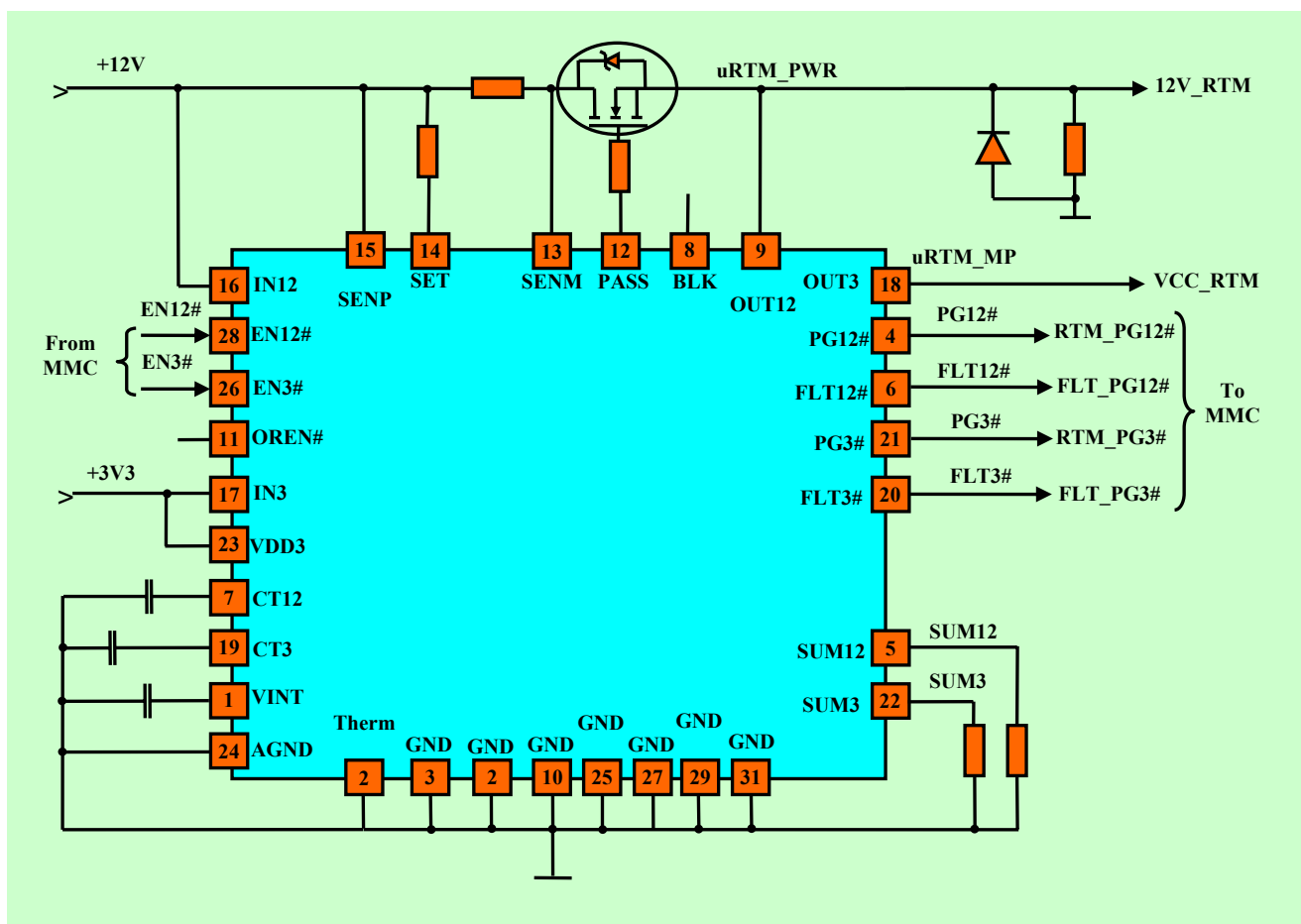


Figure 26 The usage of TPS2458

The TPS2458 circuitry draws power from an internal bus fed by a preregulator. A capacitor attached to the VINT pin provides decoupling and output filtering for this preregulator. It can draw power from either of two inputs (IN12 or IN3) or from either of the two outputs (OUT12 or OUT3). This feature allows the internal circuitry to function regardless of which channels receive power, or from what source. The external FET drive pins (PASS,) is held low during startup to ensure that the 12-V channel remains off. The internal 3.3-V channel is also held off. When the voltage on the internal VINT rail exceeds approximately 1 V, the power-on reset circuit initializes the TPS2458 [17]. The Table 17 shows pins function of TPS2458.

Table 17 The TPS2458 Terminal Function

NAME	NO.	I/O	FUNCTION DESCRIPTION
AGND	24	-	Analog ground. Ground pin for the analog circuitry inside. Bypass capacitor connection point for internal supply the TPS2458
BLK	8	O	12V blocking transistor gate drive.

NAME	NO.	I/O	FUNCTION DESCRIPTION
CT12	7	I/O	12V fault timing capacitor. A capacitor from CT12 to GND sets the time the channel can remain in current limit before it shuts down and declares a fault. Current limit causes this pin to source 10 uA into external capacitor (CT). When V_{CT12} reaches 1.35 Volt, the TPS2458 shuts the channel off by pulling the FET gate low and declares an overcurrent fault by pulling the FLT12# pin low
CT3	19	I/O	3-V fault timing capacitor. A capacitor from CT3 to GND sets the time the channel can remain in current limit before it shuts down and declares a fault. Current limit causes this pin to source 10 uA into external capacitor (CT). When V_{CT3} reaches 1.35 Volt, the TPS2458 shuts the channel off by pulling the FET gate low and declares an overcurrent fault by pulling the FLT3# pin low.
EN12#	28	I	12V enable (active low). Pulling this pin high (or allowing it to float high) turns off the 12V channel by pulling the both BLK and PASS low. An internal 200K Ω resistor pulls this pin up to VINT when disconnected.
EN3#	26	I	3V enable (active low). Pulling this pin high (or allowing it to float high) turns off the 3V channel by pulling the gate of the internal pass FET to GND. An internal 200k Ω resistor pulls this pin up to VINT when disconnected
FLT12#	6	O	12V fault output (active low) Open-drain output indicating that channel 12 has remained in current limit long enough to time out the fault timer and shut the channel down. Asserted when 12V fault timer runs out.
FLT3#	20	O	3V fault output (active low) Open-drain output indicating that channel 3 has remained in current limit long enough to time out the fault timer and shut the channel down. Asserted when 3V fault timer runs out.
GND	2, 3, 10, 25, 27, 29, 31	-	Ground connections
IN3	17	I	3V input. Supply pin for the 3V channel internal pass FET.
IN12	16	I	12V input. Supply pin for the 12V channel internal circuitry
OREN#	11	I	12V blocking transistor enable (active low). Pulling this pin low allows the 12V channel ORing function to operate normally. Pulling this pin high (or allowing it to float high) disables the 12V ORing function by pulling the BLK pin low. An internal 200-k Ω resistor pulls this pin up to VINT when disconnected.
OUT12	9	I/O	12V output. Senses the output voltage of the 12V channel.
OUT3	18	I/O	3V output. Output of the 3V channel internal pass FET.

NAME	NO.	I/O	FUNCTION DESCRIPTION
PASS	12	O	12V pass transistor gate drive. This pin sources 30uA to turn the FET on. An internal clamp prevents this pin from rising more than 14.5V above IN12. PASS connect to the FET gate with 100 Ω
PG12#	4	O	12V power good open-drain output, active low, asserts when $V_{OUT12} > PG$ threshold (10.5V).
PG3#	21	O	3V power good open-drain output, active low, asserts when $V_{OUT3} > PG$ threshold (2.85V).
SENM	13	I	12-V current limit sense. Senses the voltage on the low side of the 12-V channel current sense resistor.
SENP	15	I	12-V input sense. Senses the voltage on the high side of the 12-V channel current sense resistor.
SET	14	I	12-V current limit set. A resistor connected from this pin to SENP sets the current limit level in conjunction with SET 14 I the current sense resistor and the resistor connected to the SUM12 pin, as described in 12-V thresholds, setting current limit and fast overcurrent trip section.
SUM12	5	I/O	12 V summing node. A resistor connected from this pin to ground forms part of the channel x current limit. As the current delivered to the load increases, so does the voltage on this pin. When the voltage on this pin reaches 675 mV, the current limit amplifier acts to prevent the current from further increasing.
SUM3	22	I/O	3V summing node. A resistor connected from this pin to ground forms part of the channel x current limit. As the current delivered to the load increases, so does the voltage on this pin. When the voltage on this pin reaches 675 mV, the current limit amplifier acts to prevent the current from further increasing.
VDD3	23	I	3-V charge pump input
VINT	1	I/O	Bypass capacitor connection point for internal supply. This pin connects to the internal 2.35-V rail. A 0.1-mF capacitor must be connected from this pin to ground.

2.14 FPGA&FMC JTAG Daisy Chain

Flexible JTAG Interface (Figure 27) to reconfigure the PROM, FPGA and FMC in several ways:

- Via the DAMC2-00 Backplane JTAG Interface
- Via PCI Express and the JTAG ACE Player
- Via IPMI / I2C using the MMC as JTAG controller

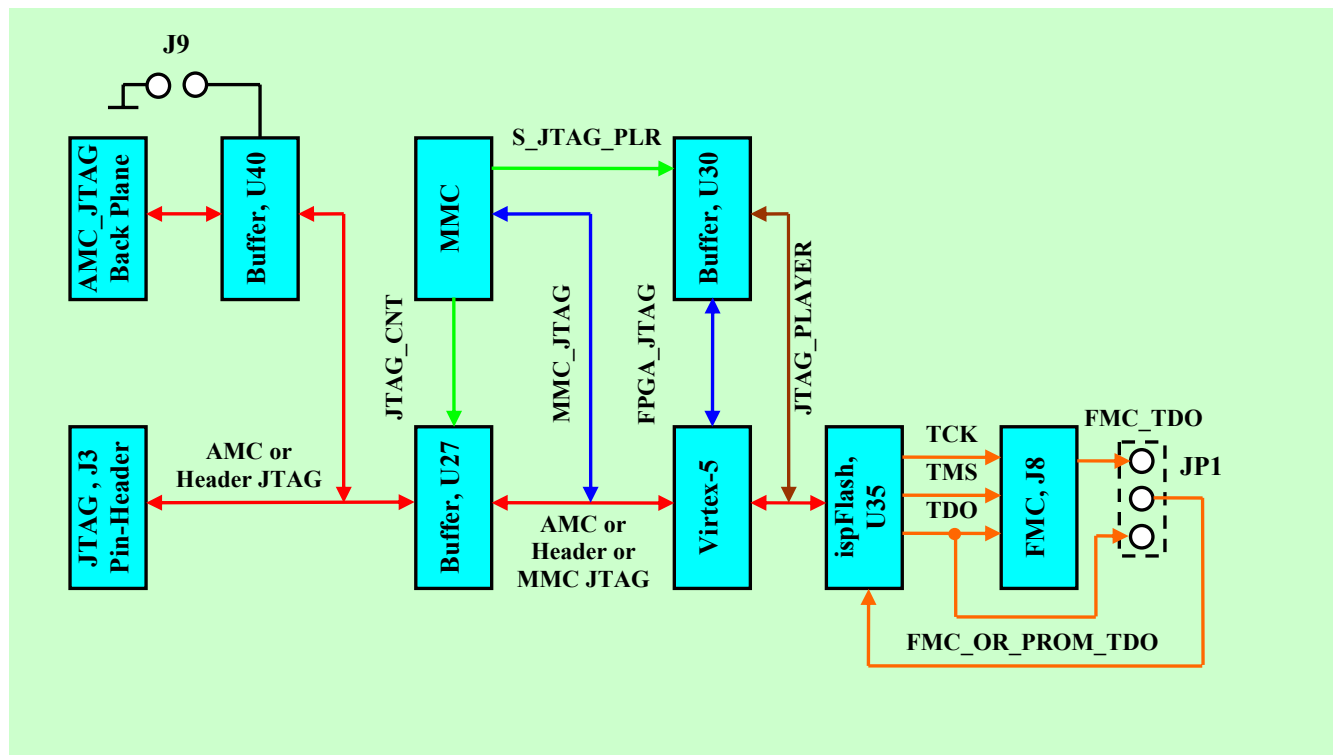


Figure 27 DAMC2-00 JATG daisy chain

The JTAG daisy chain can be controlled by signals from the uTCA edge connector or from the on-board J3 JTAG connector. The on-board FPGA JTAG header is used for configuration of FPGA, for loading of configuration PROM and for debugging in stand-alone mode.

In addition, the MMC can also generate JTAG sequences, with blocking signals from J3 and the edge connector.

At last, FPGA JTAG ACE (Advanced Configuration Environment) [18] Player can be implemented in FPGA. This software gives users great flexibility in creating in-system programming (ISP) solutions. The users can to revise existing designs, package the new bitstream programming files with the provided software utilities, and update the Platform PROM through the JTAG interface using the Embedded JTAG ACE Player.

The pin-header J9 defines source of basic JTAG signals: Backplane of xTCA or on-board pin-header. The jumper JP1 is used for selection of last element in JTAG Daisy Chain: when FMC Mezzanine Board is not installed on DAMC2-00, then JP1 should be installed so that TDO output of ispFlash will be connected to JTAG_TDO.

2.15 User LEDs

The 13 discrete LEDS are installed on the board and are used to display the status of the internal logic and powers. These LEDs are attached as shown in table 18.

Table 18 USER LEDs

LED REFERENCE	USAGE	COLOUR	REMARKS
V2	Select boot Version of FPGA	Green	-
V3	Present Management Power +3V3	Green	-
V4	2V5 Power is OK	Green	-
V5	Present Payload Power _12V	Green	-
V6	MGT Powers are OK	Green	-
V7	3V3 Power is OK	Green	-
V8	1V8 Power is OK	Green	-
V9	1V Power is OK	Green	-
V10	DONE FPGA	Green	-
V11	Heart Beat FPGA	Green	FPGA is alive
V14	RED-YELLOW-GREEN User define LEDs	RED, YELLOW, GREEN	Installed on the Front Panel
V15	RTM present	Green	-
V17	MMC RESET	RED	-

Besides, the three LEDs have a fixing assignment and are controlled by MMC:

- V1 – Failure **Red** LED;
- V18 – USD_LED **Green** LED;
- V19 – Hot-Swap **Blue** LED

3 Power consideration

The DAMC2-00 requires two power sources, the module management power for the MMC (nominal: +3V3V DC), and a single payload power (nominal: +12V DC) for the module components. The power supply circuitries on the board - DC-DC converters and LDO regulators, produce VCC0V9_VREF, VCC0V9_VTT1, +1V0, +1V2, +1V8, +2V5, REF_2V5 and +3V3 voltages. The +3V3 and +2V5 power rails and +1V0 FPGA core power are delivered by Linear Technology DC-DC uModules (LTM4600) – Figure 28. The system monitor of FPGA needs reference power – REF_2V5, which is made by REF3025, low voltage dropout voltage reference [19].

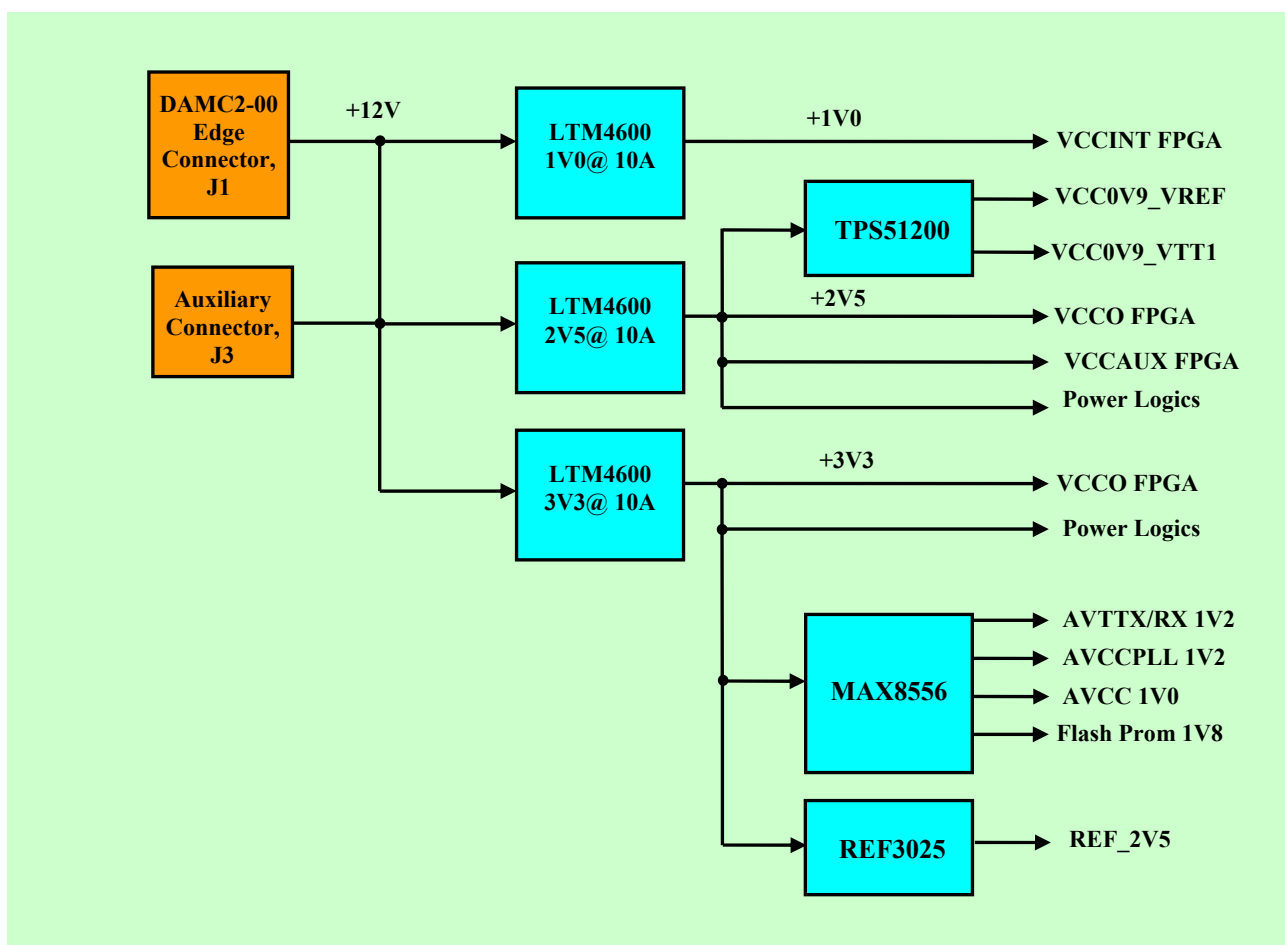


Figure 28 Payload Power

The two DDR2 SDRAM chips need two reference and termination powers - VCC0V9_VREF, VCC0V9_VTT1, which are generated by TPS51200, sink/source DDR Termination Regulator [20]. The +1V8 power for the Platform Flash memory is generated by MAX8556ETE low-dropout linear regulators. The GTP power supply – 1V0 and 1V2, are created by MAX8556ETE also. The GTP power supplies and +1V8 power are sourced from the +3V3 power rail. In normal operation, DAMC2-00 power is provided through the AMC edge connector. The J3 Auxiliary Power

Connector allows running the DAMC2-00 without xTCA crate during debug and tests. The pinout of Auxiliary Power Connector is shown in Table 19.

Table 19 Pinout of Auxiliary Power Connector - J3

PIN'S NUMBER	POWER&CONTROL	PIN'S NUMBER	POWER&CONTROL
4	GND	1	GND
5	Management Power,+3V3	2	MMC_Enable#
6	Payload Power, +12V	3	Payload Power, +12V

Do not apply +12 Volts to Auxiliary Power Connector without or before applying Power Management (3V3) to the DAMC2-00. Do not use this connector when the card is connected to a Backplane via the AMC edge connector.

3.1.1 DC-DC uModule

The DAMC2-00 has three LTM4600 DC-DC uModules, which have next main features [21]:

- Complete Switch Mode Power Supply
- Wide Input Voltage Range: 4.5V to 20V
- 10A DC, 14A Peak Output Current
- 0.6V to 5V Output Voltage
- 1.5% Output Voltage Regulation
- Ultra fast Transient Response
- Current Mode Control
- Pb-Free (e4) RoHS Compliant Package with Gold-Pad Finish
- Up to 92% Efficiency
- Programmable Soft-Start
- Output Over voltage Protection
- Optional Short-Circuit Shutdown Timer
- Small Footprint, Low Profile (15mm x 15mm x 2.8mm) Surface Mount LGA Package.

3.1.2 GTP voltage Regulators

The DAMC2-00 board provides point-of-load regulation for the GTP supplies with three high precision, low dropout linear regulators from MAXIM. The MAX8556ETE LDO regulators

provide up to four amps of current. The ultra-low input voltage requirement minimizes the voltage drop across the regulator saving the added cost of thermal solutions in most applications. The following Figure 29 shows a high-level block diagram of the GTP power supplies.

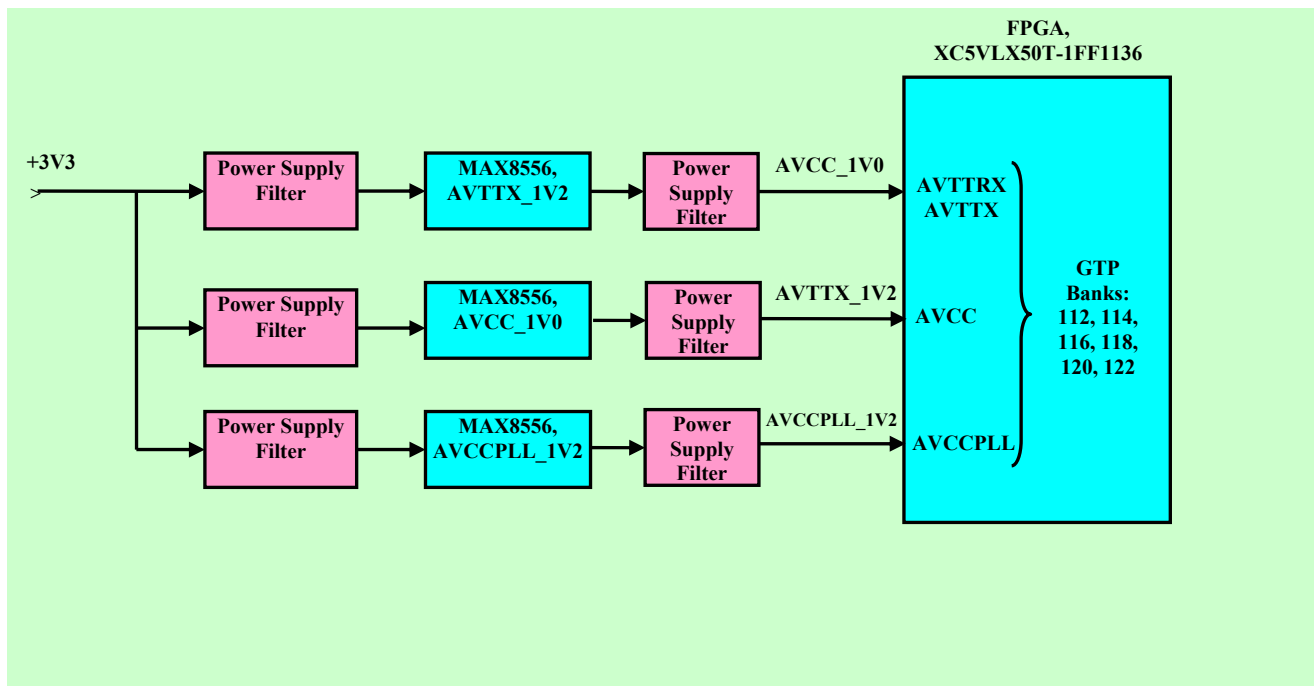



Figure 29 GTP Powers

3.1.3 MAX8556ETE

The MAX8556ETE Ultra-Low-input-Voltage low-dropout linear regulators operate from input voltages as low as 1.425V and are able to deliver up to 4A of continuous output current with a typical dropout voltage of only 100mV. The output voltage is adjustable from 0.5V to $V_{IN} - 0.2V$. Main features of the MAX8556ETE [22] are:

- 1.425V to 3.6V Input Voltage Range;
- Guaranteed 4A Output Current;
- **±1% Output Accuracy Over Load/Line/Temperature;**
- **100mV Dropout at 4A Load (typ);**
- Built-in soft-start;
- 800µA (typ) Operating Supply Current;
- 150µA (max) Shutdown Supply Current;
- Short-Circuit Current Foldback Protection;
- Thermal-Overload Protection;
- ±10% Power-OK;

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- Fast Transient Response;
- 16-Pin Thin QFN 5mm x 5mm Package.

4 PCB

This chapter provides information about the PCB design of the DAMC2-00 board. The physical dimensions of the raw PCB are 149mm x 181mm. This 14-layer board has eight signal layers, 3 GND layers and 3 power planes and uses FR4 material.

4.1 Printed Circuit Board (PCB) of DAMC2-00

The PCB consists of 14 physical layers: eight signal layers, three GND layers and three split power planes and uses FR4 material. The Plane Assignments are defined in table 20.

Table 20 Plane Assignment

LAYER	LAYER DESCRIPTION	PLANE TYPE
1	Signal_Top, and Power Area Fills: +1V, +1V8, +2V5, +3V3, +12V, 12V_RTM, Rsence, V_OSC and VCC0V9_VTT1, GND	Positive
2	Plane_1: GND	Positive
3	Signal_2 and Power Area Fills: VccT0, VccT1, VccT2, VccT3	Positive
4	Split Power Plane_2: +1V, +2V5, +3V3, VCC_RTM	Positive
5	Signal_3	Positive
6	Plane_3: GND	Positive
7	Signal_4	Positive
8	Plane_4: GND	Positive
9	Signal_5	Positive
10	Split Power Plane_5: +2V5, +3V3, +12V, AVCCPLL_1V2, AVTTX_1V2, VCC0V9_VREF	Positive
11	Signal_6	Positive
12	Signal_7	Positive
13	Split Power Plane_6: +1V8, +3V3, +12V, AVCCPLL_1V2, AVCC_1V0, AVTTX_1V2, VCC,	Positive

LAYER	LAYER DESCRIPTION	PLANE TYPE
	V_OSC1, GND	
14	Signal_Bottom, Split Power Plane: +3V3, +12V, AVCCPLL_1V2, AVTTX_1V2, AVCC_1V0, VCC0V9_VTT1, VCC_SCLK, GND, GND_SCLK	Positive

4.2 Stack-up PCB of DAMC2-00

Figure 30 shows a stack-up diagram of the DAMC2-00 PCB

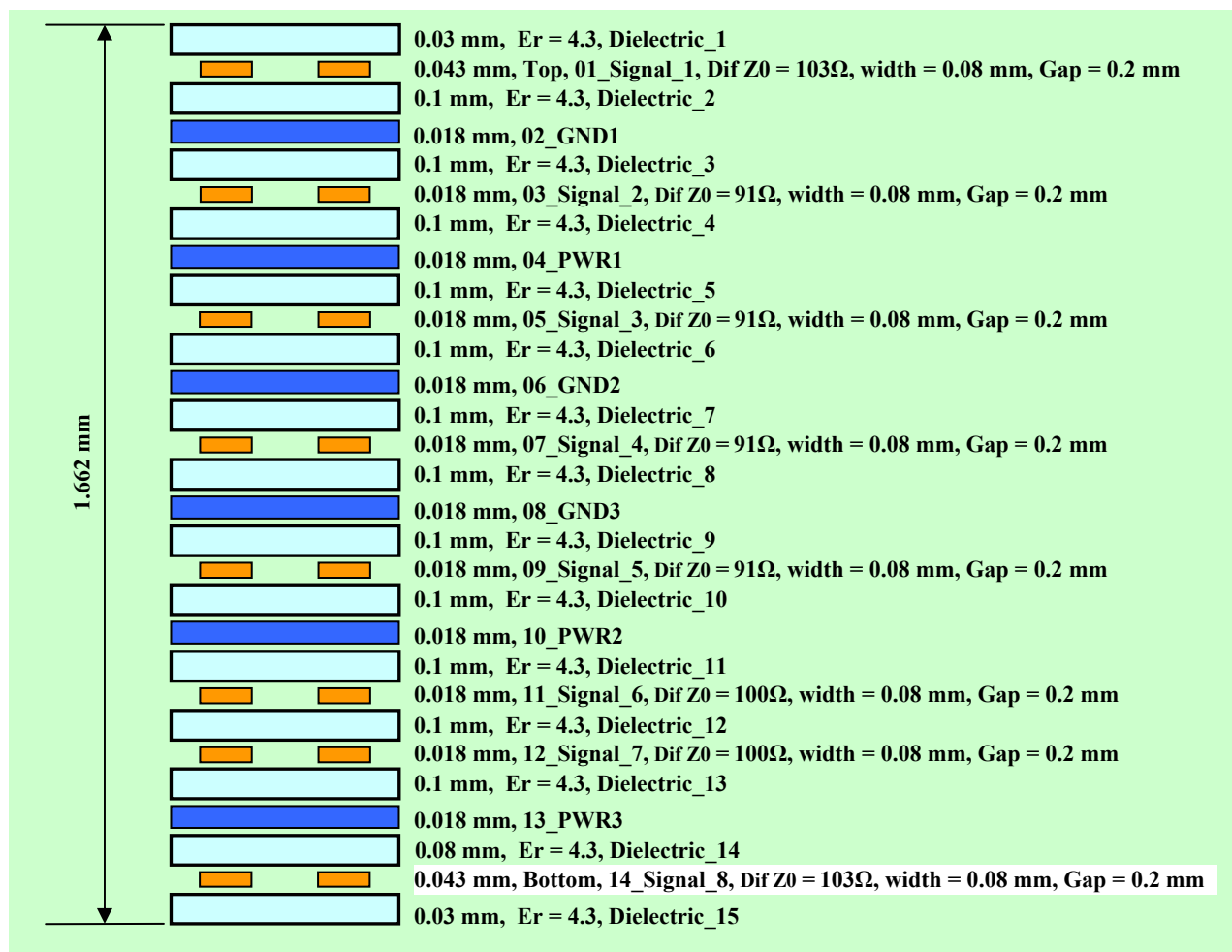


Figure 30 DAMC2-00 PCB Stack-up

4.3 Routing GTP Traces

The routing of high-speed GTP and LVDS traces was big challenge of DAMC2-00 PCB design [23]. The follow routing and placement guidelines were implemented:

1. The high-speed components and FPGA were placed on the unrouted board first.

- The high-speed clock and high-speed differential pairs were routed with minimum trace lengths. Maintain maximum possible distance between high-speed clocks/periodic signals to high-speed differential pairs and any connector leaving the PCB (such as, I/O connectors, control and signal headers, or power connectors).
- The route of high-speed differential signals using a minimum of vias and corners. This reduces signal reflections and impedance changes.
- When it becomes necessary to turn 90°, there was used two 45° turns or an arc instead of making a single 90° turn. This reduces reflections on the signal by minimizing impedance discontinuities.
- The high-speed differential traces do not route under crystals, oscillators, clock synthesizers or ICs that use and/or duplicate clocks.
- There are no stubs of high-speed signals, as stubs will cause signal reflections and affect signal quality.
- All traces were routed over continuous planes (VCC or GND).
- When a high-speed differential signal changes layers, the ground stitching vias should be placed close to the signal vias.


5 Virtex-5 Decoupling Capacitors

A simple PCB-decoupling network for each Virtex-5 LXT family device is listed in Table 21. Many of the devices require very few PCB ceramic capacitors because high frequency ceramic capacitors are already present inside the device package (mounted on the substrate) [24]. Thus, fewer PCB decoupling capacitors are needed in Virtex-5 devices than in previous device families.

Table 21 Required PCB Capacitor Quantities per Virtex-5, LXT devices

PACKAGE	DEVICE	VCCINT			VCCAUX			VCCO (PER I/O BANK)			TOTAL
		330 UF	2.2 UF	0.22 UF	33 UF	2.2 UF	0.22 UF	47 UF	2.2 UF	0.22 UF	
FF1136	XC5VLX50T	1	-	-	1	-	-	-	-	-	2
FF1136	XC5VLX85T*	2	-	-	1	-	-	-	-	-	3
FF1136	XC5VLX110T*	2	-	-	2	-	-	-	-	-	4
FF1136	XC5VLX155T*	3	-	-	2	-	-	-	-	-	5

* - pin compatible devices, which can to replace the **XC5VLX50T**

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