

NOTES

1. RESISTANCE VALUE IN Ohms
2. REFERENCE DESIGNATOR USED:
- A. INTEGRATED CIRCUITS: U1 - U51

B. CERAMIC CAPS: C0 - C3, C6 - C9, C11, C12, C15,C16, C21, C22, C24, C27 - C44, C46 - C61, C63 - C68, C70 - C92, C94 - C96, C98 - C110, C112 - C114, C119 - C122, C125 - C132, C135 - C150, C153 - C164, C167, C168, C170 - C181, C184 - C189, C191 - C195, C197 - C230, C232 - C262, C264 - C270, C272 - C277.

C. CAPACITORS ARRAY: C13, C14, C23, C62, C69, C 93, C117, C118, C165, C166, C169, C182, C183, C190, C196, C263, C271

D. SMD ALUMINUM ELECTROLITIC CAPACITOR: C20.

E. LOW ESL&ESR TANTALUM CAPS: C4, C5, C10, C17 - C19, C25, C26, C45, C97, C111, C115, C116, C123, C124, C133, C134, C151, C152, C231.

F. SMD RESISTORS: R1 - R49, R51 - R54, R57, R58, R60 - R67, R69, R70, R72 - R89, R91 - R101, R103, R104, R106 - R110, R112 - R115, R117 - R121, R123 - R164, R169 - R180.

G. ARRAY CHIP RESISTORS: R50, R55, R56, R59, R68, R71, R90, R102, R105, R111, R116, R122, R165 - R168.

H. CONNECTORS/HEADERS: J1 - J31, JP1.

I. OSCILLATORS, RESONATOR: Q1 - Q4.

J. EMI FILTERS (BEADS&INDUCTORS): L1 - L52.

K. SWITCH (PUSHBUTTON, MICROSWITCH): SW1, SW2.

L. SMD LEDs, FRONT PANEL LEDS: V1 - V11, V14, V15, V17, V18, V19.

M. SMD DIODE AND TRANSISTOR: V12, V13, V16

N. TEST POINTS: TP1, TP2

O. SFP CAGE AND ESD STRIP: X1, X2
3. BOARD PROPERTIES:
- A. FR4 BOARD MATERIAL

B. MINIMUM TRACE WIDTH/SPACING: 0.08/0.1 MM

C. MINIMUM VIA SIZE: 0.2 MM

D. STACKUP (14 LAYERS):

1. TOP - SIGNAL ROUTING, Plane Shape Areas: +12V, +3V3,+2V5, +1V, Rsence, V\_OSC, VCC0V9\_VTT11, 1V8, 2V5, 12V\_RTM, GND

2. POWER PLANE: GND

3. SIGNAL ROUTING, Plane Shape Areas: VccT0, VccT1, VccT2, VccT3

4. SPLIT POWER PLANE: +1V, +2V5, +3V3, AVCCPLL\_118, AVCCP\_112, AVCCP\_114\_1, AVCCP\_116, AVCCP\_118, AVCCP\_120\_1, AVCC\_3V3, AVTTRXC, AVTTTX\_112\_1, VCC, VCC\_RTM, VRN\_12, 2V5\_CP

5. SIGNAL ROUTING

6. POWER PLANE: GND

7. SIGNAL ROUTING

8. POWER PLANE: GND

9. SIGNAL ROUTING

10. SPLIT POWER PLANE: +2V5, +3V3, AVCCPLL\_1V2, AVTTX\_1V2, VCC0V9\_VREF, VRP\_20, VRN\_20

11. SIGNAL ROUTING, 12V\_RTM Plane Shape Area

12. SIGNAL ROUTING, VCC Plane Shape Area

13. SPLIT POWER PLANE: +3V3, +12V, AVCCPLL\_1V2, AVCC\_1V0, AVTXX\_1V2, GND\_SCLK, VCC, V\_OSC1, 1V8, 1V8\_SW

14. SIGNAL ROUTING, Plane Shape Areas: +1V, +3V3, +12V, AVCCPLL\_1V2, AVCCP\_118\_1, AVCC\_1V0, AVTTTX\_118, AVTTX\_1V2, FB, GND, GND\_SCLK, REF\_GND, REF\_2V5, REF\_3V3, VCC\_SCLK, VCC0V9\_VTT1

REV.	DESCRIPTION	OWNER
0	PROTOTYPE	DESY/FE
	Insert I2C buffer in uRTM IPMI Control of Hot swap controller should be changed- altered timing capacitors Error: all DQS diff. signals should go from CC I/O Xilinx Connect all signals REC of MLVDS and all *_CC of FMC to local clock - input "P" No components shall be placed on side 1 of the carrier card in the I/O area of FMC Hot-Swap controller: value of CT3 (C143) and CT12 (C144) should be altered to 1uF! PCB: SLOT for Hot Swap Switch must be ADDED!!! Clearance trace-to-plane should be > 0.2 mm Positions of mounting holes for FMC should be corrected Mounting holes for FMC should have free couper area!!! Trace between V1 and R6 (Front Red Led) schould be done in inner Layer!!! Free couper area around J15 and around mounting part of Front Panel Signal RTM1_S20 does not exist, -> correct bus RTM1_S[22:0] to RTM1_S[21:0]	

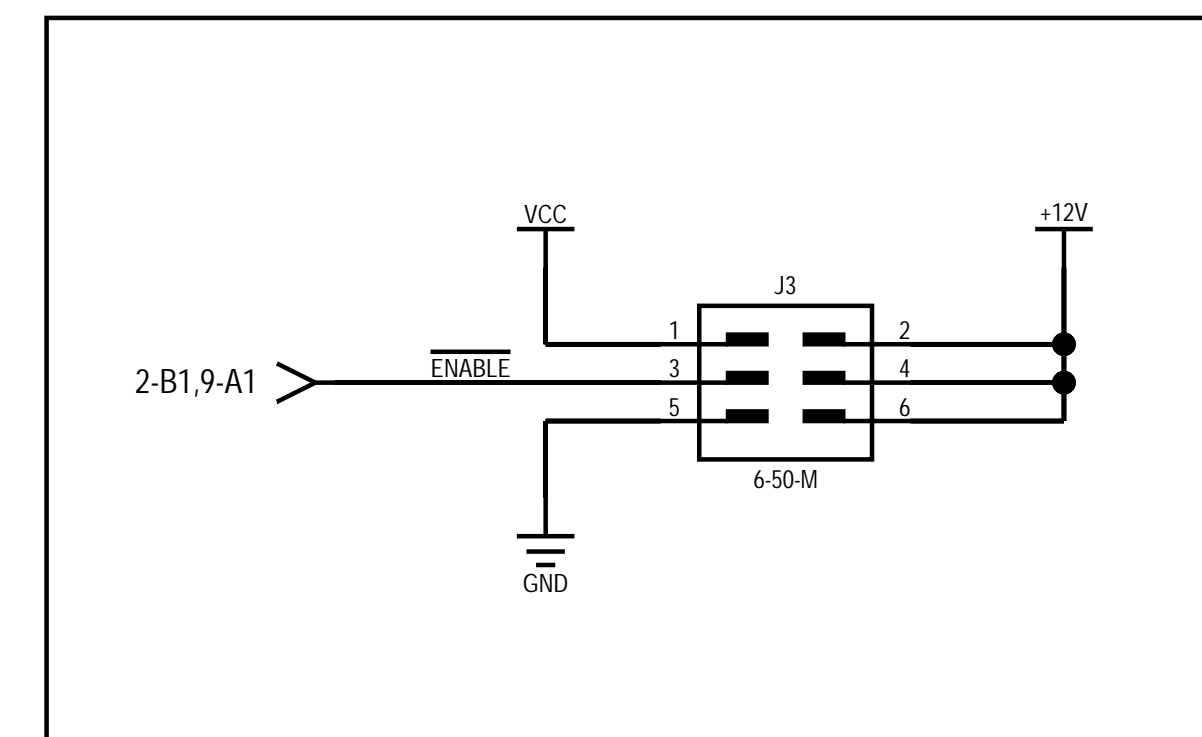
SCHEMATIC CONTENTS

- SCHEMATIC1:
- 1, 2, 3, 4, 5, 6, 7, 8, 9 - CONSTRUCTION PROPOSALS
10. BLOCK SCHEMATIC OF DAMC2
11. DDR2 POWER
12. DAMC2 WITH TWO HOME MADE MEZZANINE BOARDS
13. LAST DAMC2 BLOCK DIAGRAM
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4. ispFLASH
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6. uRTM Hot Swap CONTROLLER
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19. Powers for GTP and GTP\_SWITCH
20. MLVDS bus to Edge Connector
21. Two CLOCK Crosspoint Switches, TCLK\_B
22. GLOBAL CLOCKS
23. Spare VIRTEX-5 Banks
24. Four SFP connectors
25. SFP CONTROLLER, USER LEDs
26. Two connectors to RTM, 3 Amp/12V
27. 2V5 Interface to RTM
28. Power for GTP, DDR2 and ispFlash
29. Main Power for DAMC+FMC+uRTM

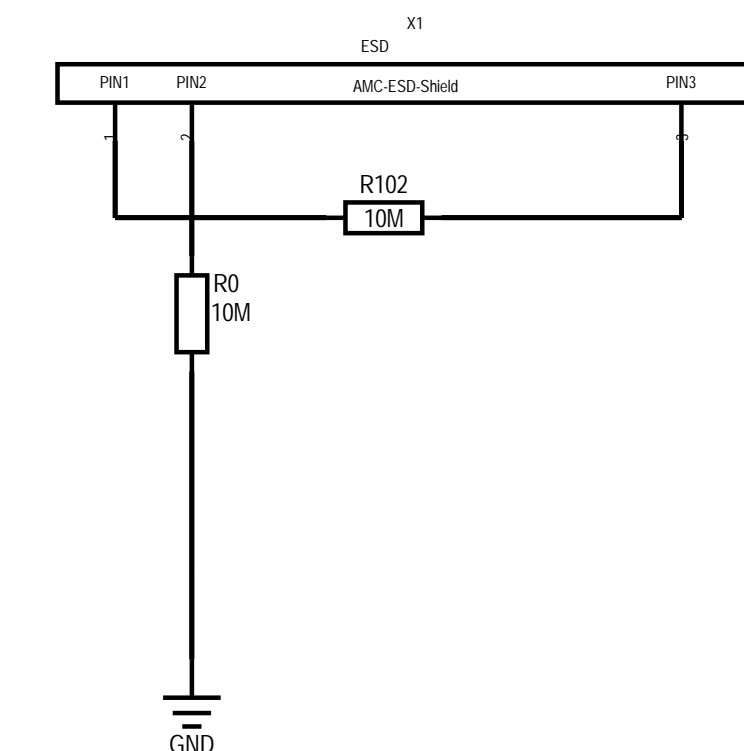
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		Schematic:	schematic2
Drawn by:	Vetrov P.	Sheet:	
Layouter:	Vetrov P.	DESY- FEA	Notkestrasse 85 D-22607 Hamburg
Changed of sch:	Vetrov P.		
Date Changed:	07.03.2012	PCB No:	8423
		Rev:	02
		Size:	A3
Date of prod. data:		PCB name:	DAMC2_02
		Sheet:	1 of 32

# EDGE Plastic Connector

## AUX\_Power\_Connector



## ESD strip

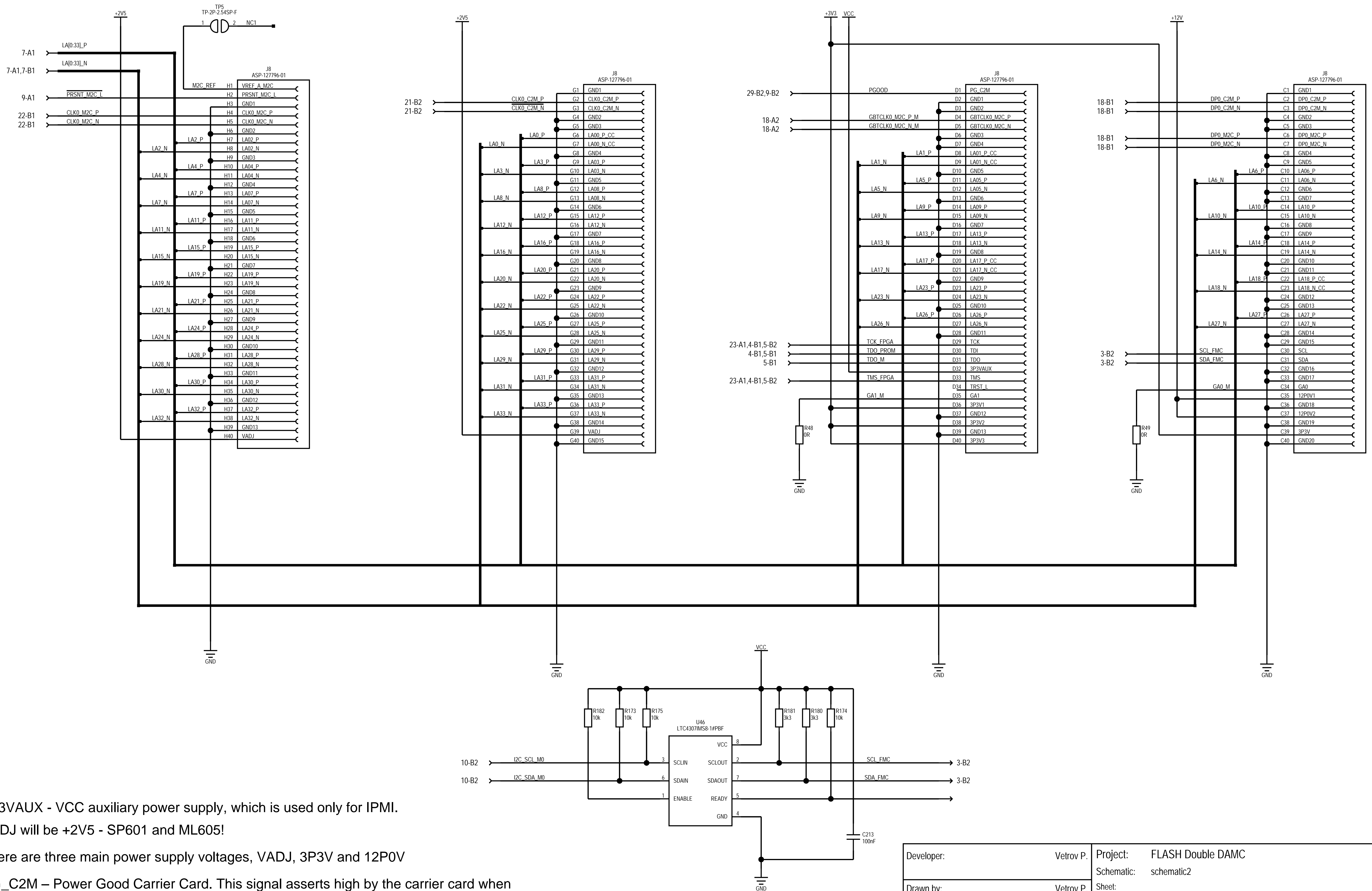


← Should be open!!!!

Max Hight of components on side 2 is 3mm!!!  
Max thickness of PCB is 1.76 mm (1.6 mm +10%)!!!

Developer:	Vetrov P.	Project: FLASH Double DAMC					
Drawn by:	Vetrov P.	Schematic: schematic2					
Layouter:	Vetrov P.	DESY- FEA Notkestrasse 85 D-22607 Hamburg					
Changed of sch:	Vetrov P.						
Date Changed:	07.03.2012	PCB No:	8423	Rev:	02	Size:	A3
Date of prod. data:		PCB name:	DAMC2_02	Sheet:	2	of	32

# FMC connector (LPC)



3P3VAUX - VCC auxiliary power supply, which is used only for IPMI.

VADJ will be +2V5 - SP601 and ML605!

There are three main power supply voltages, VADJ, 3P3V and 12P0V

PG\_C2M – Power Good Carrier Card. This signal asserts high by the carrier card when power supplies, VADJ, 12P0V, 3P3V, are within tolerance.

VREF\_A\_M2C - ref. voltage associated with the signaling standard used by the bank A data pins, LAXx.

If the signaling standard on Bank A does not require a reference voltage then this pin can be left unconnected.

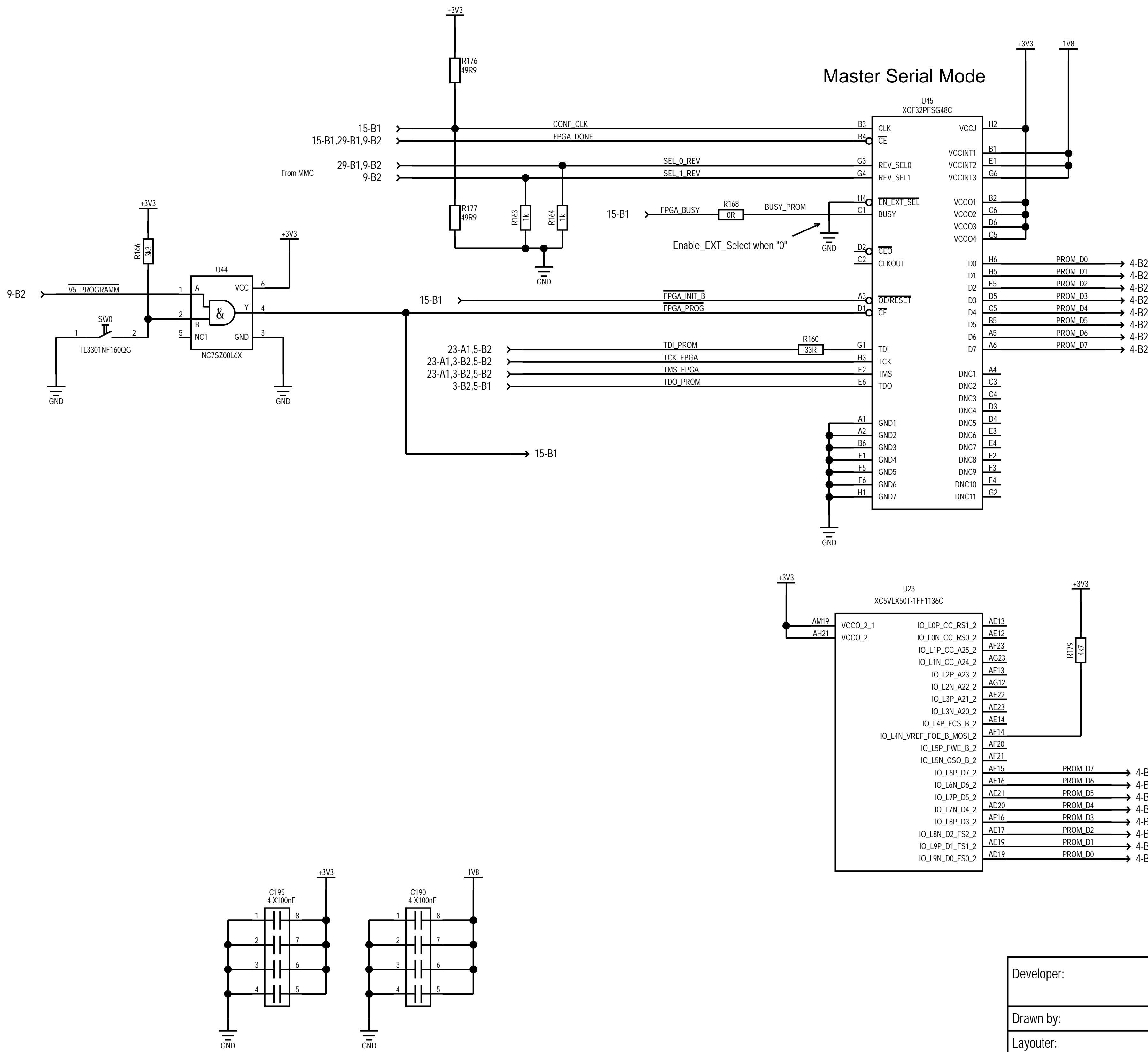
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		Schematic: schematic2					
Drawn by:	Vetrov P.	Sheet:					
Layouter:	Vetrov P.	DESY- FEA Notkestrasse 85					
Changed of sch:	Vetrov P.	D-22607 Hamburg					
Date Changed:	07.03.2012	PCB No:	8423	Rev:	02	Size:	A3
Date of prod. data:		PCB name:	DAMC2_02	Sheet:	3	of	32

# FPGA Master SelectMAP (Parallel) Mode

+3V3\_Payload = +3V3

+3V3 MP = VCC

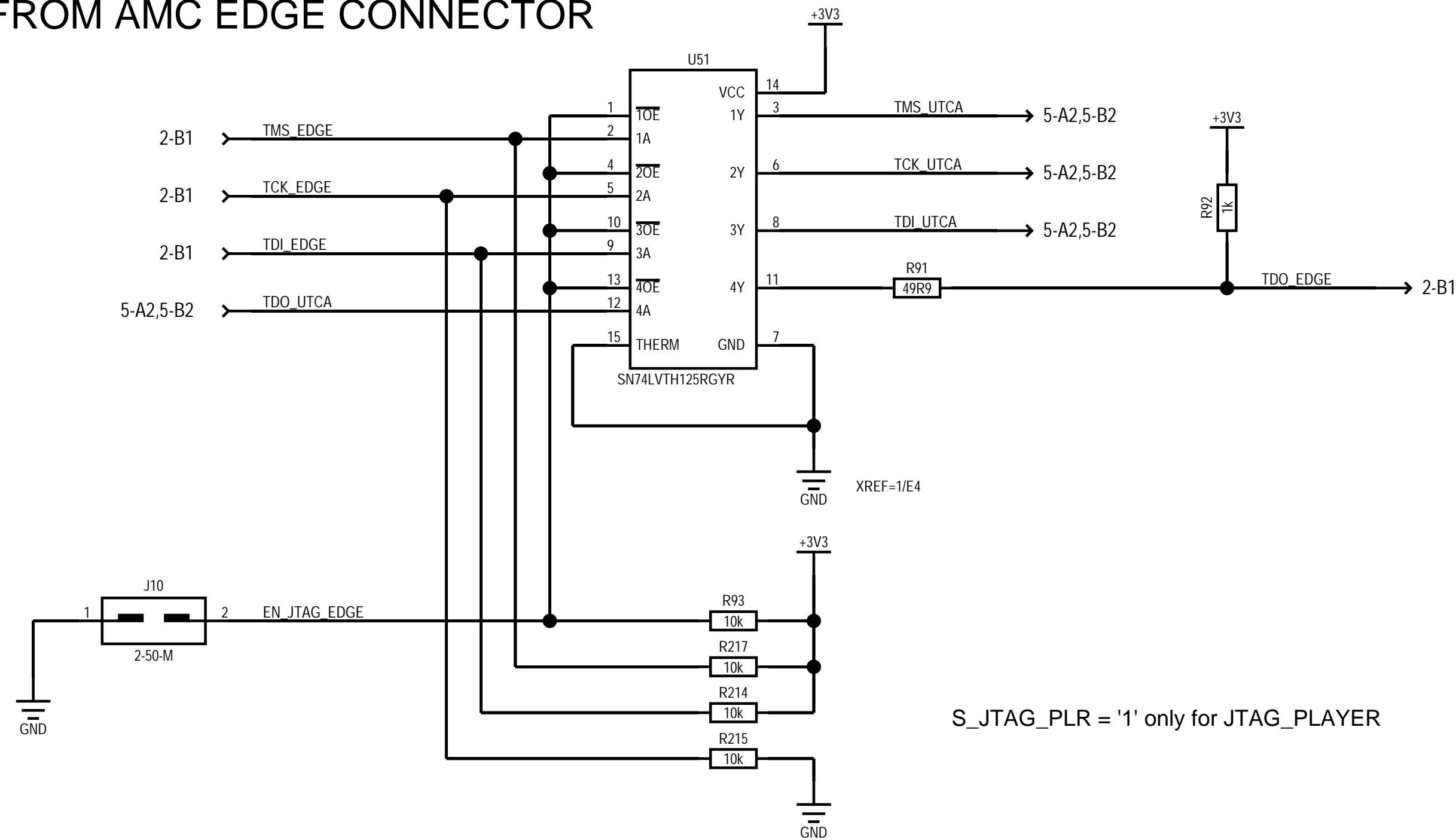
Revision Numbers, should be connected to MMC - sel\_rev!



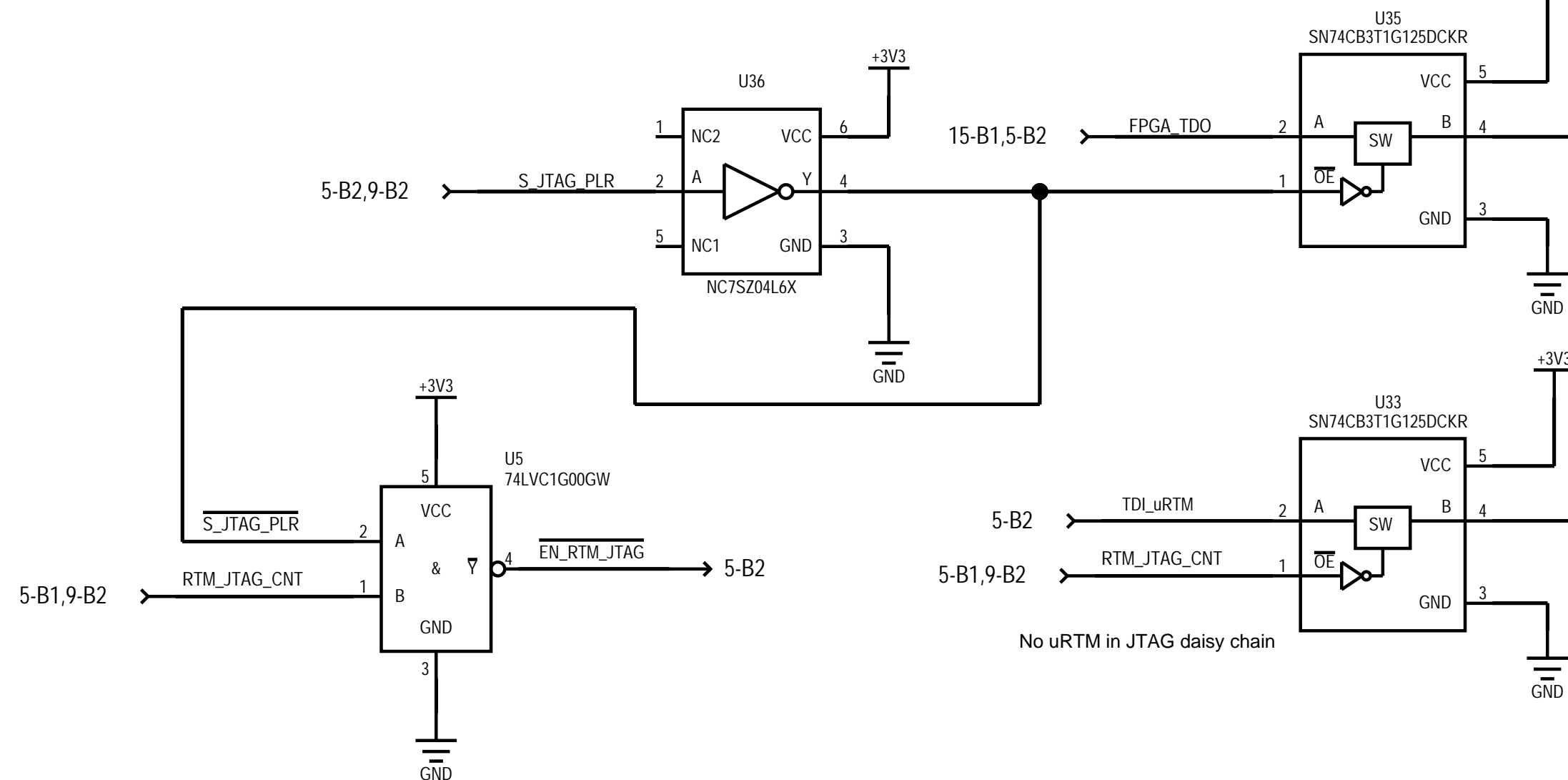
Developer:	Vetrov P.	Project:	FLASH Double DAMC		
		Schematic:	schematic2		
Drawn by:	Vetrov P.	Sheet:			
Layouter:	Vetrov P.	DESIGN- FEA	Notkestrasse 85 D-22607 Hamburg		
Changed of sch:	Vetrov P.				
Date Changed:	07.03.2012	PCB No:	8423	Rev:	02
Date of prod. data:		PCB name:	DAMC2_02	Size:	A3
		Sheet:	4	of	32

# JTAG Chain

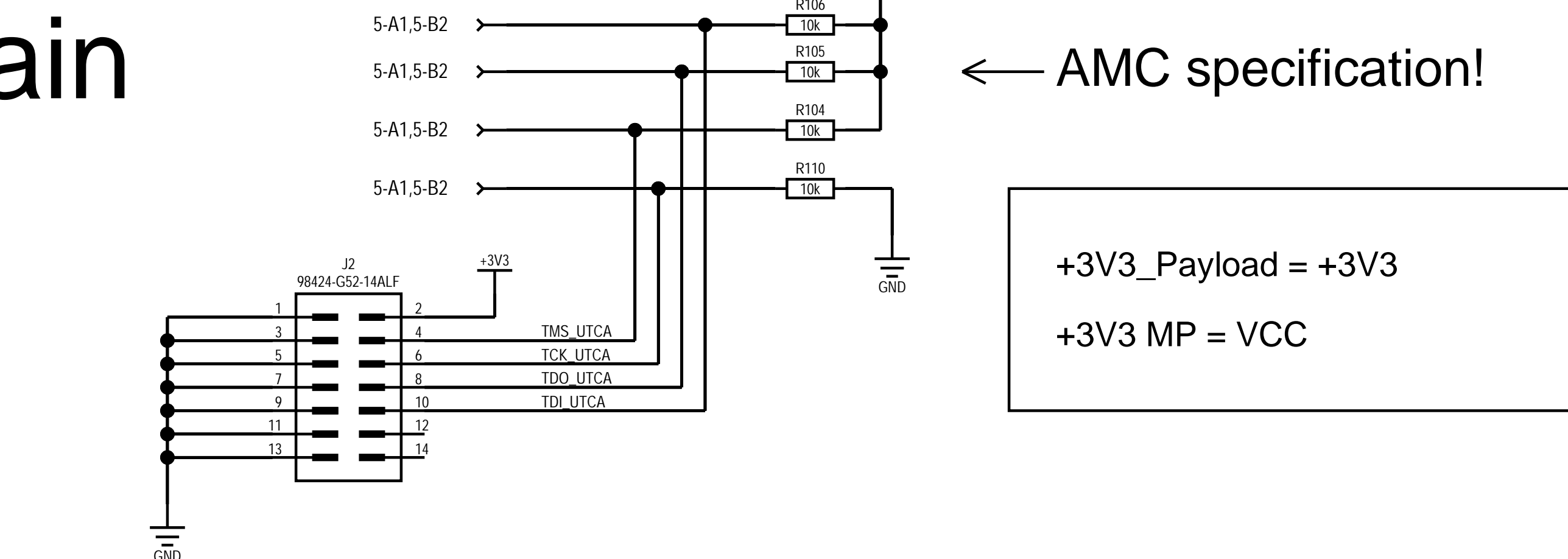
## JTAG SIGNALS FROM AMC EDGE CONNECTOR



S\_JTAG\_PLR = '1' only for JTAG\_PLAYER



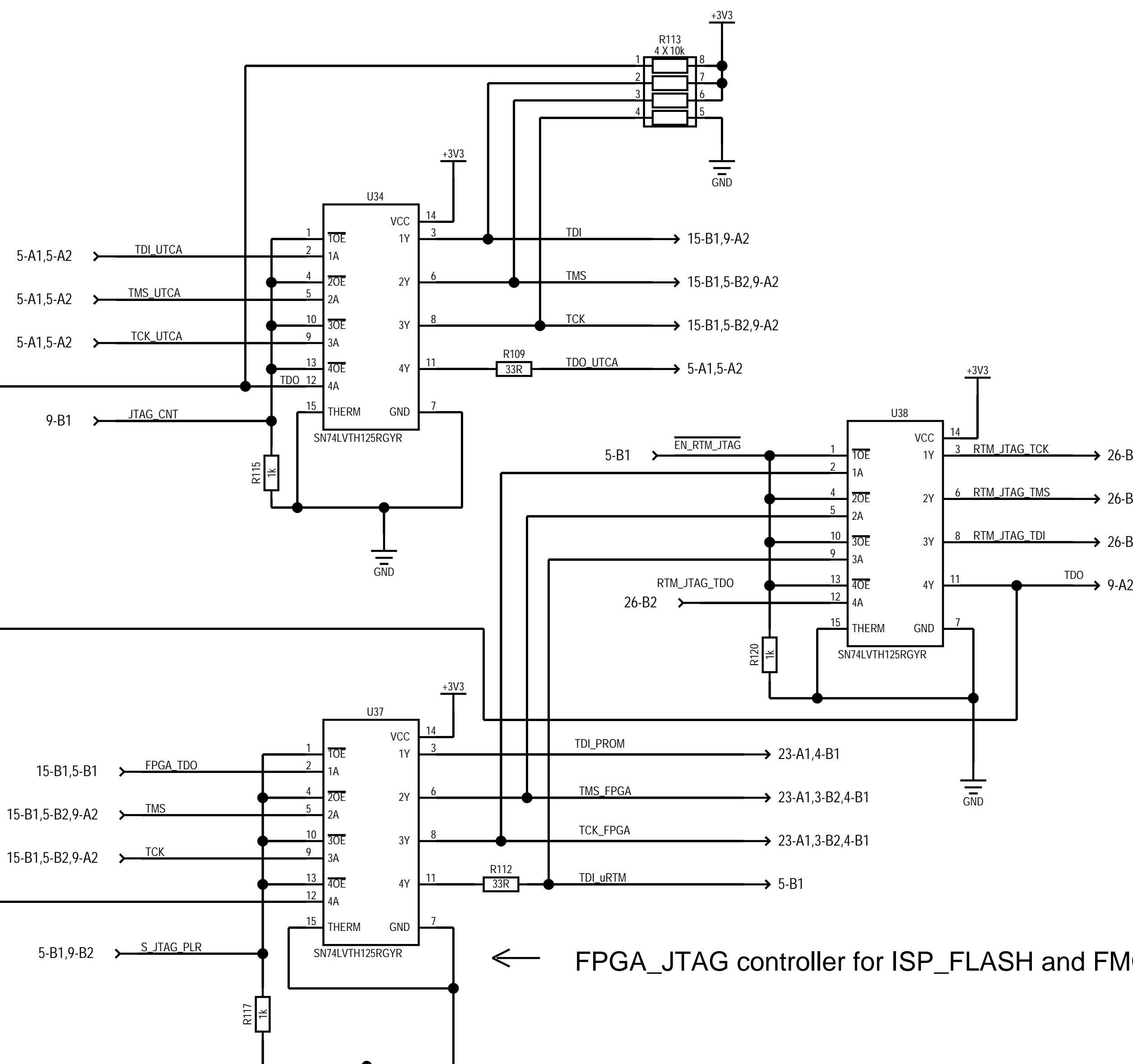
No uRTM in JTAG daisy chain



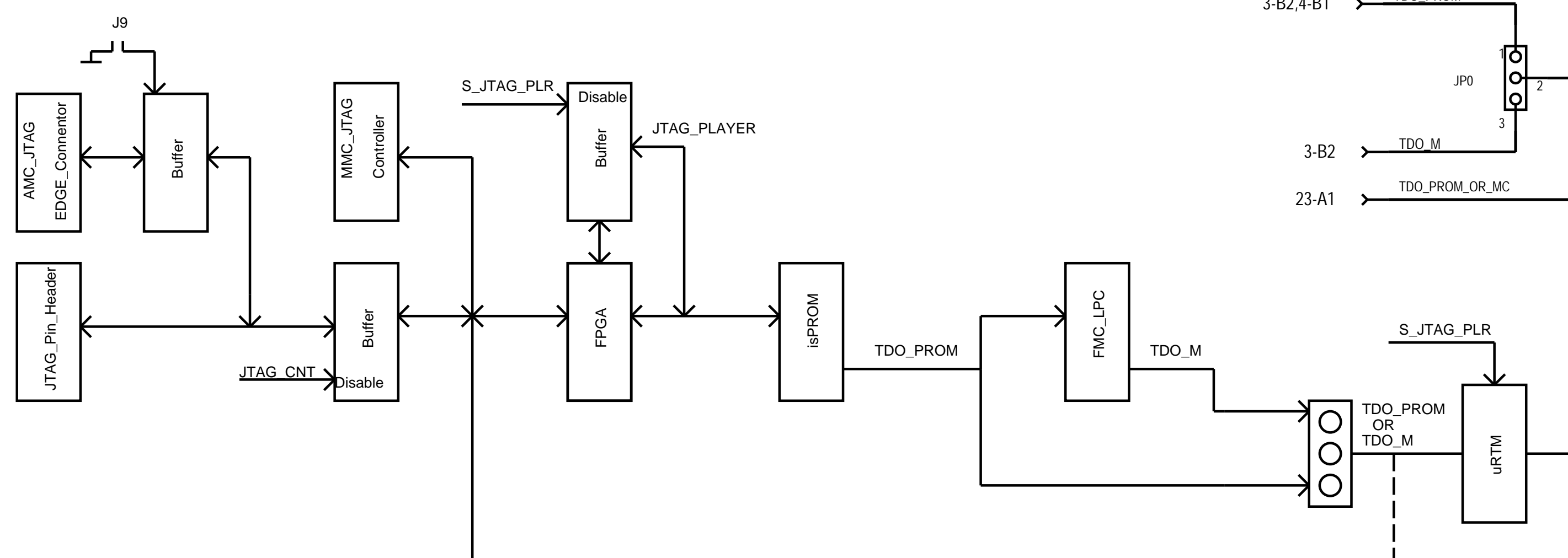
- AMC specification!

+3V3\_Payload = +3V3  
+3V3 MP = VCC

LVTH125's OUTPUT IN HIGH IMPEDANCE IF VCC <1.5V!!!!



## FPGA\_JTAG controller for ISP\_FLASH and FMC

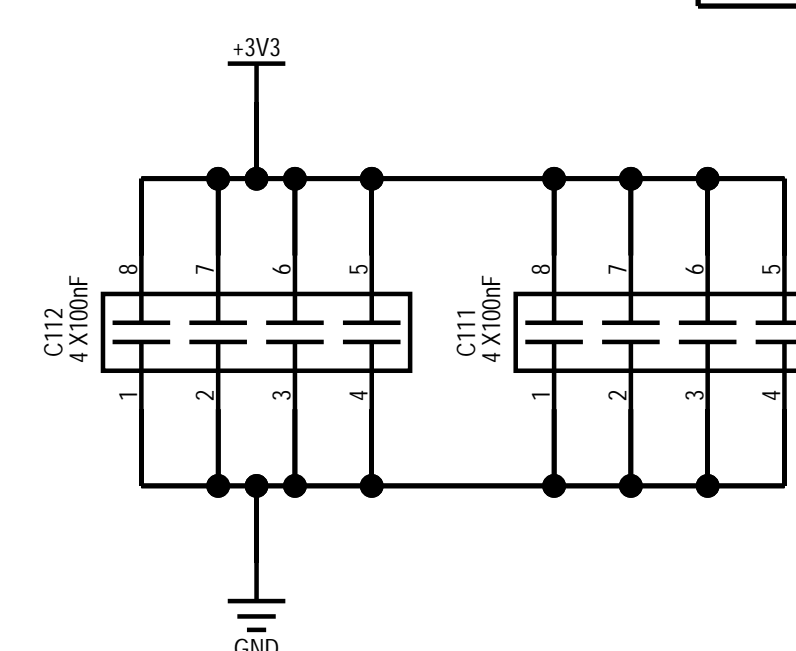


If signal JTAG\_CNT= "1", then JTAG signals will be got from MMC, otherwise from AMC edge connector or JTAG pin-header J3

If FPGA\_JTAG\_PLAYER regime is set, then S\_JTAG\_PLR = '1' and ISP\_FLASH and FMC will receive JTAG signals from XILINX but normal JTAG daisy chain will be finished on XILINX, that is FPGA\_TDO will go to JTAG TDO.

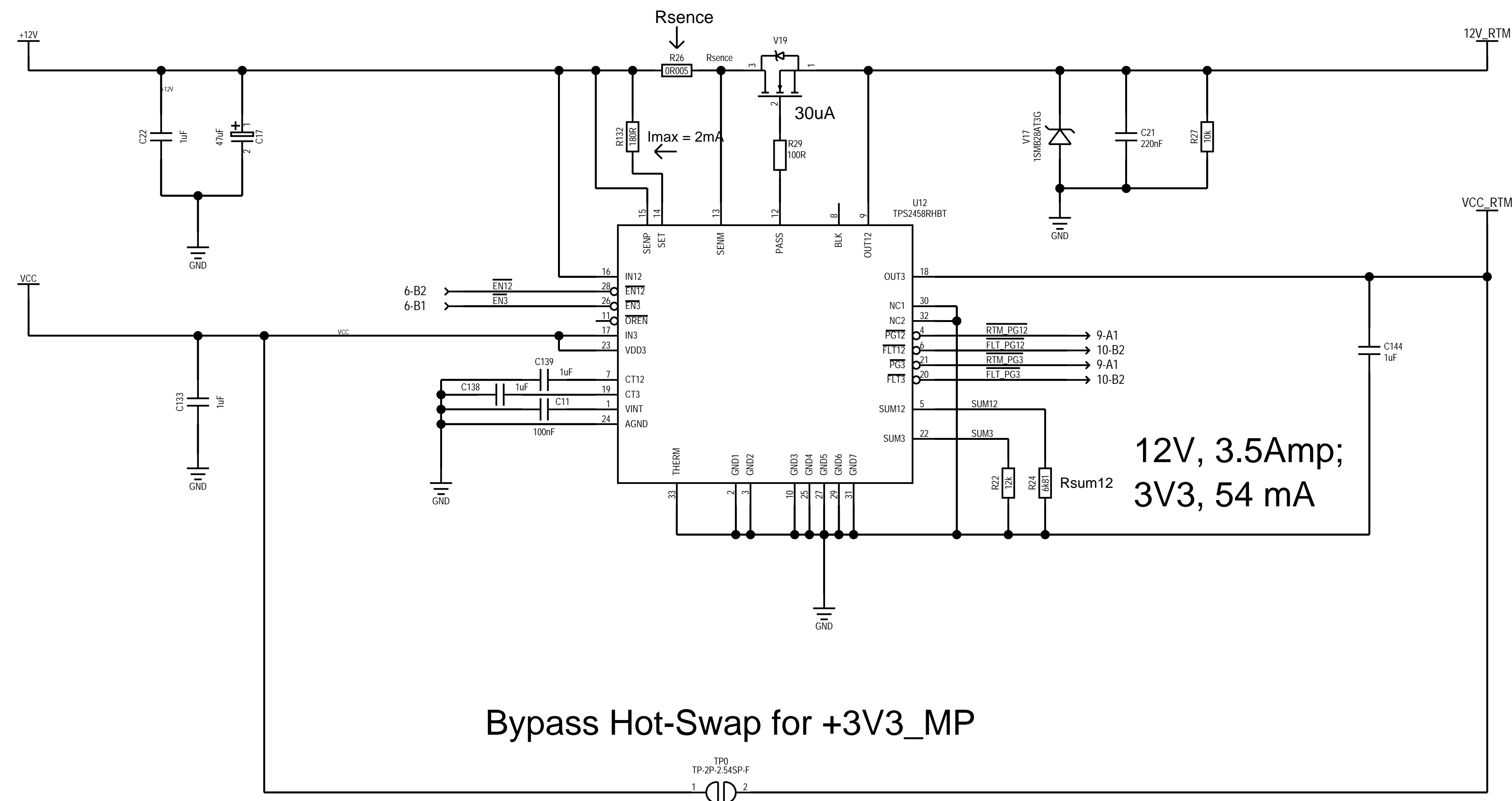
In FPGA\_JTAG\_PLR regime JTAG daisy chain will not include uRTM board.

If signal RTM\_JTAG\_CNT= "1", then RTM will includes in FPGA JTAG chain, except the FPGA\_JTAG\_PLR regime

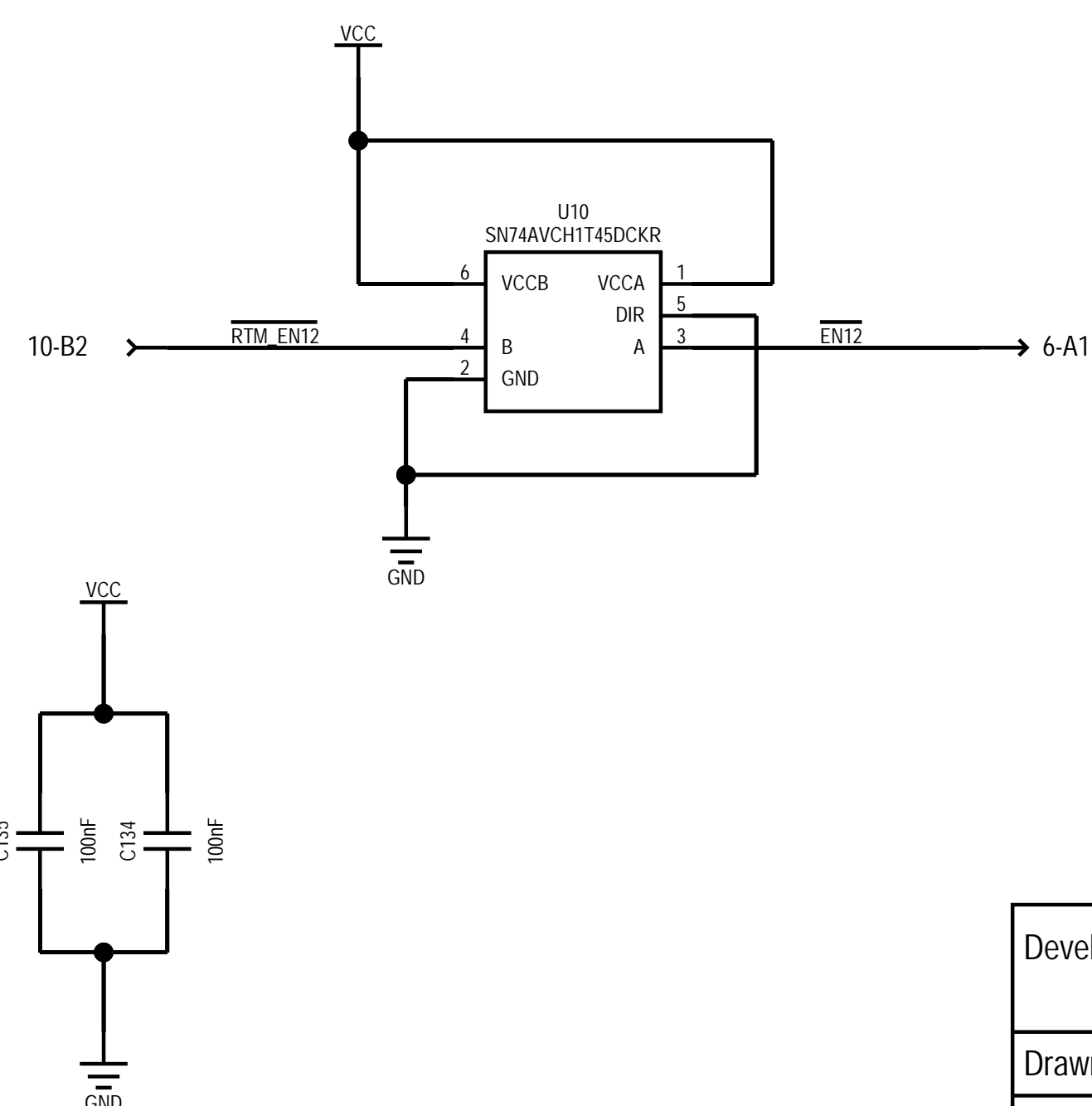
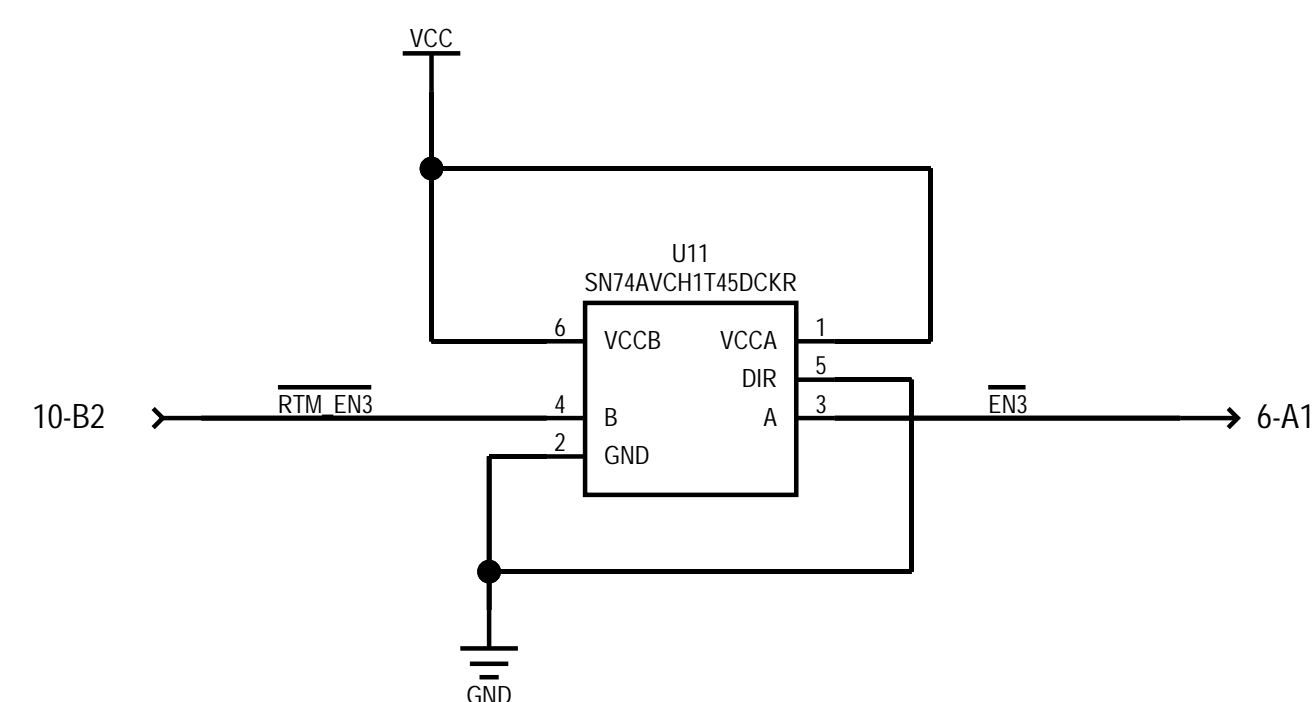


Developer:	Vetrov P.	Project:	FLASH Double DAMC				
		Schematic:	schematic2				
Drawn by:	Vetrov P.	Sheet:					
Layouter:	Vetrov P.	DESY- FEA	Notkestrasse 85 D-22607 Hamburg				
Changed of sch:	Vetrov P.						
Date Changed:	07.03.2012	PCB No:	8423	Rev:	02	Size:	A3
Date of prod. data:		PCB name:	DAMC2_02	Sheet:	5	of	32

# uRTM Hot Swap CONTROLLER



## Bypass Hot-Swap for +3V3\_MP



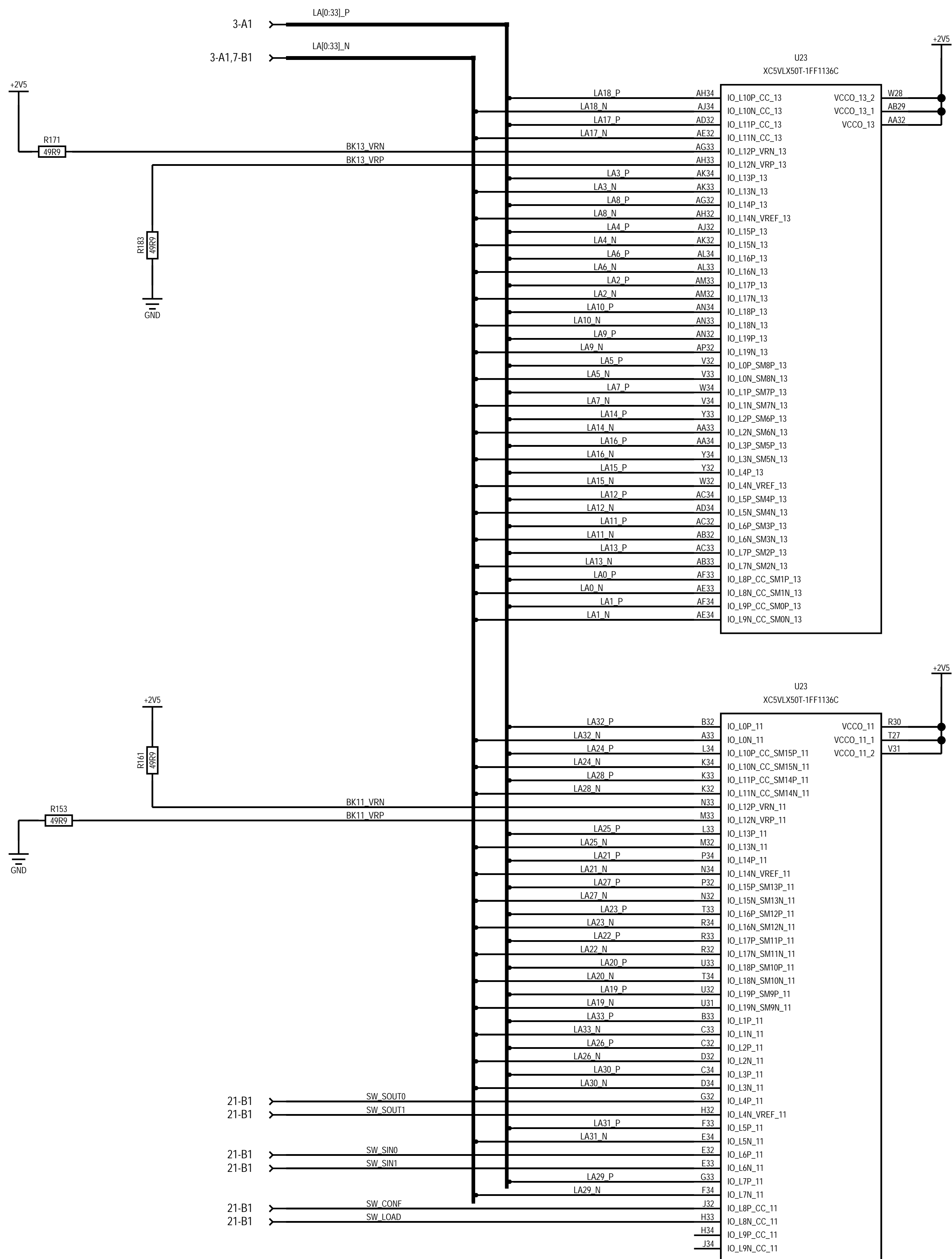
Signals #RTM\_EN12 and #RTM\_EN3 are active low!

Signals #RTM\_EN12 and #RTM\_EN3 have internal pull-up

Developer:	Vetrov P.	Project: FLASH Double DAMC					
Drawn by:	Vetrov P.	Schematic: schematic2					
Layouter:	Vetrov P.	DESY- FEA Notkestrasse 85 D-22607 Hamburg					
Changed of sch:	Vetrov P.						
Date Changed:	07.03.2012	PCB No:	8423	Rev:	02	Size:	A3
Date of prod. data:		PCB name:	DAMC2_02	Sheet:	6	of	32

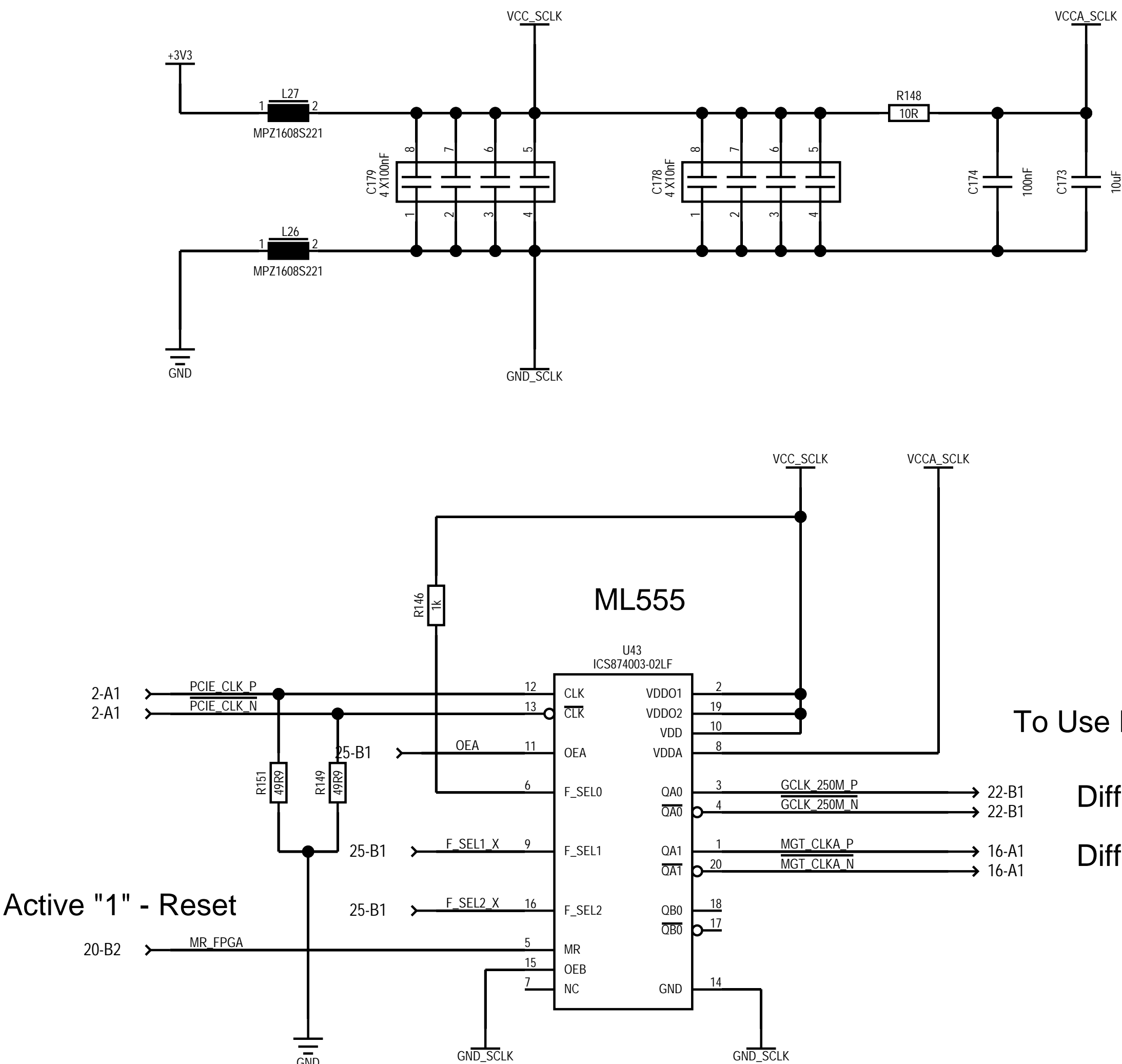


# Interface to FMC (LPC) connector



Developer:	Vetrov P.	Project: FLASH Double DAMC					
		Schematic: schematic2					
Drawn by:	Vetrov P.	Sheet:					
Layouter:	Vetrov P.	DESY- FEA Notkestrasse 85 D-22607 Hamburg					
Changed of sch:	Vetrov P.						
Date Changed:	07.03.2012	PCB No:	8423	Rev:	02	Size:	A3
Date of prod. data:		PCB name:	DAMC2_02	Sheet:	7	of	32

PCIExpress Clock



True Table

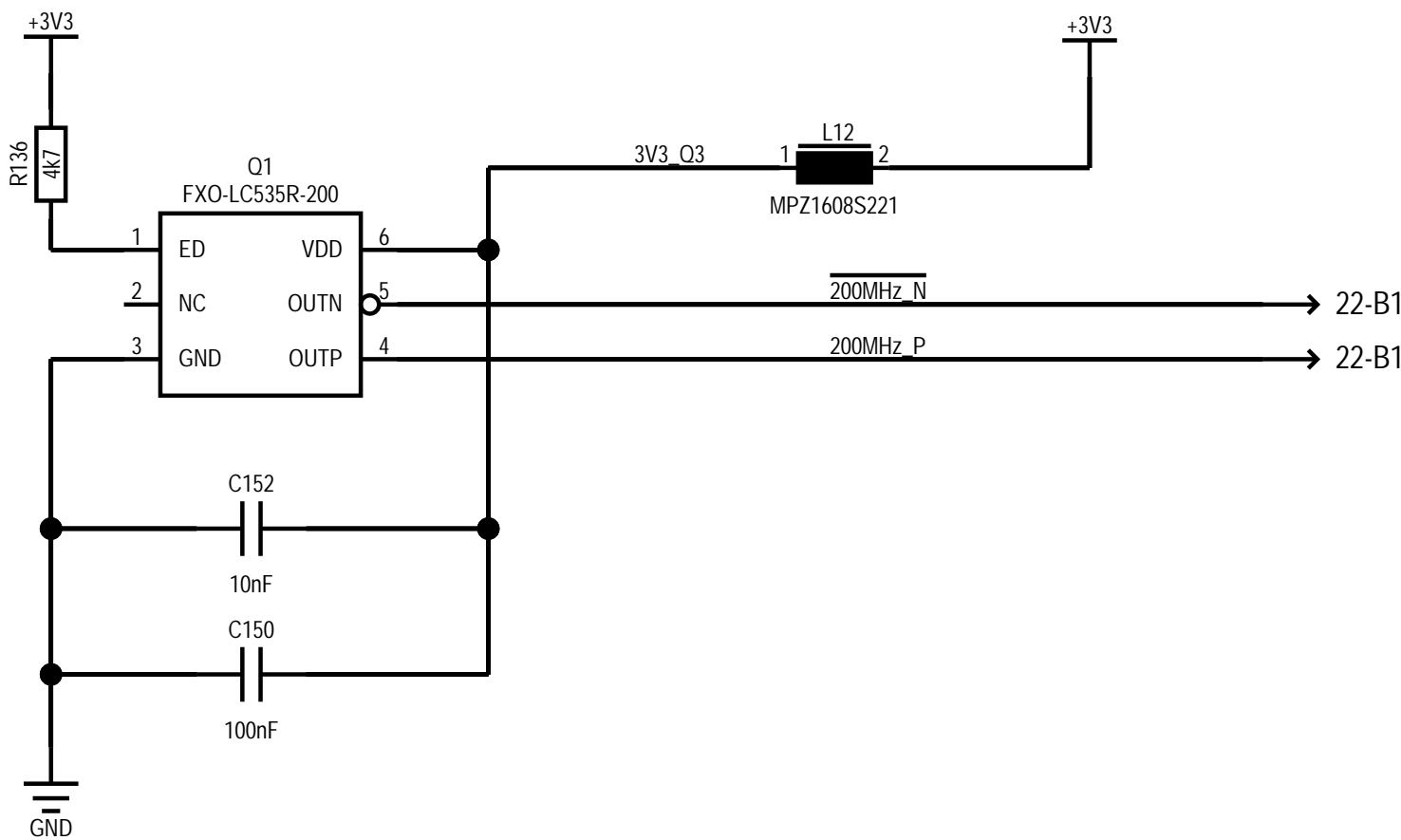
Inputs			Outputs	
F_SEL2	F_SEL1	F_SEL0	QA0/nQA0, QA1/nQA1	QB0/nQB0
0	0	0	/2	/2
1	0	0	/5	/2
0	1	0	/4	/2
1	1	0	/2	/4
0	0	1	/2	/5
1	0	1	/5	/4
0	1	1	/4	/5
1	1	1	/4	/4

To Use Differential Termination Attribute in FPGA for supporting LVDS signals

Differential Global Clock input of FPGA(GCLK) - 250MHz

Differential reference clock for GTP transceiver(MGT\_REFCLK) - 250MHz

IODELAY CLOCK



TO VIRTEX

Developer:	Vetrov P.	Project:	FLASH Double DAMC		
		Schematic:	schematic2		
Drawn by:	Vetrov P.	Sheet:			
Layouter:	Vetrov P.	DESIGN- FEA	Notkestrasse 85		
Changed of sch:	Vetrov P.		D-22607 Hamburg		
Date Changed:	07.03.2012	PCB No:	8423	Rev:	02
Date of prod. data:		PCB name:	DAMC2_02	Size:	A3
				Sheet:	8 of 32



# MMC

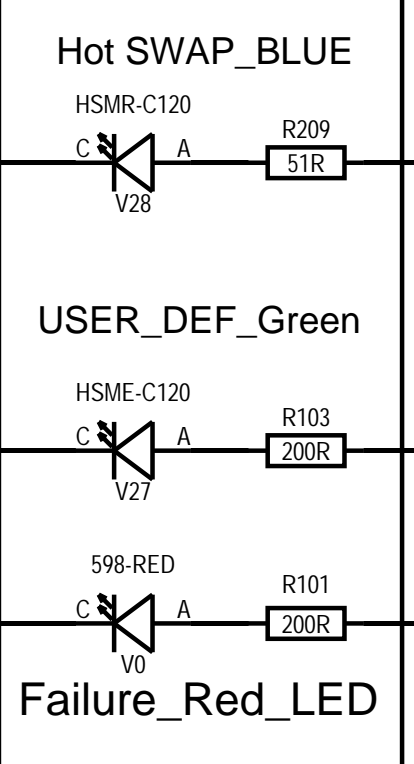
+3V3\_Payload = +3V3  
+3V3 MP = VCC  
max 150mA

ON\_FRONT\_PANEL!!!

HSMR-C120

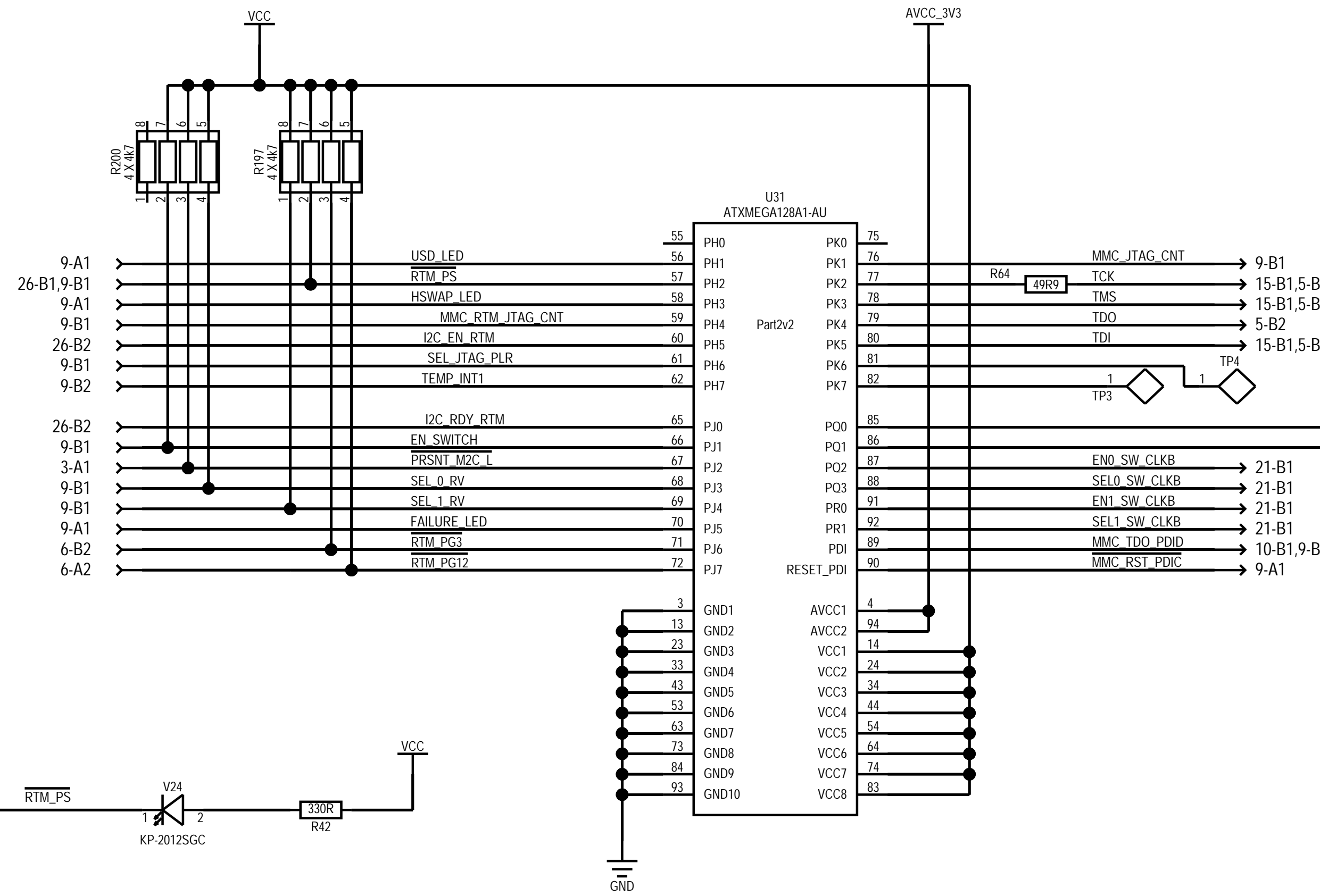
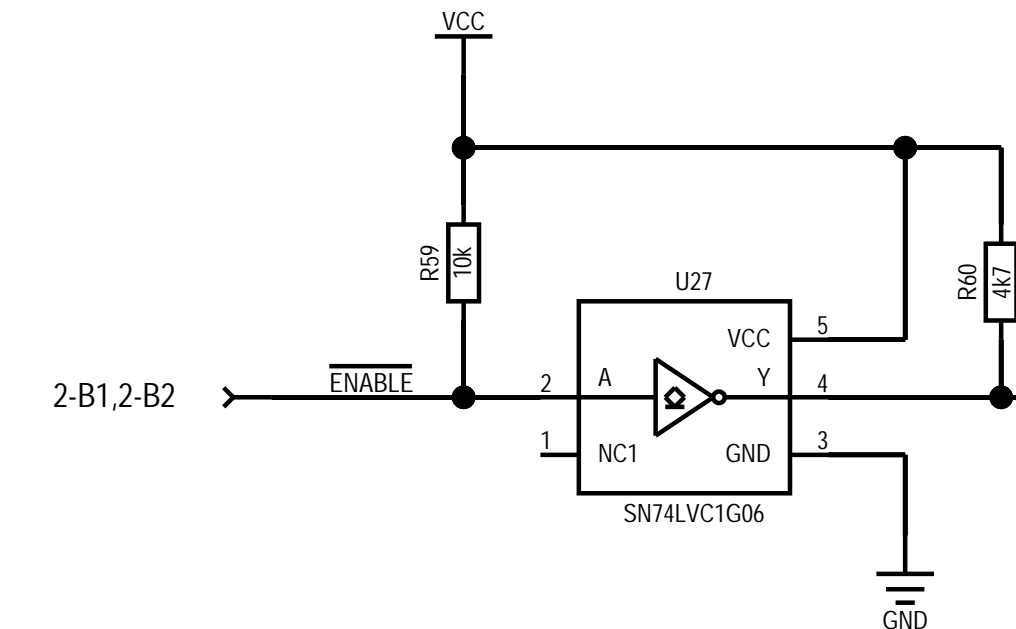
HSME-C120

5988010107F



V1 should be moved in PCB top on 0.5mm

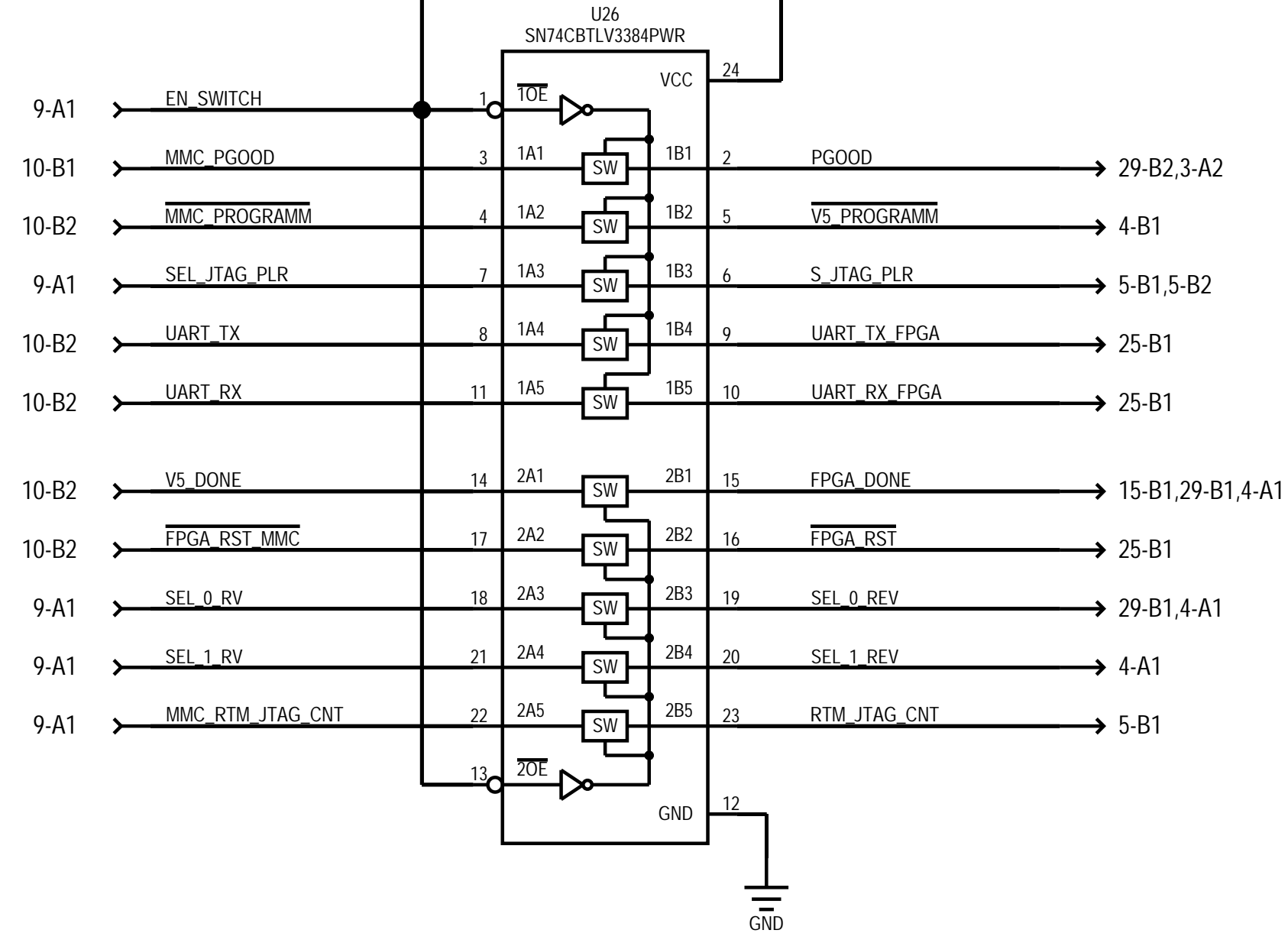
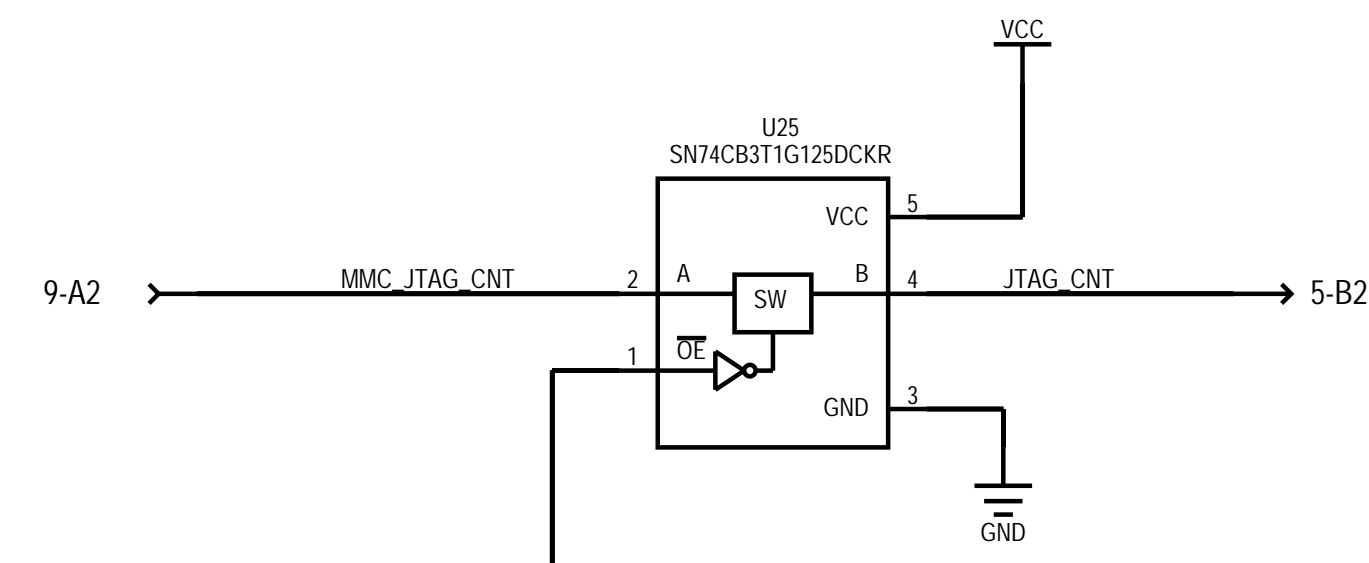
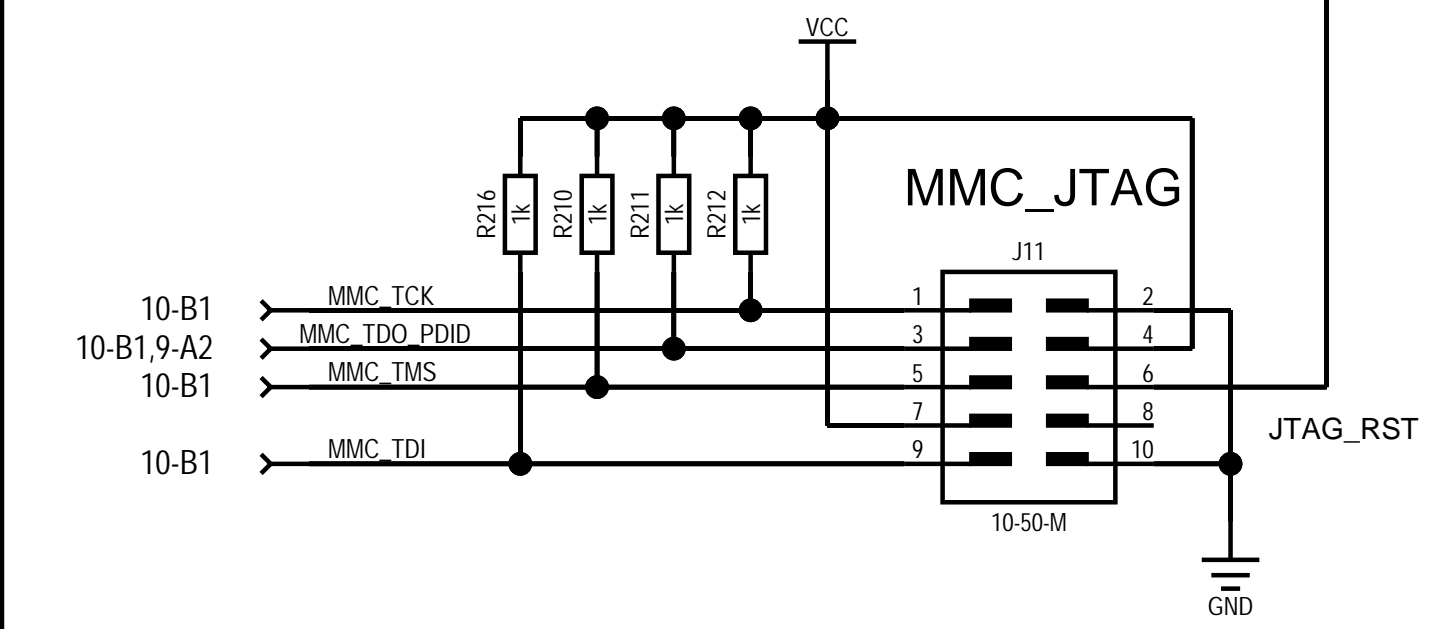
ON\_BOARD!!!RED



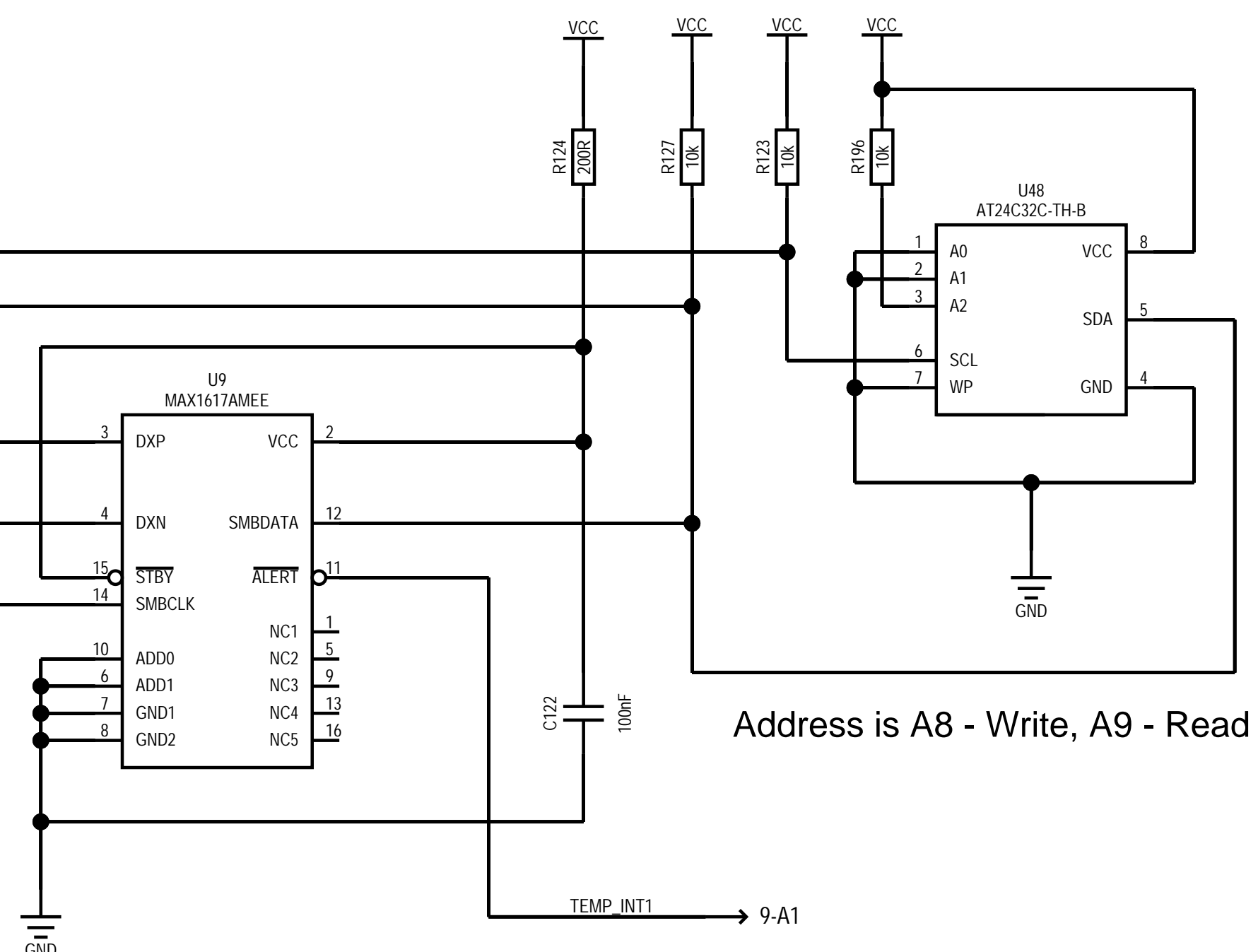
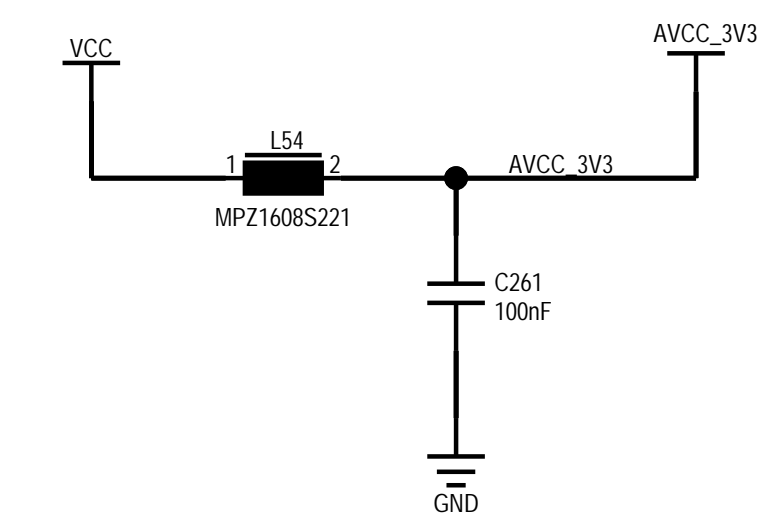
JTAG\_TO\_FPGA

Program and Debug Interface

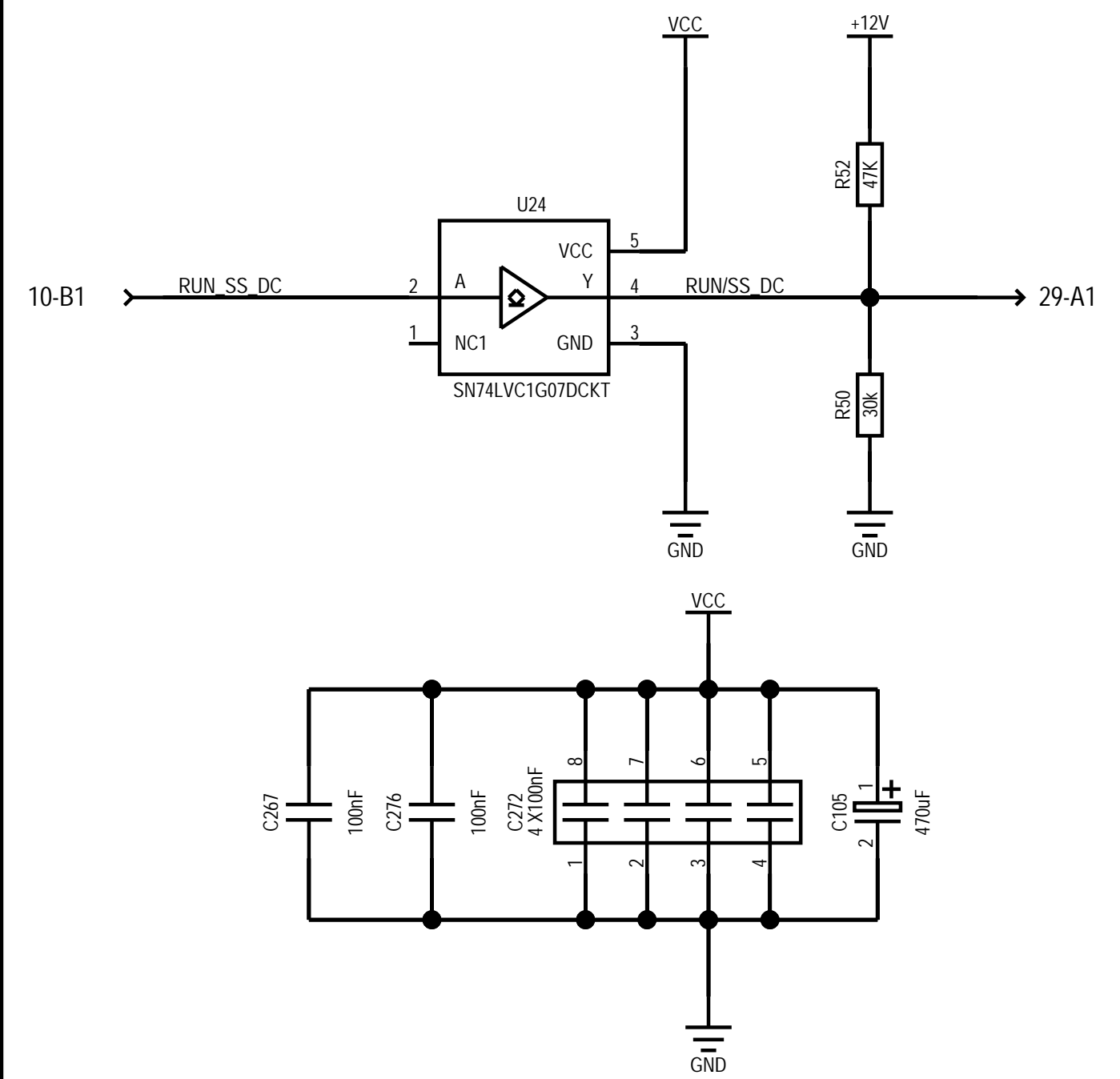
After Power-up signals:  
EN0/1\_SW\_CLKB should be "0"



Temperature-sensing diode pins of FPGA

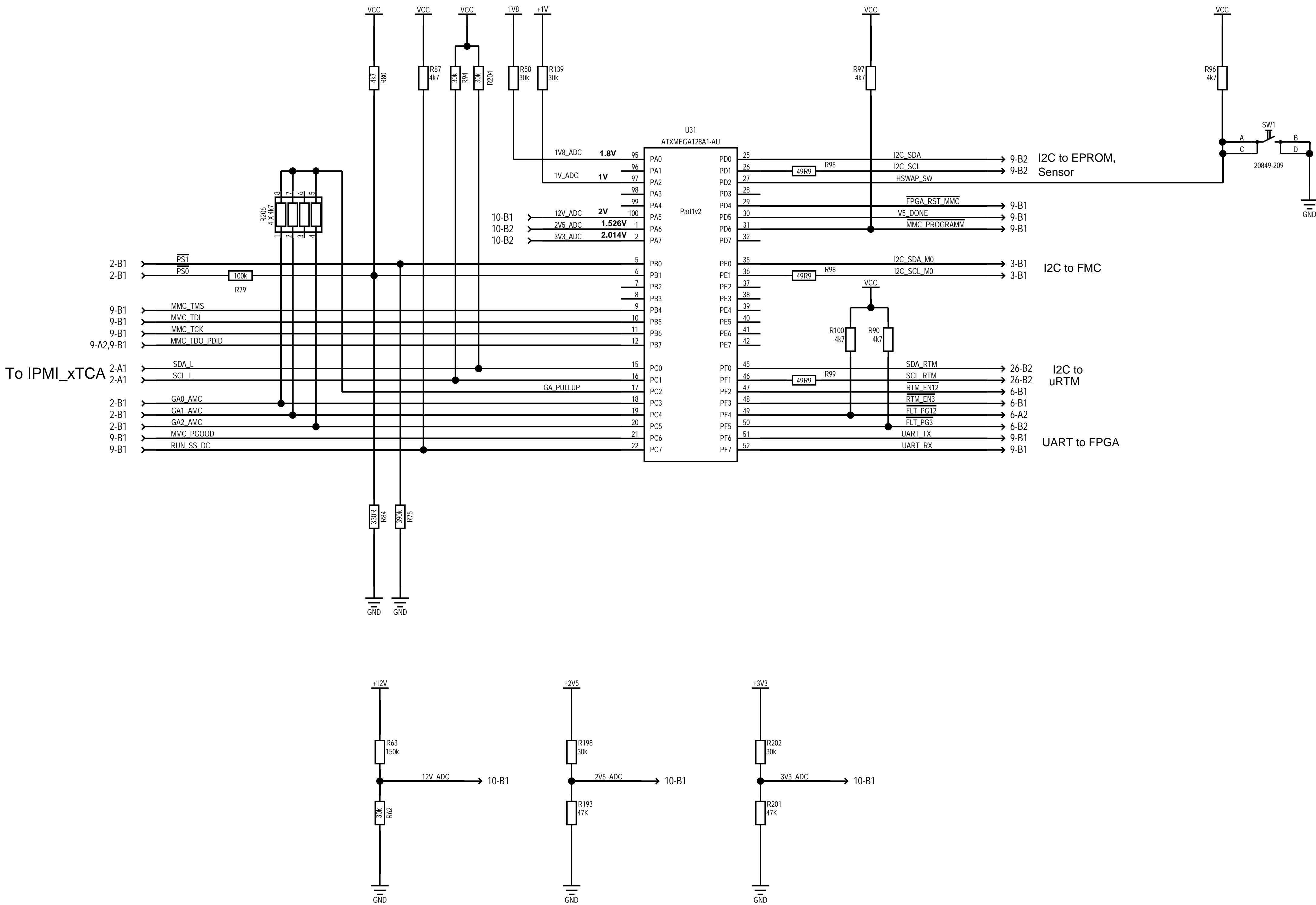


Address is A8 - Write, A9 - Read



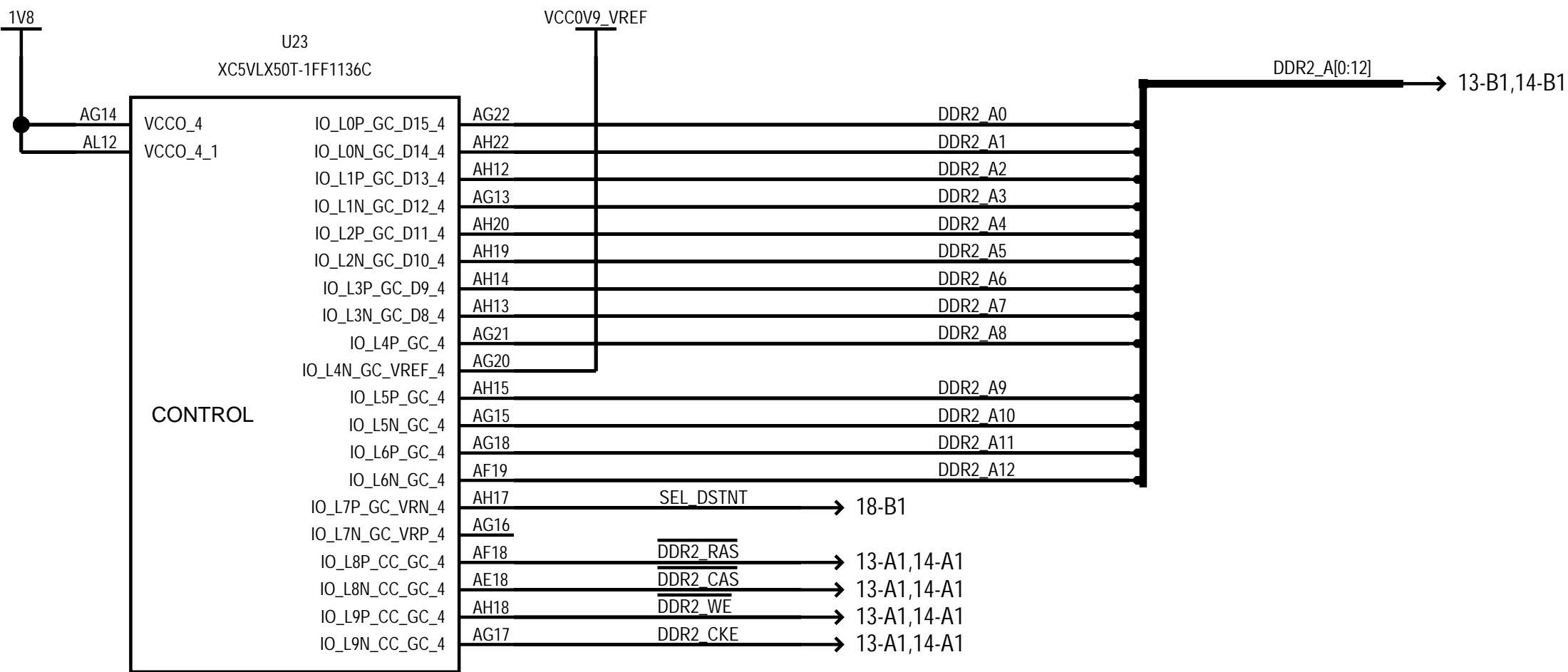
Developer:	Vetrov P.	Project:	FLASH Double DAMC
Drawn by:	Vetrov P.	Schematic:	schematic2
Layouter:	Vetrov P.	Sheet:	
Changed of sch:	Vetrov P.	DESIGN - FEA	Notkestrasse 85 D-22607 Hamburg
Date Changed:	07.03.2012	PCB No:	8423
Date of prod. data:		PCB name:	DAMC2_02
Rev:	02	Size:	A3
Sheet:	9 of 32		

MMC\_2

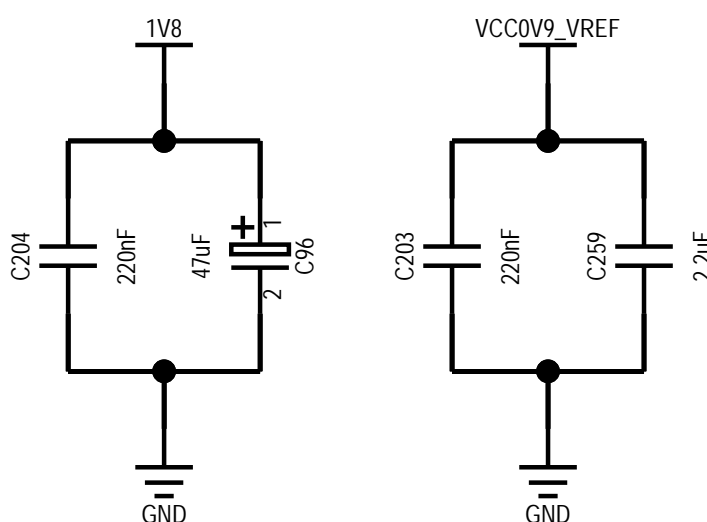


Developer:	Vetrov P.	Project:	FLASH Double DAMC		
		Schematic:	schematic2		
Drawn by:	Vetrov P.	Sheet:			
Layouter:	Vetrov P.	DESIGN- FEA	Notkestrasse 85 D-22607 Hamburg		
Changed of sch:	Vetrov P.				
Date Changed:	07.03.2012	PCB No:	8423	Rev:	02
				Size:	A3
Date of prod. data:		PCB name:	DAMC2_02	Sheet:	10 of 32

# DDR2 address and control signals

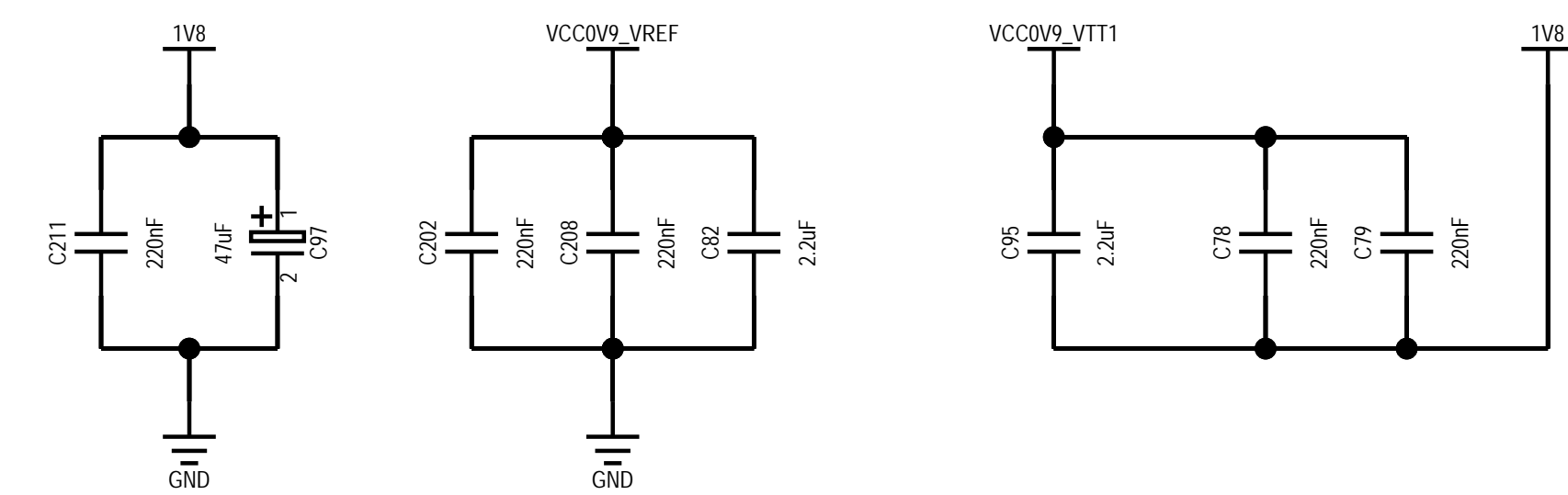
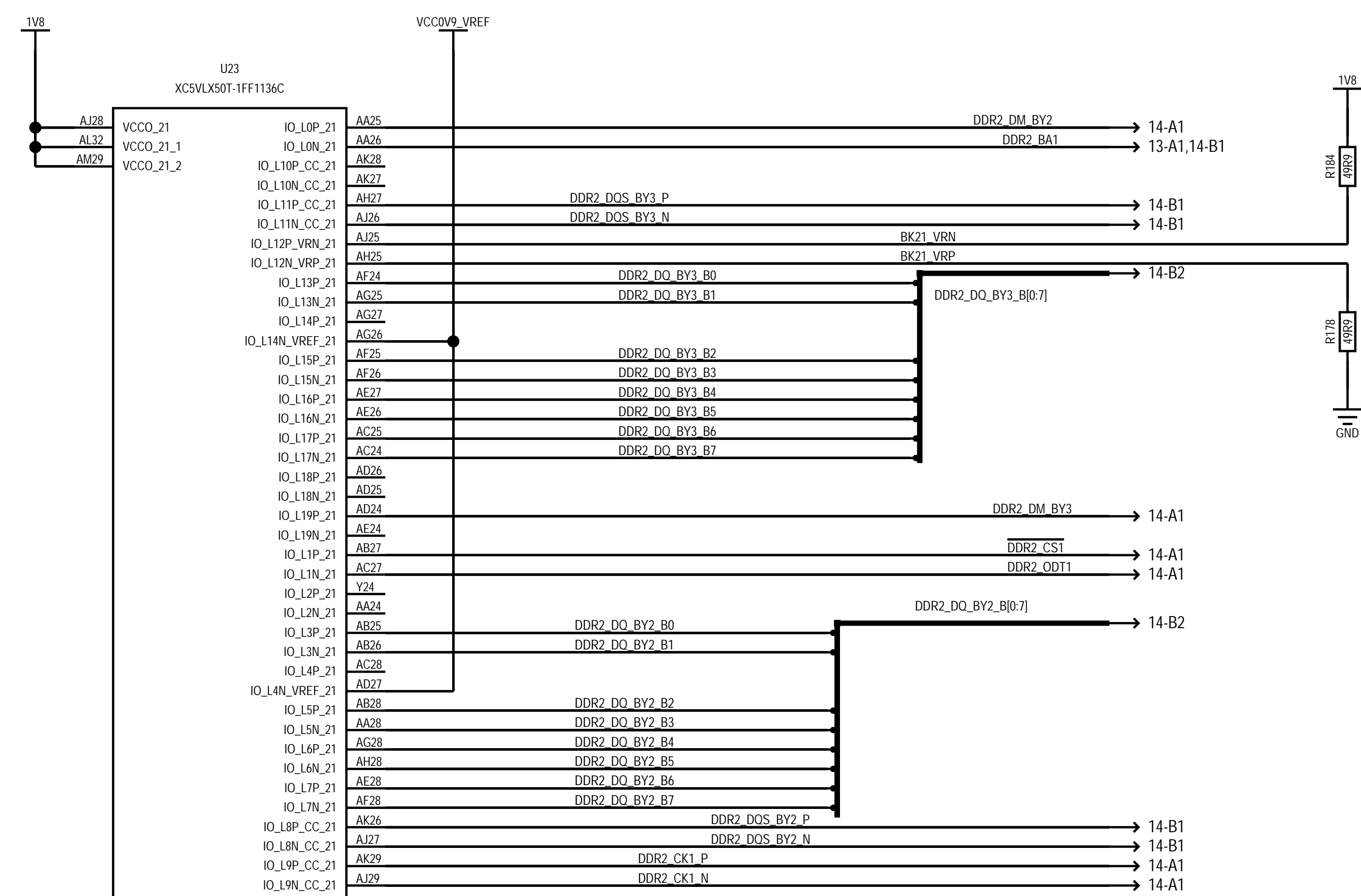
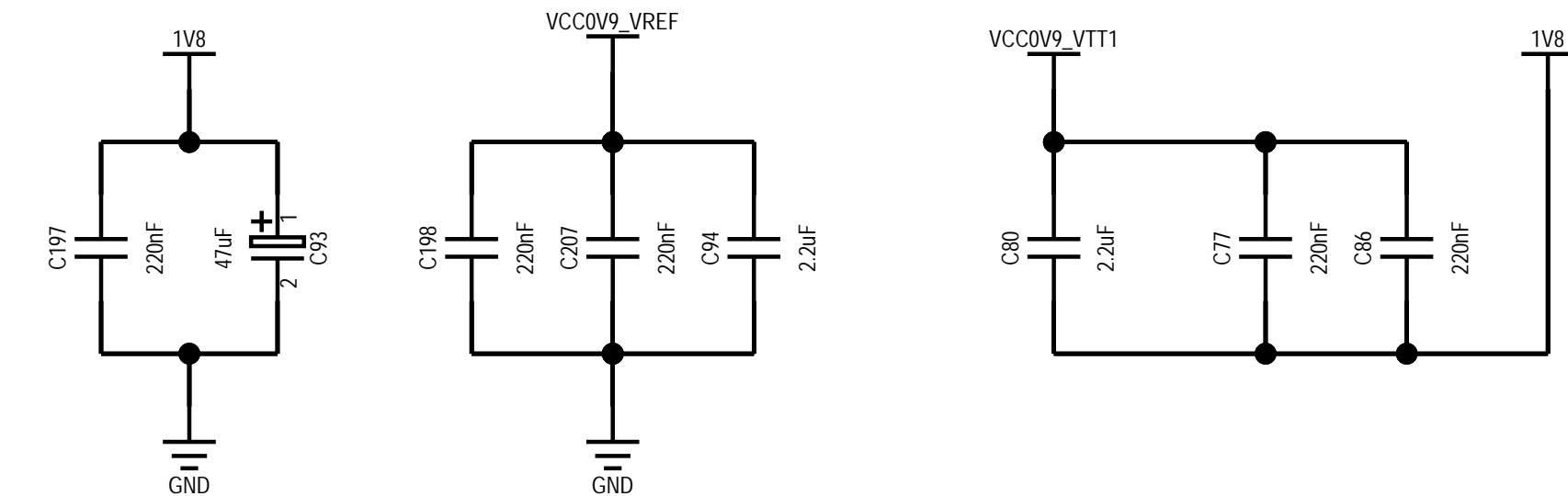
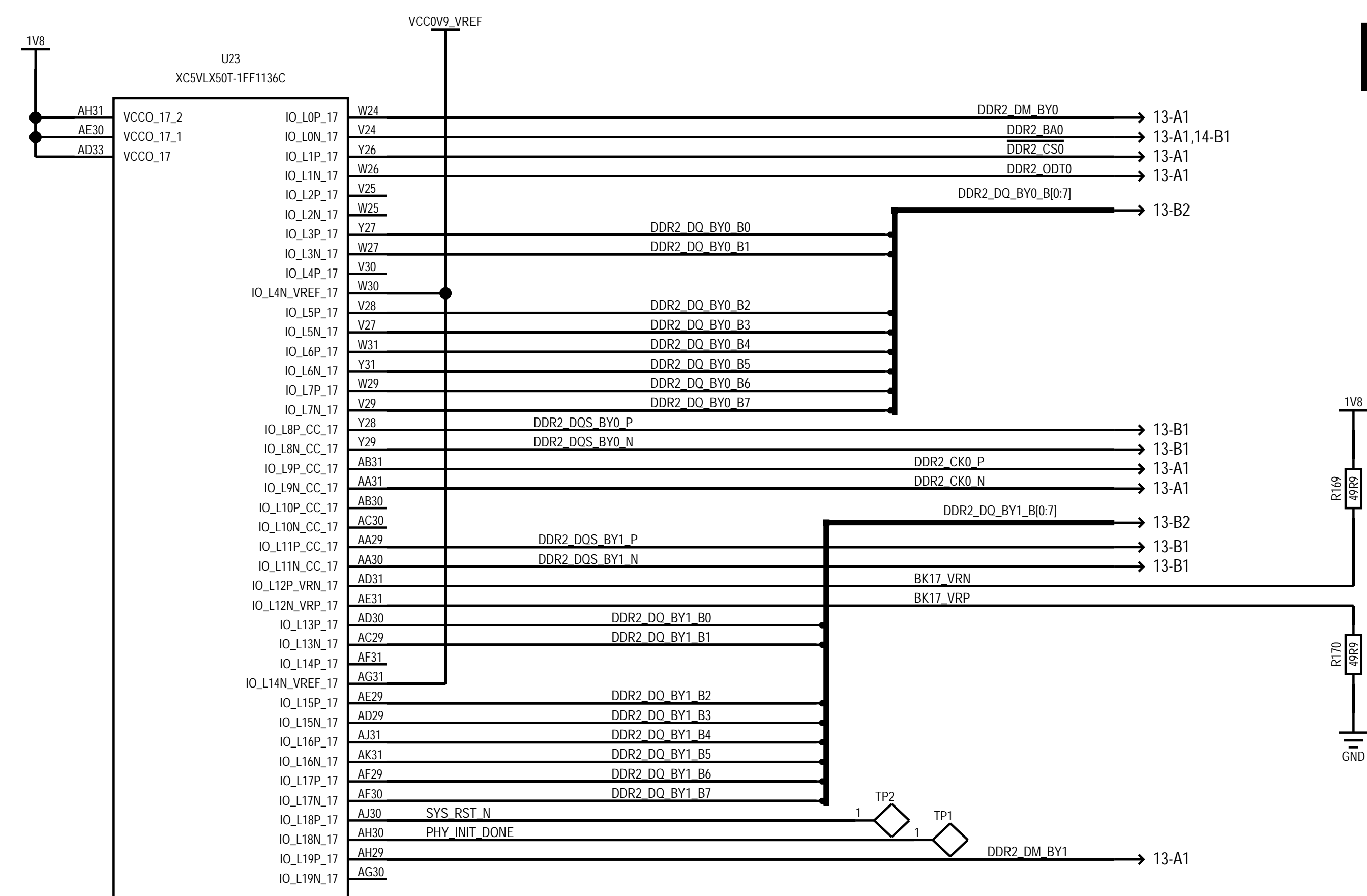


Note that DDR2 ODT does NOT act on the address/control signals, so its usually a good idea to continue to descrete terminate these signals at the memory end of the line.



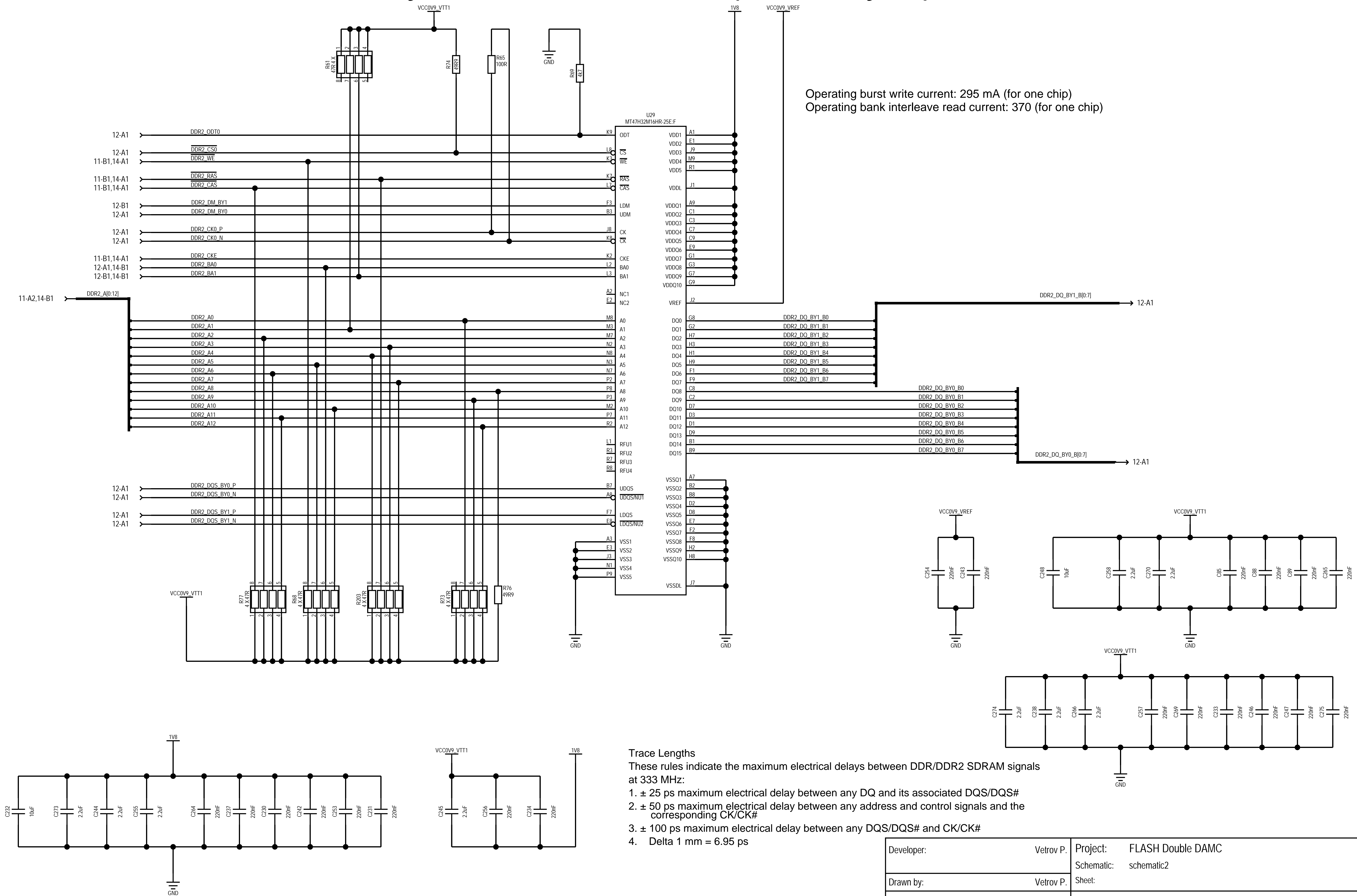
Developer:	Vetrov P.	Project:	FLASH Double DAMC
Drawn by:	Vetrov P.	Schematic:	schematic2
Layouter:	Vetrov P.	Sheet:	
Changed of sch:	Vetrov P.	DESY- FEA	Notkestrasse 85 D-22607 Hamburg
Date Changed:	07.03.2012	PCB No:	8423
Date of prod. data:		PCB name:	DAMC2_02
		Rev:	02
		Size:	A3
		Sheet:	11 of 32

# DDR2 data and control signals



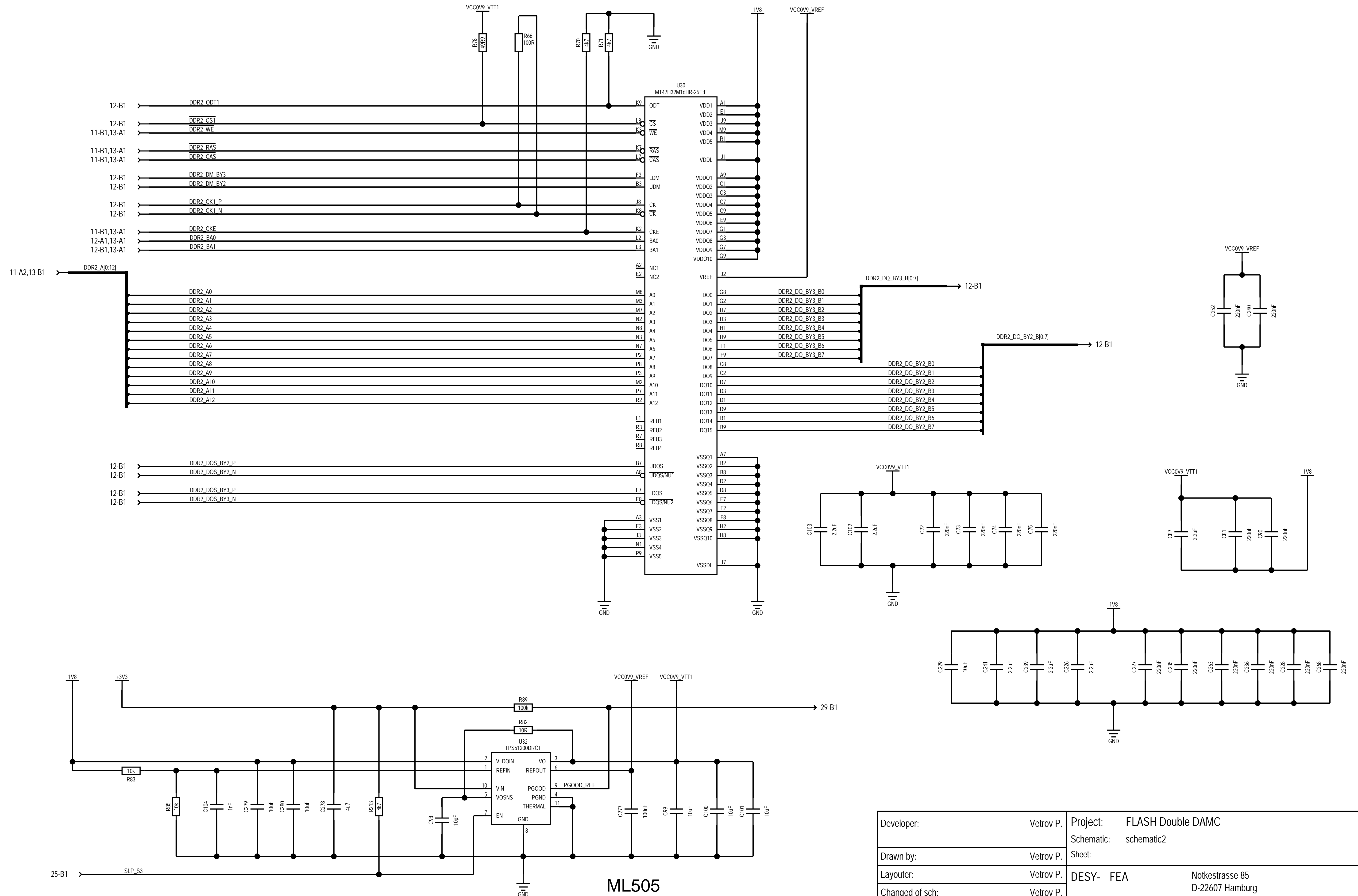
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Layer:	Vetrov P.	Sheet:	
Changed of sch:	Vetrov P.	DESIGN- FEA	Notkestrasse 85 D-22607 Hamburg
Date Changed:	07.03.2012	PCB No:	8423
Date of prod. data:		PCB name:	DAMC2_02
		Rev:	02
		Size:	A3
		Sheet:	12 of 32

# DDR2 Bytes 0&1 - ODT(64 MByte)



Developer:	Vetrov P.	Project:	FLASH Double DAMC		
		Schematic:	schematic2		
Drawn by:	Vetrov P.	Sheet:			
Layouter:	Vetrov P.	DESIGN- FEA	Notkestrasse 85 D-22607 Hamburg		
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Date Changed:	07.03.2012	PCB No:	8423	Rev:	02
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				Sheet:	13 of 32

# DDR2 Bytes 2&3 - ODT (+64MByte)



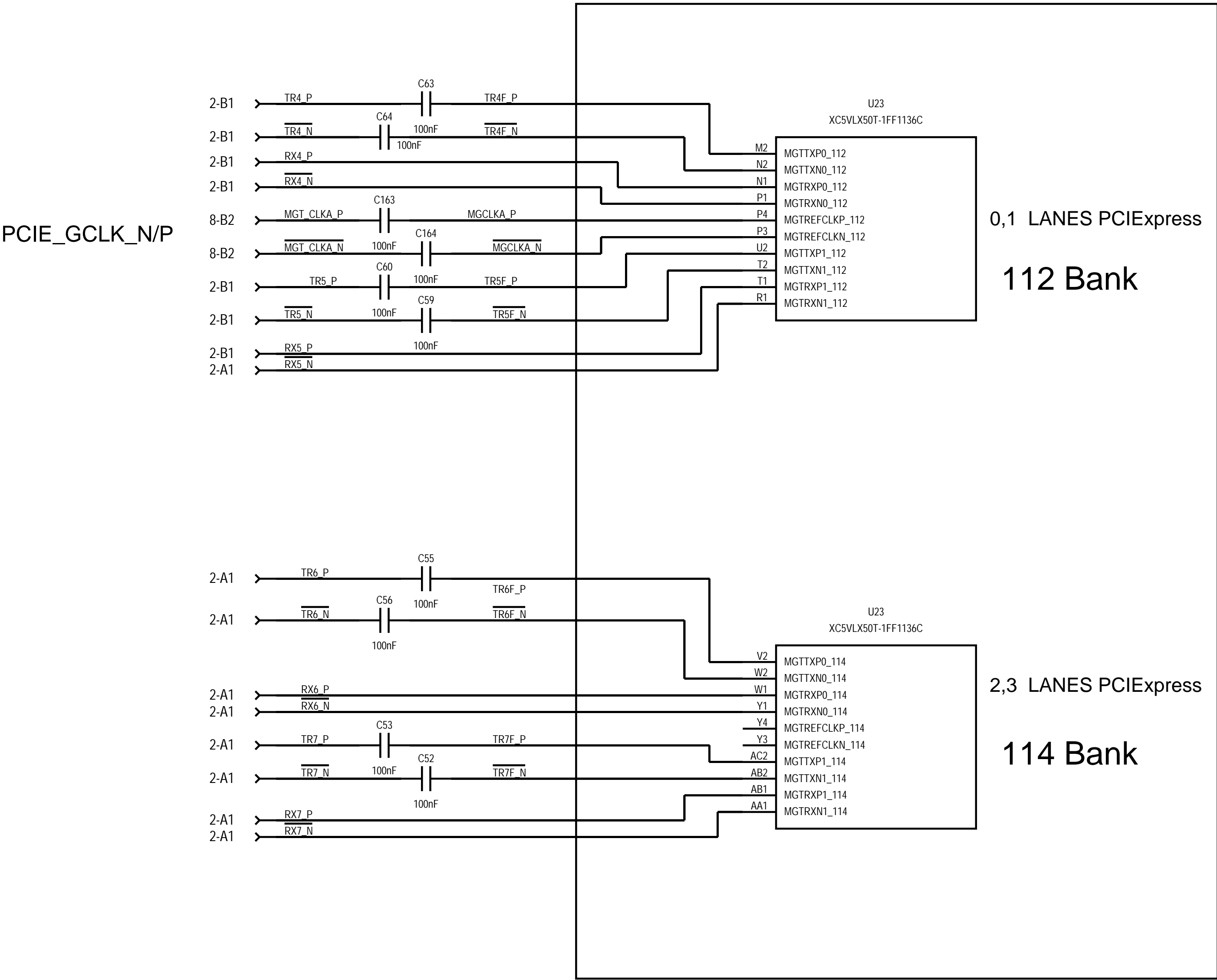
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		Schematic: schematic2					
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Layouter:	Vetrov P.	DESY- FEA Notkestrasse 85 D-22607 Hamburg					
Changed of sch:	Vetrov P.						
Date Changed:	07.03.2012	PCB No:	8423	Rev:	02	Size:	A3
Date of prod. data:		PCB name:	DAMC2_02	Sheet:	14	of	32

A
B
C
D
E
F





# 4 LANES PCIExpress to back plane



FOR GTP reference clock total jitter, peak-peak < 40 ps

Min. output clock jitter for VIRTEX-5 120 ps

AVCC 1.0V - 110mA per DUAL\_GTP= 0.66A

AVCCPLL 1.2V - 60mA per DUAL\_GTP = 0.36A

AVTTTX 1.2V - 90mA per DUAL\_GTP = 0.09A \* 6 = 0.54 A

AVTTRX 1.2V - 50mA per DUAL\_GTP = 0.003A

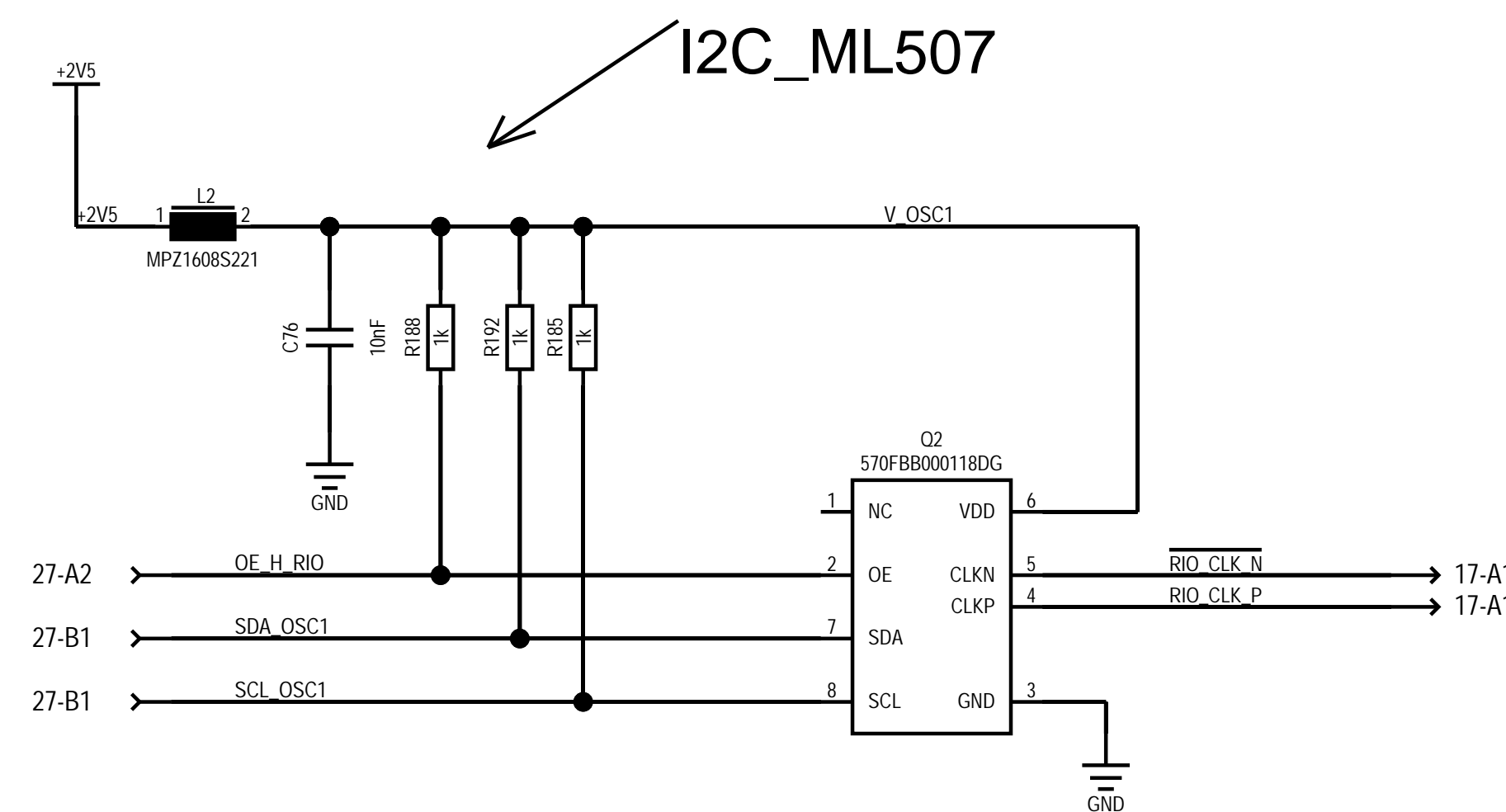
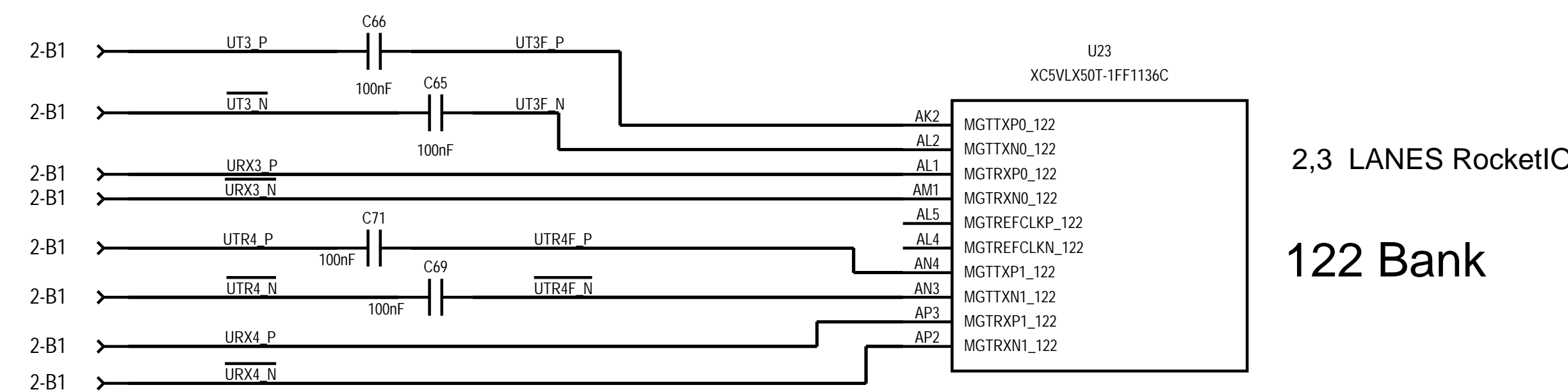
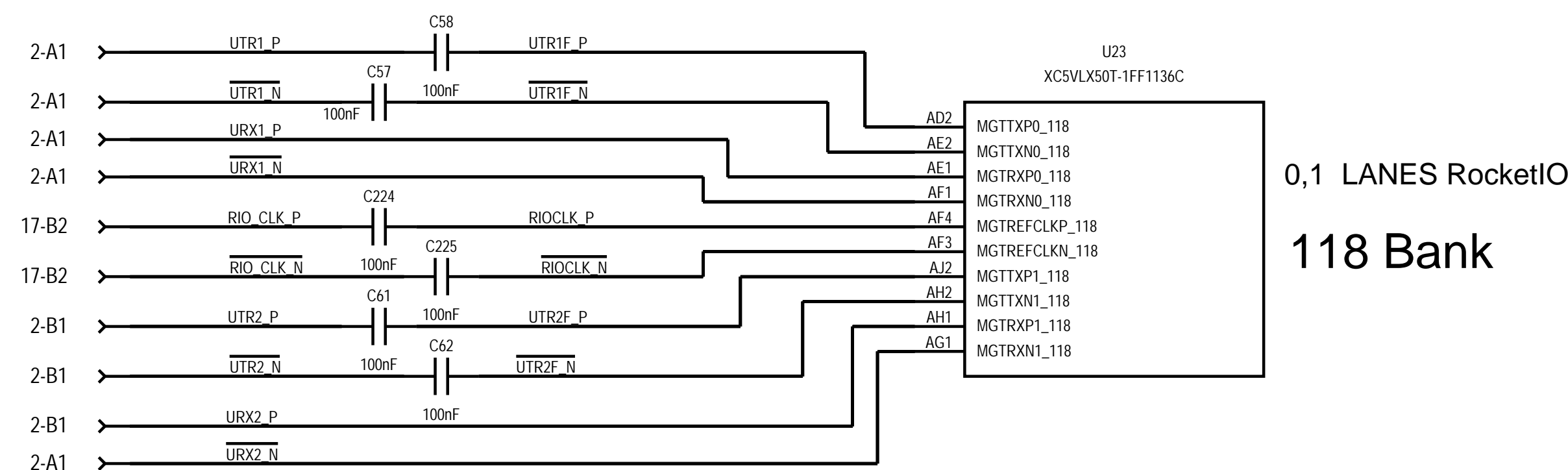
AVTTTRXC 1.2V - 0.5mA per DUAL\_GTP = 0.003A

One Regulator = 1.152 A

Look\_DS202

Developer:	Vetrov P.	Project:	FLASH Double DAMC			
		Schematic:	schematic2			
Drawn by:	Vetrov P.	Sheet:				
Layouter:	Vetrov P.	DESIGN- FEA	Notkestrasse 85			
Changed of sch:	Vetrov P.		D-22607 Hamburg			
Date Changed:	07.03.2012	PCB No:	8423	Rev:	02	Size: A3
Date of prod. data:		PCB name:	DAMC2_02	Sheet:	16 of	32

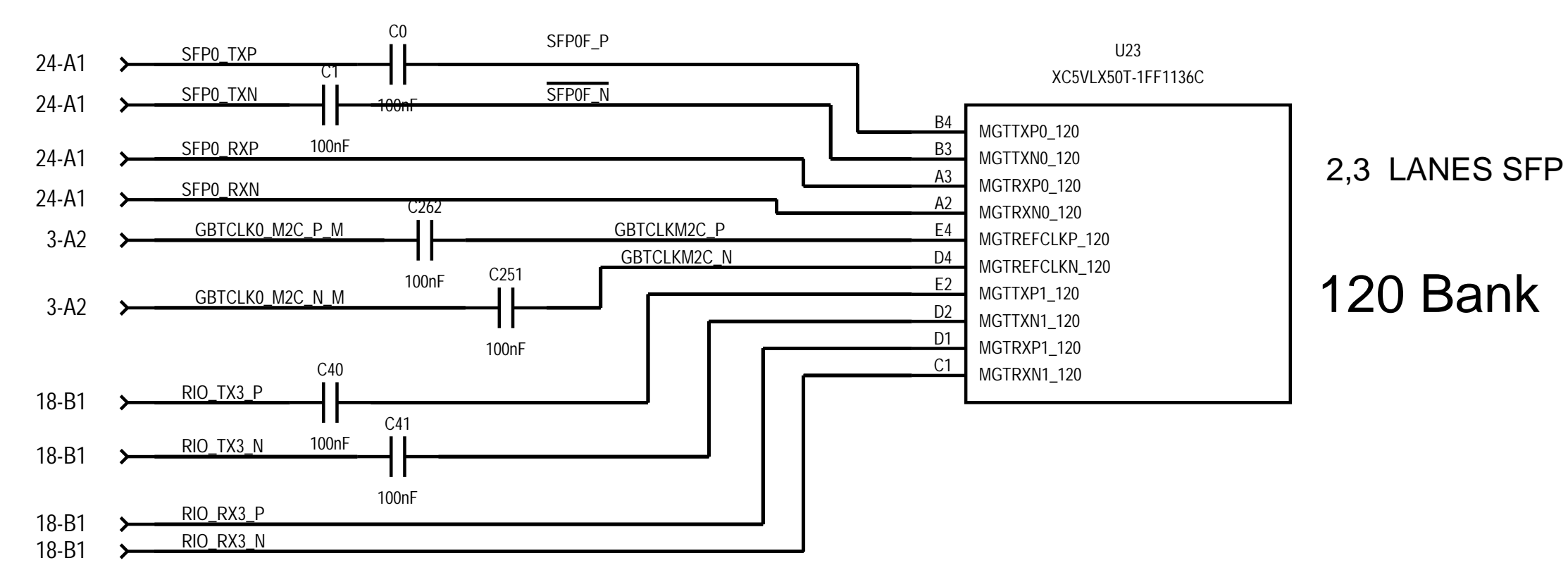
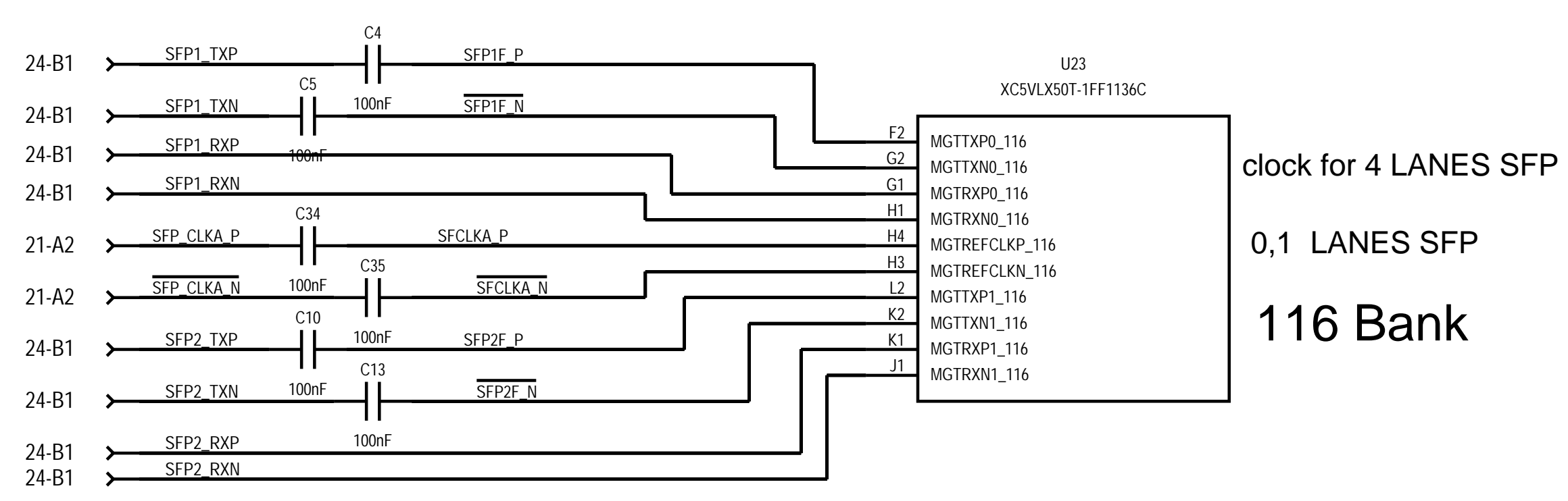
# 4 LANES to EDGE Connector - Ports 12-15



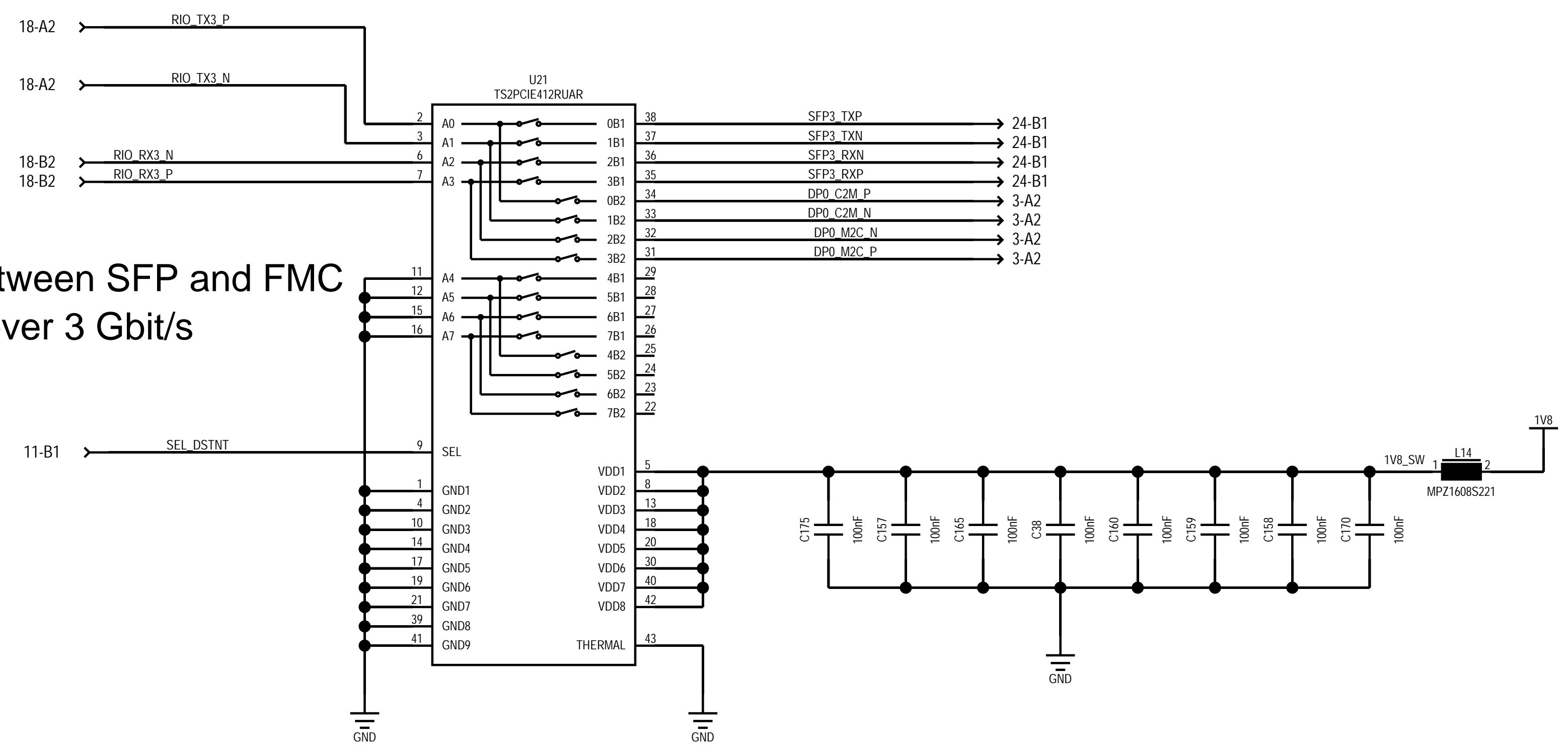
PART NUMBER: 570FBB000118DG  
OSCILLATOR SPECIFICATION SUMMARY  
Model Number: Si570 (Programmable XO)  
Output Format: LVDS VDD: 2.5V  
Output Enable Polarity: OE active high  
Temperature Stability: +/- 20 ppm  
Frequency Range: 10 - 810 MHz  
Startup Frequency (MHz): 156.250000  
I2C Address: 55 hex (85 decimal)  
Operating Temperature Range (°C): -40 to +85  
Datasheet: si570\_si571.pdf

Developer:	Vetrov P.	Project:	FLASH Double DAMC				
		Schematic:	schematic2				
Drawn by:	Vetrov P.	Sheet:					
Layouter:	Vetrov P.	DESY- FEA	Notkestrasse 85 D-22607 Hamburg				
Changed of sch:	Vetrov P.						
Date Changed:	07.03.2012	PCB No:	8423	Rev:	02	Size:	A3
Date of prod. data:		PCB name:	DAMC2_02	Sheet:	17	of	32

# 3 Lanes to SFP connectors and one to SFP or to FMC



SWITCH between SFP and FMC  
Bandwidth over 3 Gbit/s

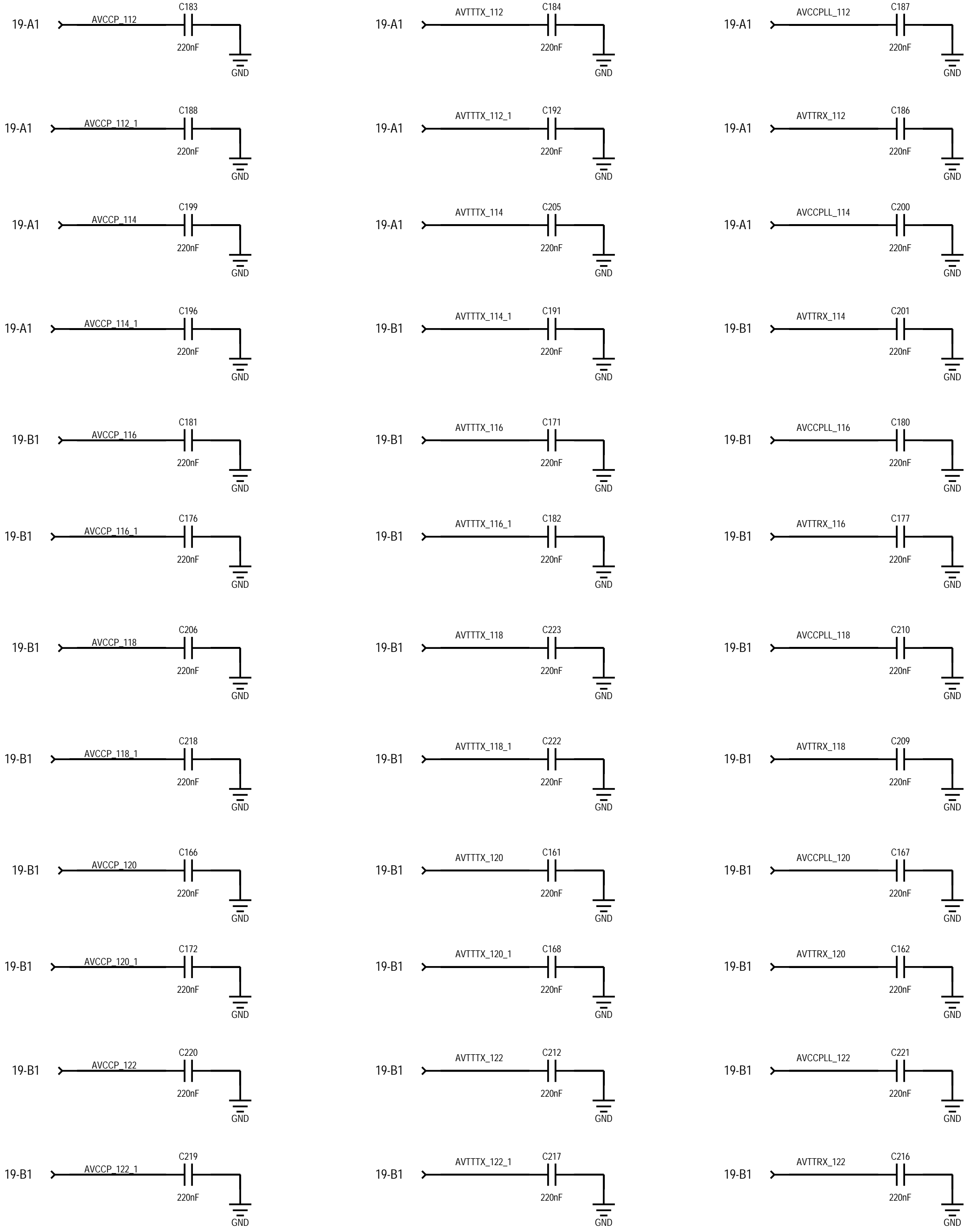
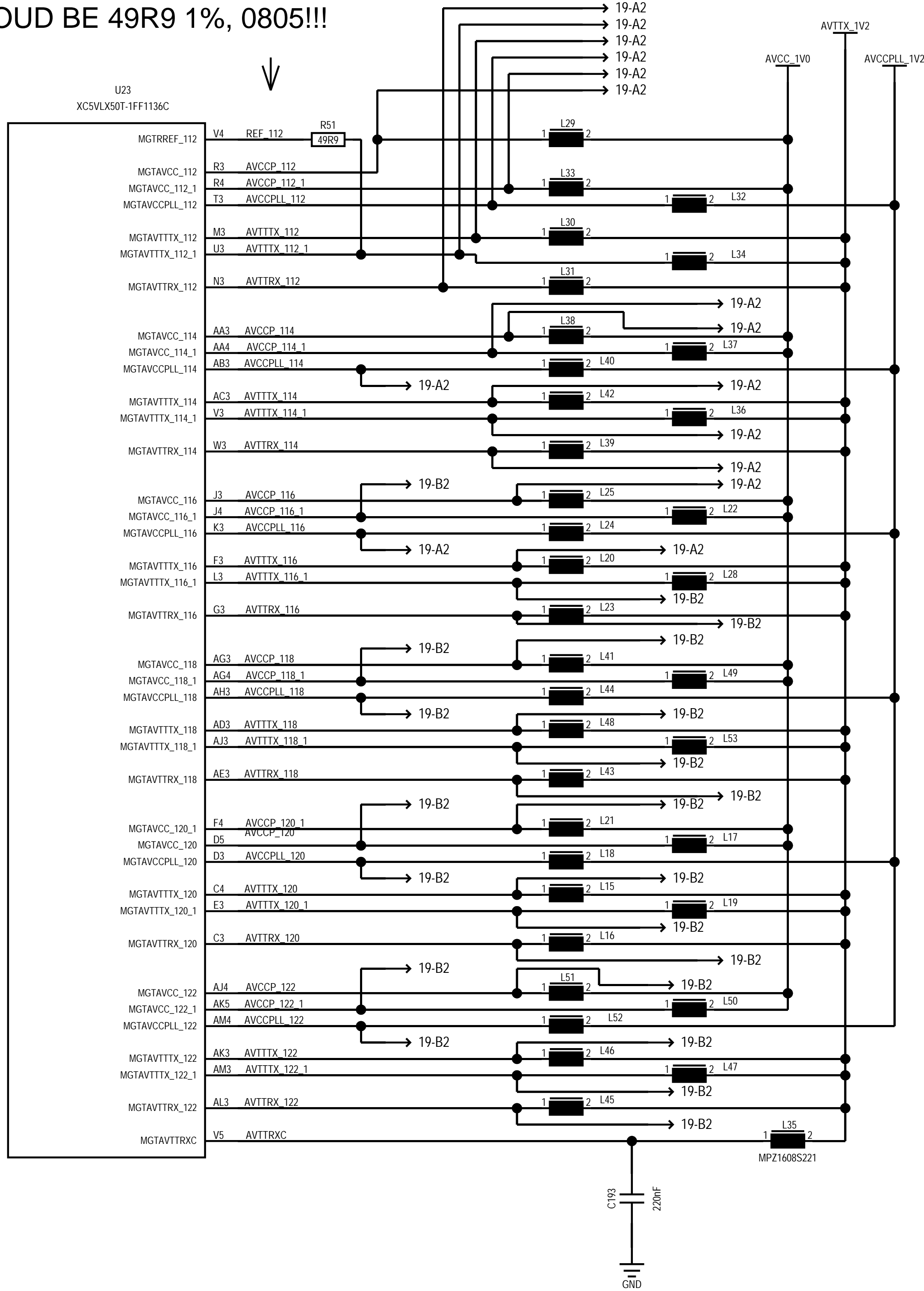


Reference clock needs to arrive at one of the GTP tiles chosen in the design and routed to the other GTP tiles. The reference clock arriving at one GTP tile can be routed to any other GTP tile that is up to three GTP tiles away in either the north or south direction. The GTP

Developer:	Vetrov P.	Project:	FLASH Double DAMC
Drawn by:	Vetrov P.	Schematic:	schematic2
Layouter:	Vetrov P.	Sheet:	
Changed of sch:	Vetrov P.	DESY- FEA	Notkestrasse 85 D-22607 Hamburg
Date Changed:	07.03.2012	PCB No:	8423
Date of prod. data:		PCB name:	DAMC2_02
		Rev:	02
		Size:	A3
		Sheet:	18 of 32

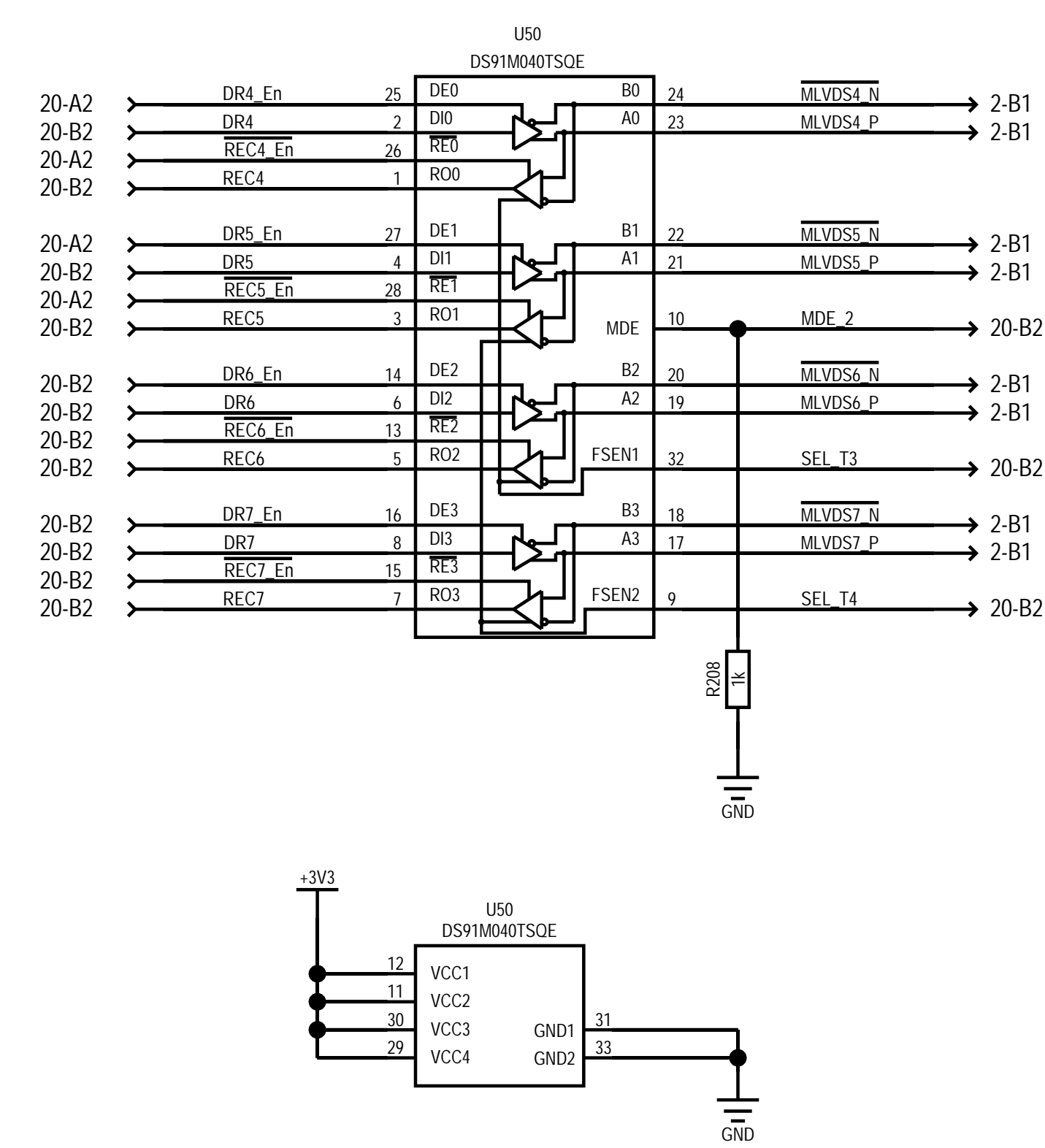
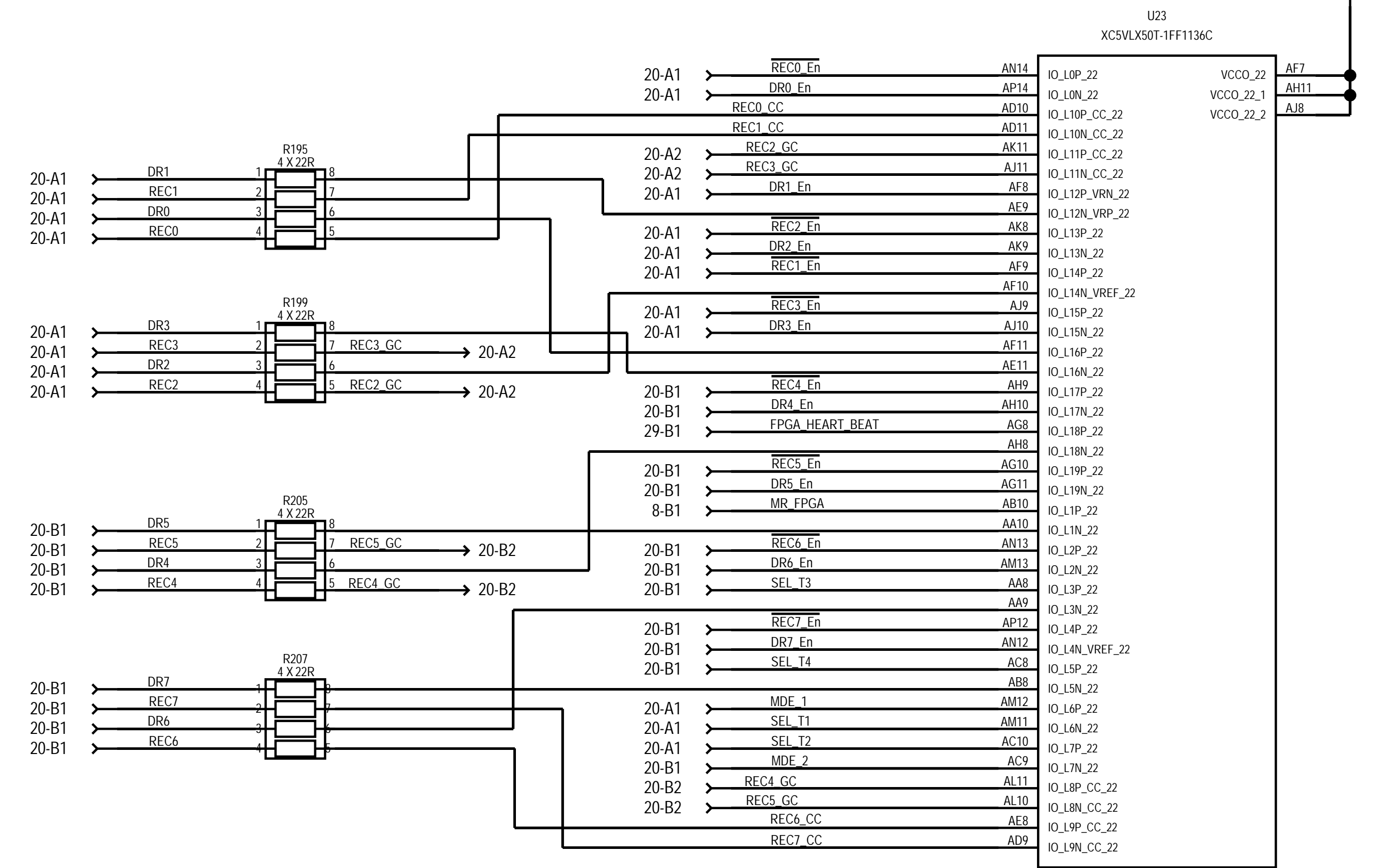
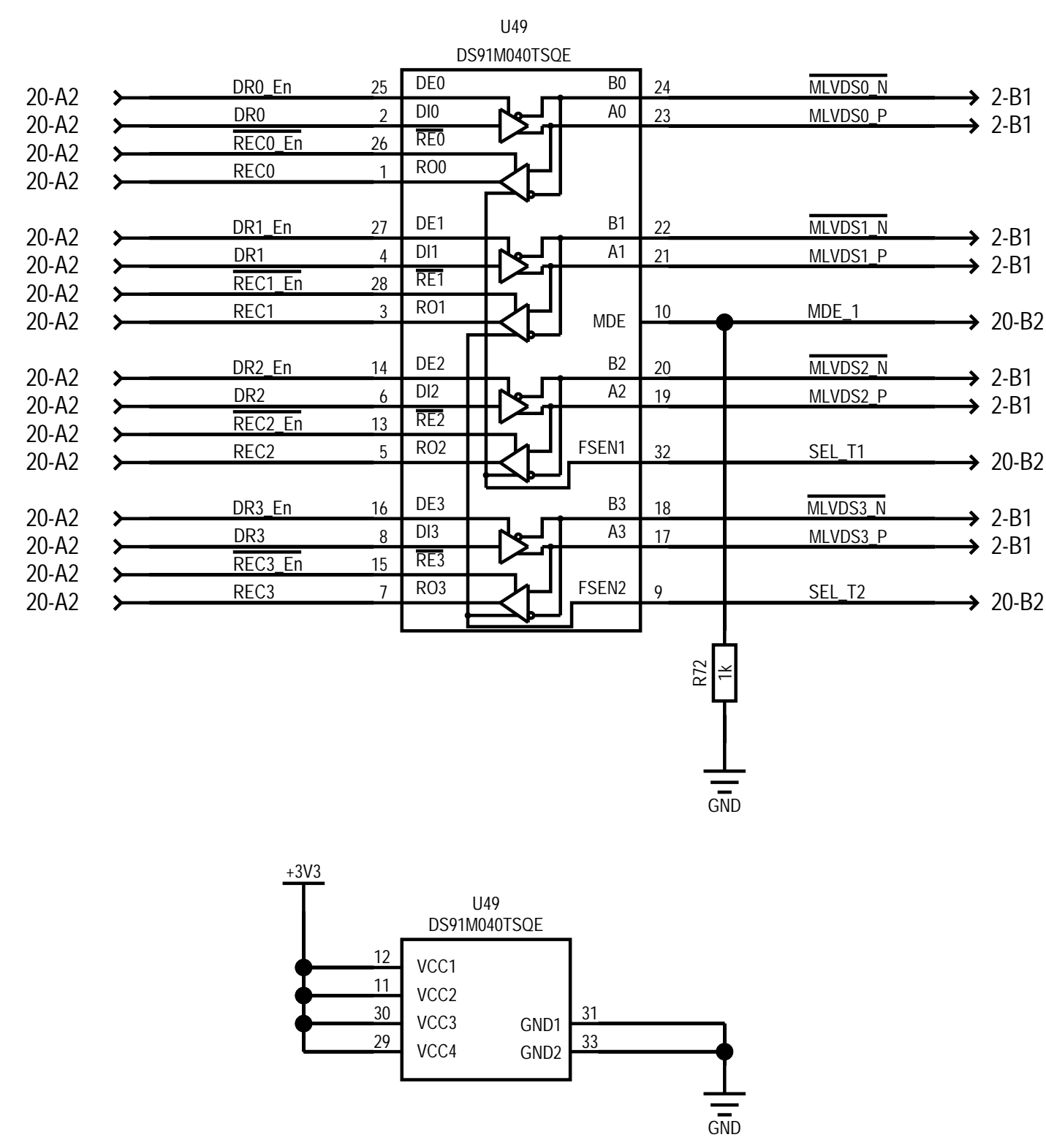
# Powers for GTP and GTP\_SWITCH

IT SHOUD BE 49R9 1%, 0805!!!

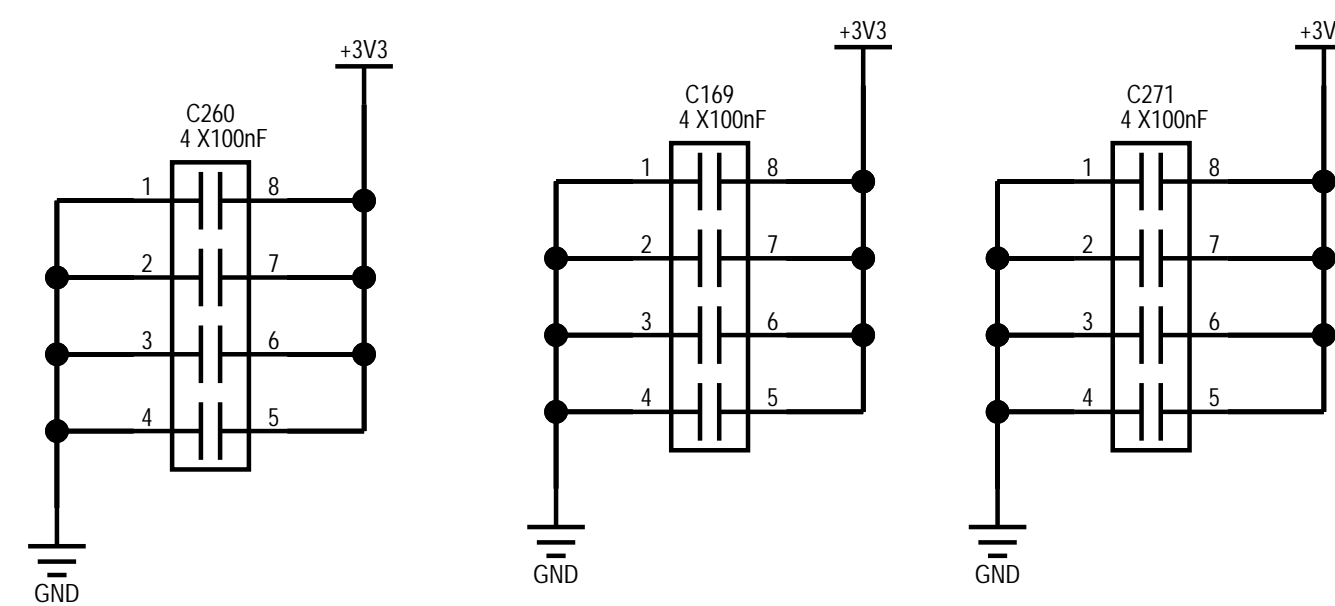


Developer:	Vetrov P.	Project:	FLASH Double DAMC		
Drawn by:	Vetrov P.	Schematic:	schematic2		
Layouter:	Vetrov P.	Sheet:			
Changed of sch:	Vetrov P.	DESY- FEA	Notkestrasse 85 D-22607 Hamburg		
Date Changed:	07.03.2012	PCB No:	8423	Rev:	02
Date of prod. data:		PCB name:	DAMC2_02	Size:	A3
		Sheet:	19 of 32		

# MLVDS bus to Edge Connector



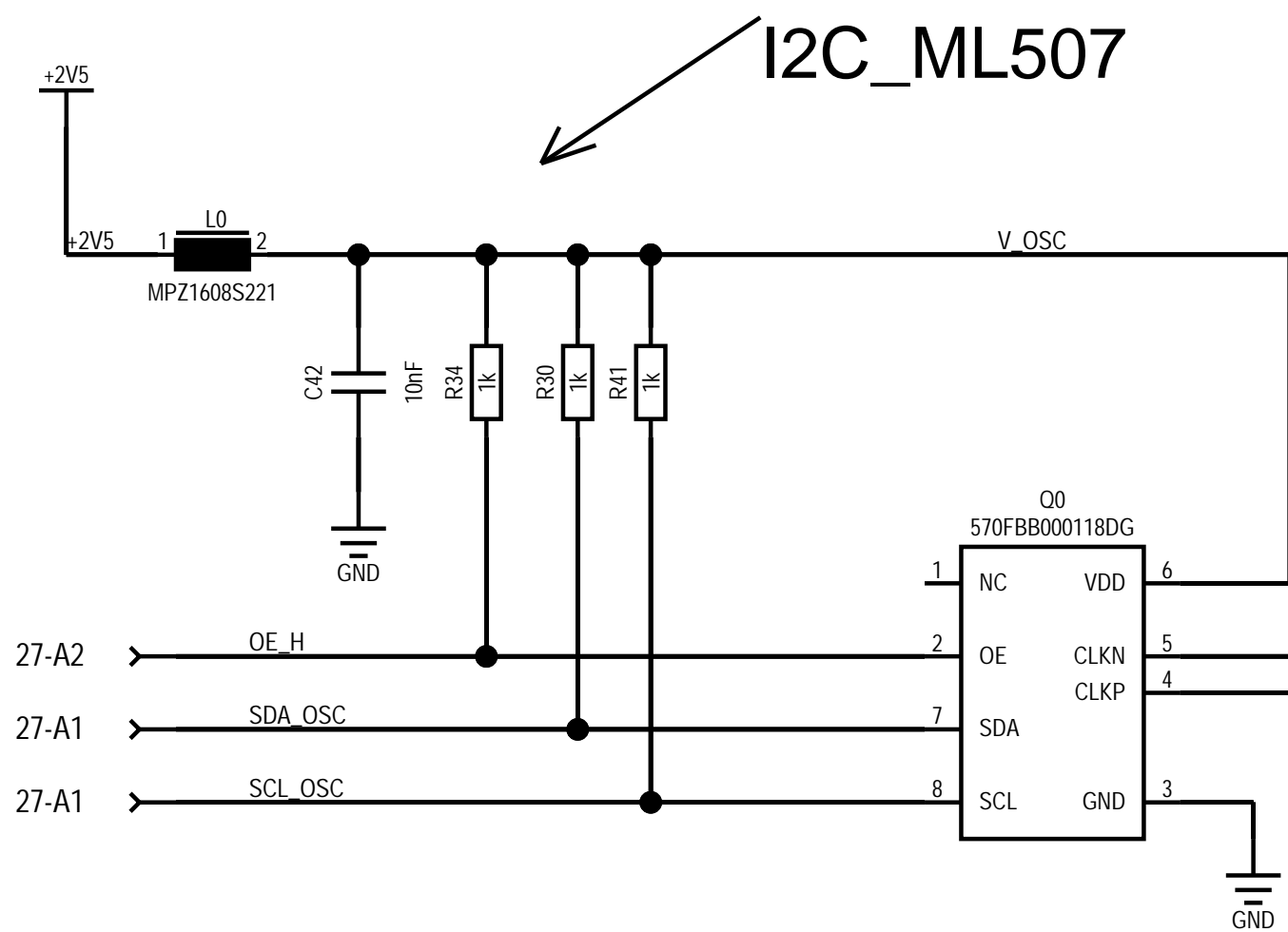
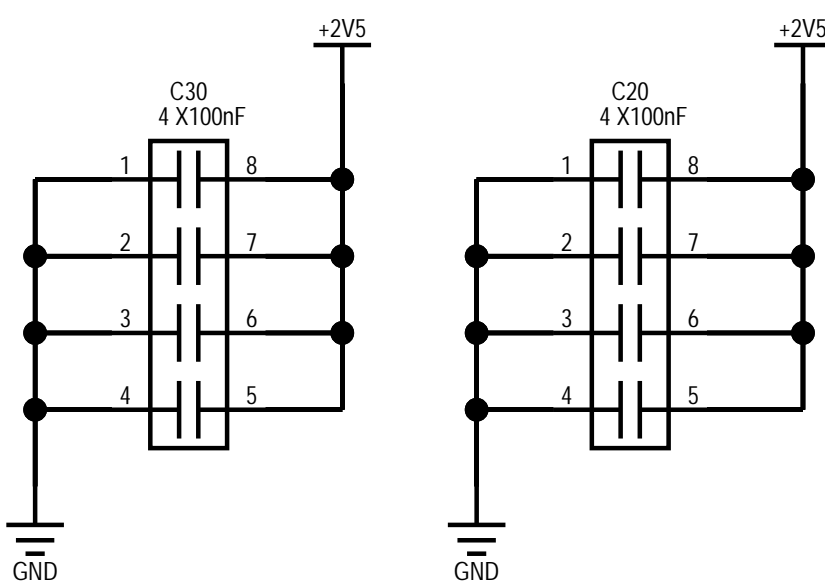
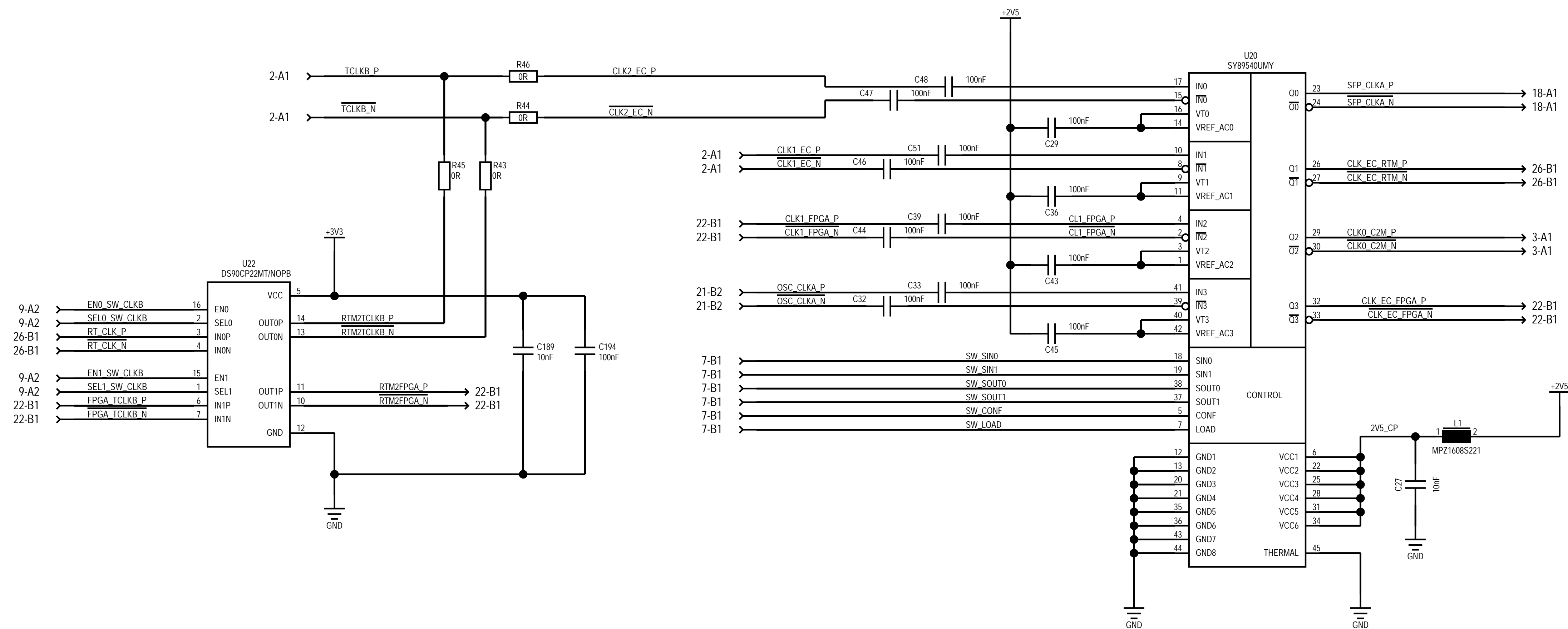
Connect signals Port\_RX to local clock - input "P"!  
Connect signals Port\_TX to local clock - input "N"!



Developer:	Vetrov P.	Project:	FLASH Double DAMC
Drawn by:	Vetrov P.	Schematic:	schematic2
Layouter:	Vetrov P.	Sheet:	
Changed of sch:	Vetrov P.	DESIGN- FEA	Notkestrasse 85 D-22607 Hamburg
Date Changed:	07.03.2012	PCB No:	8423
Date of prod. data:		PCB name:	DAMC2_02
		Rev:	02
		Size:	A3
		Sheet:	20 of 32

# LOW JITTER CLOCK Crosspoint Switch

Ultra Low Jitter design: < 10 ps deterministic jitter



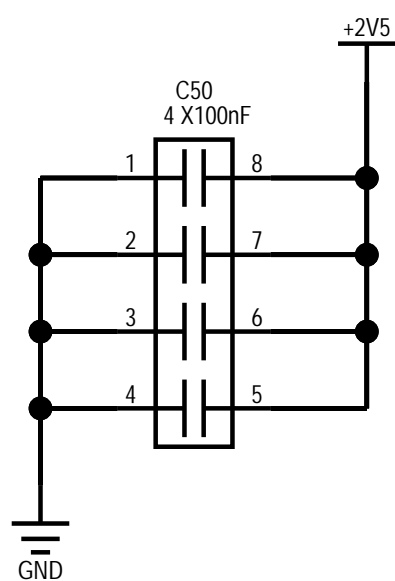
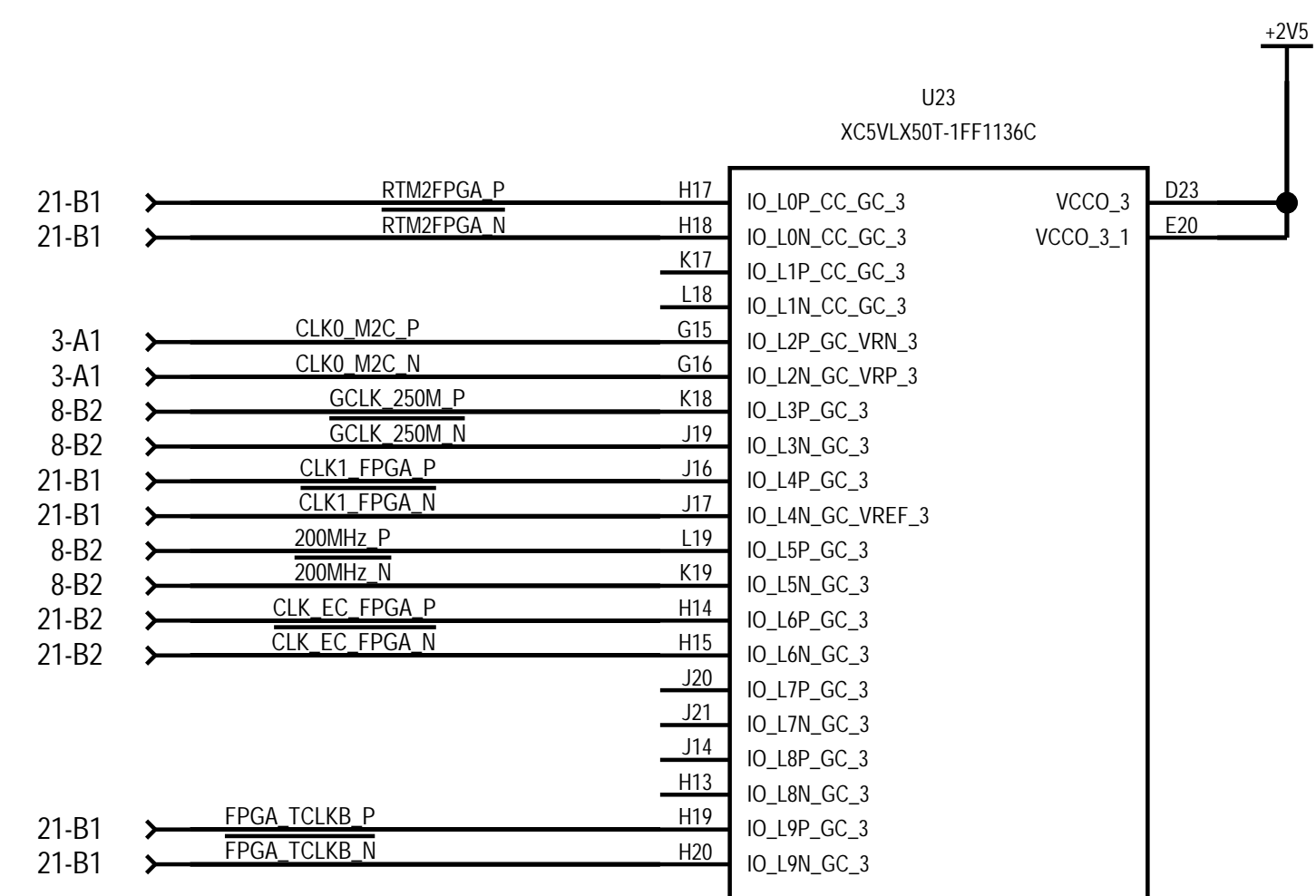
570FBB000118DG SMD Crystal Oscillator 156.25MHz

Any-rate programmable output  
frequencies from 10 to 945 MHz and  
select frequencies to 1.4 GHz

Frequency Range Supported (MHz): 10 - 810

Developer:	Vetrov P.	Project:	FLASH Double DAMC		
		Schematic:	schematic2		
Drawn by:	Vetrov P.	Sheet:			
Layouter:	Vetrov P.	DESY- FEA	Notkestrasse 85 D-22607 Hamburg		
Changed of sch:	Vetrov P.				
Date Changed:	07.03.2012	PCB No:	8423	Rev:	02
Date of prod. data:		PCB name:	DAMC2_02	Size:	A3
		Sheet:	21	of	32

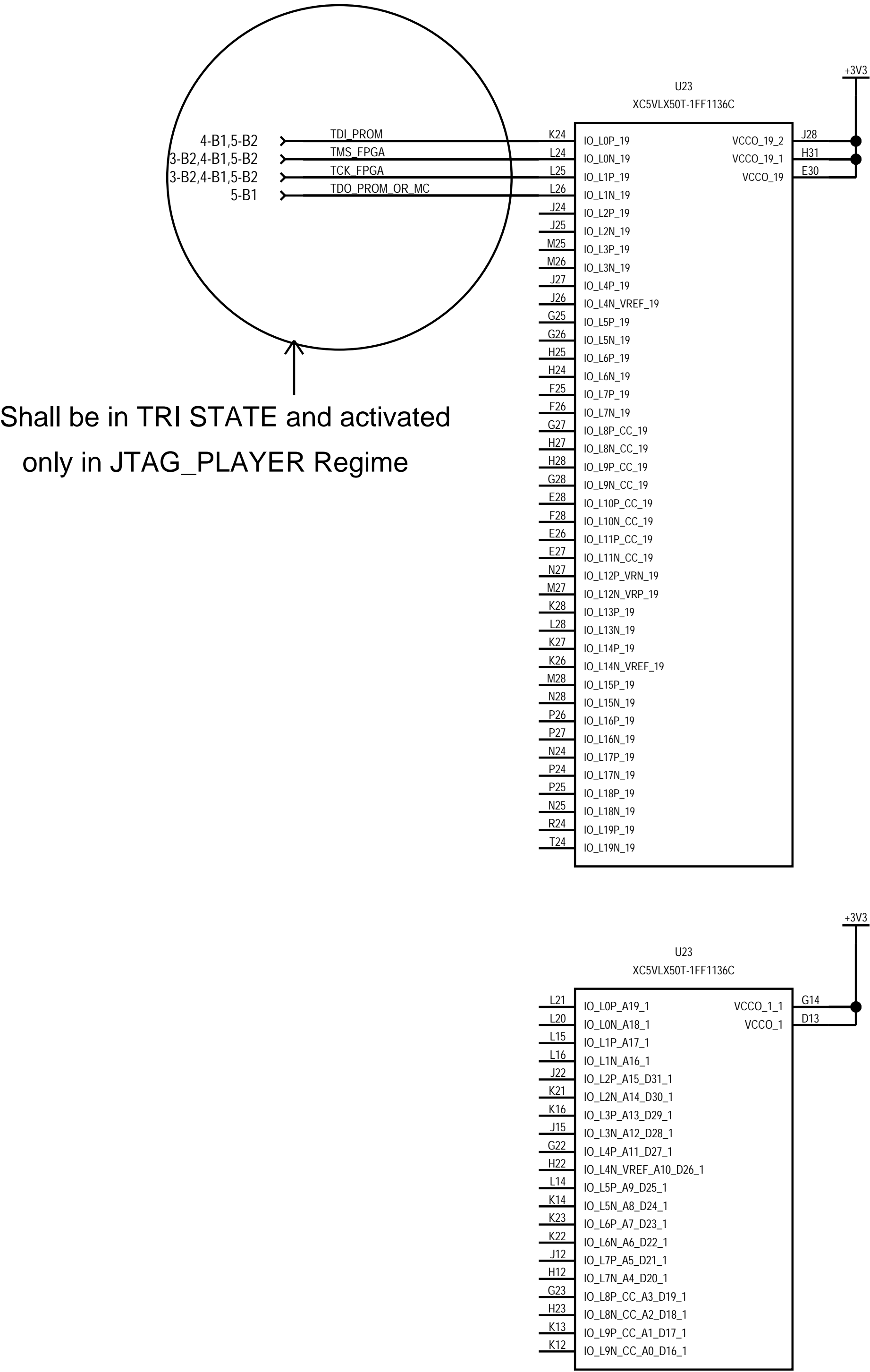
# GLOBAL CLOCKS



Developer:	Vetrov P.	Project:	FLASH Double DAMC		
		Schematic:	schematic2		
Drawn by:	Vetrov P.	Sheet:			
Layouter:	Vetrov P.	DESIGN- FEA	Notkestrasse 85		
Changed of sch:	Vetrov P.		D-22607 Hamburg		
Date Changed:	07.03.2012	PCB No:	8423	Rev:	02
Date of prod. data:		PCB name:	DAMC2_02	Size:	A3
				Sheet:	22 of 32

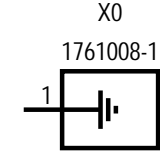
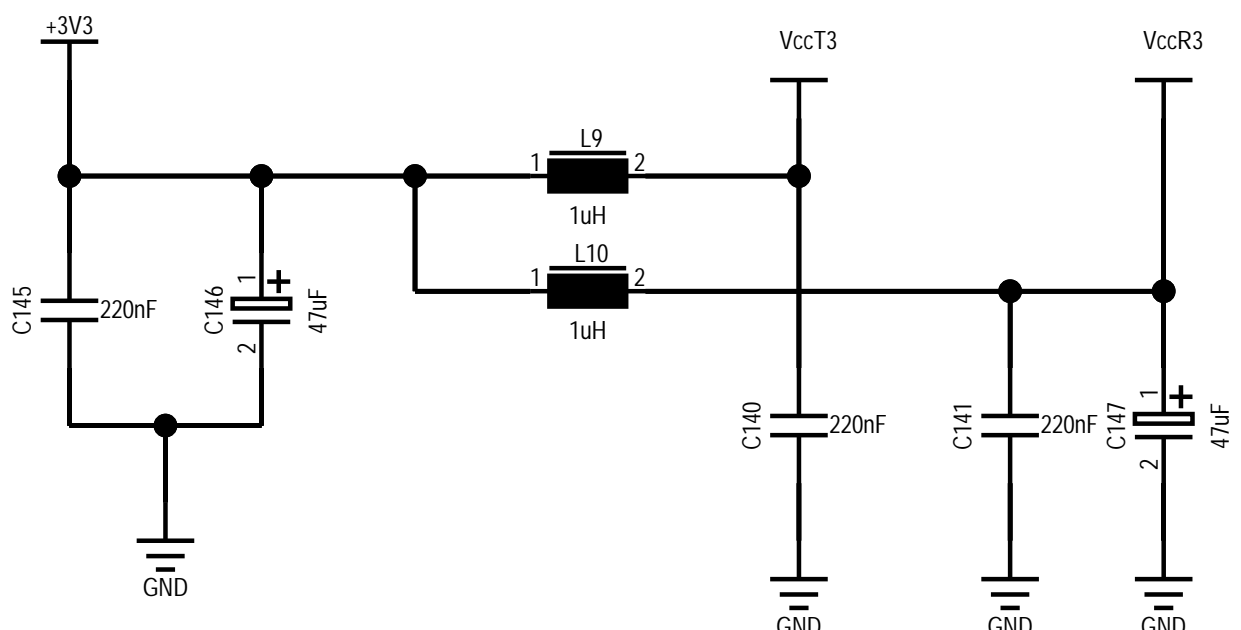
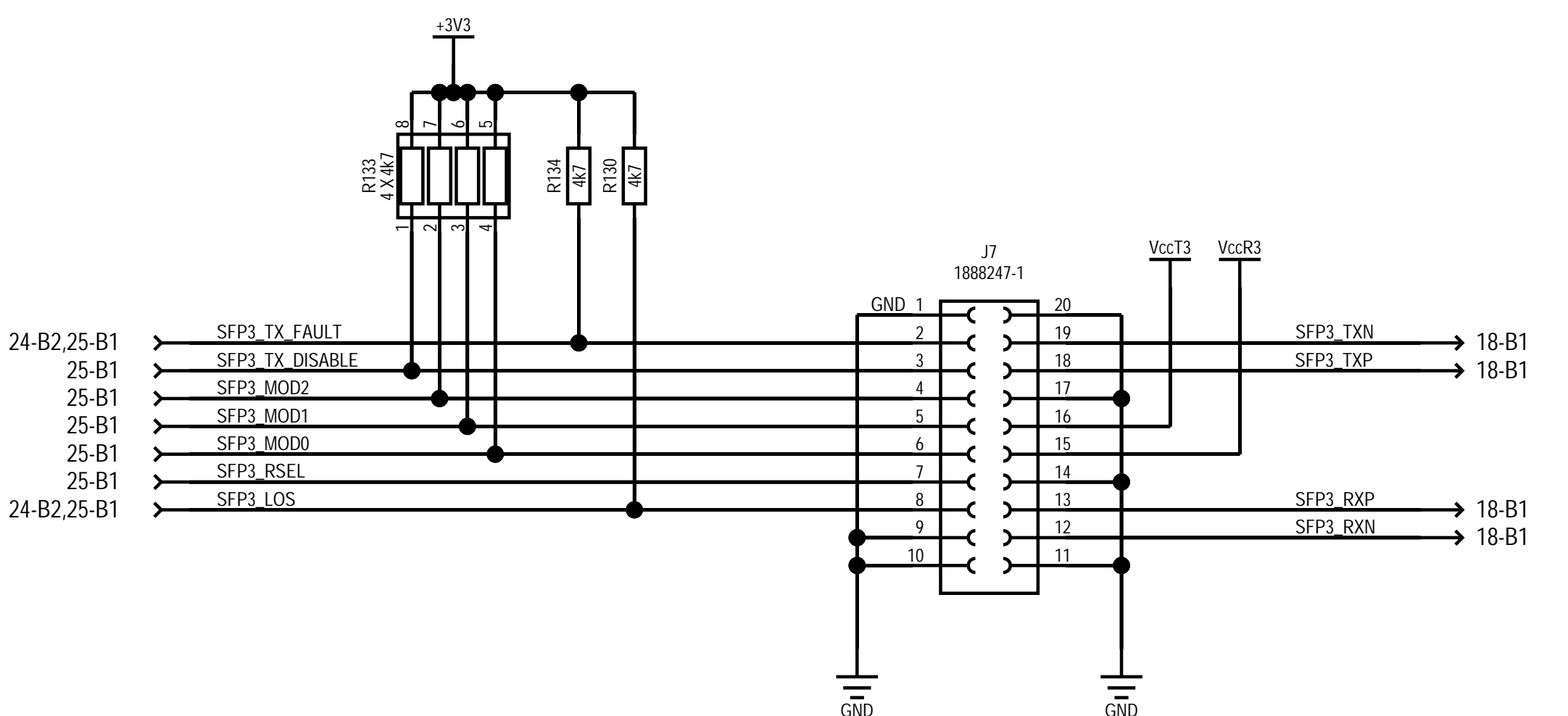
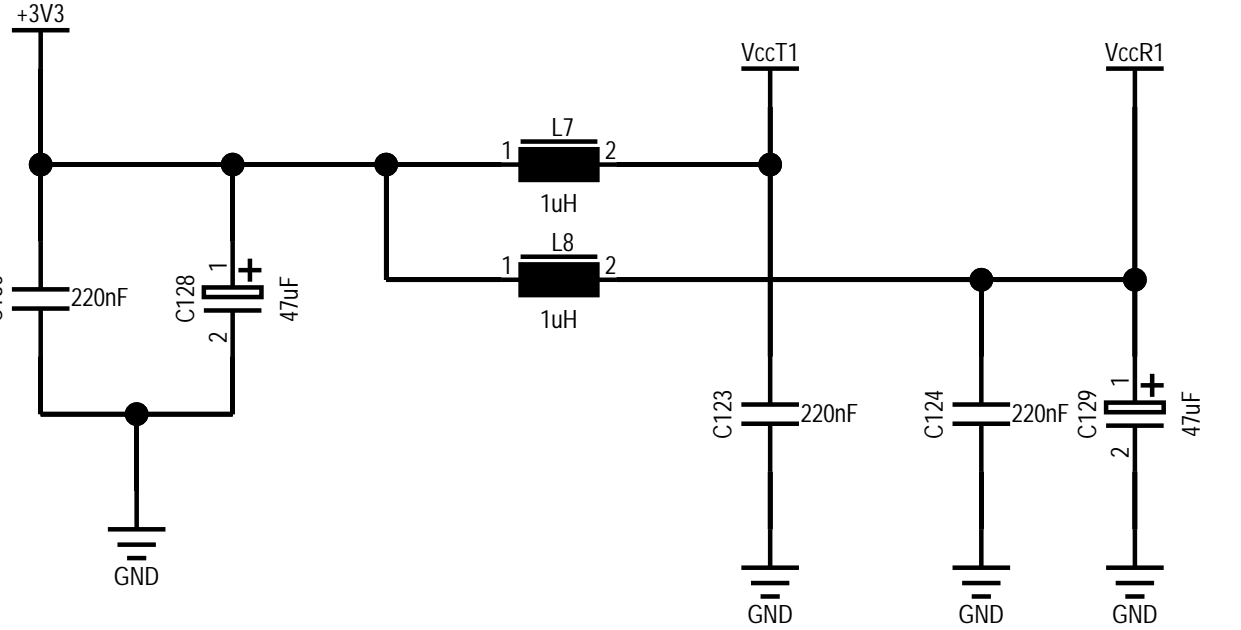
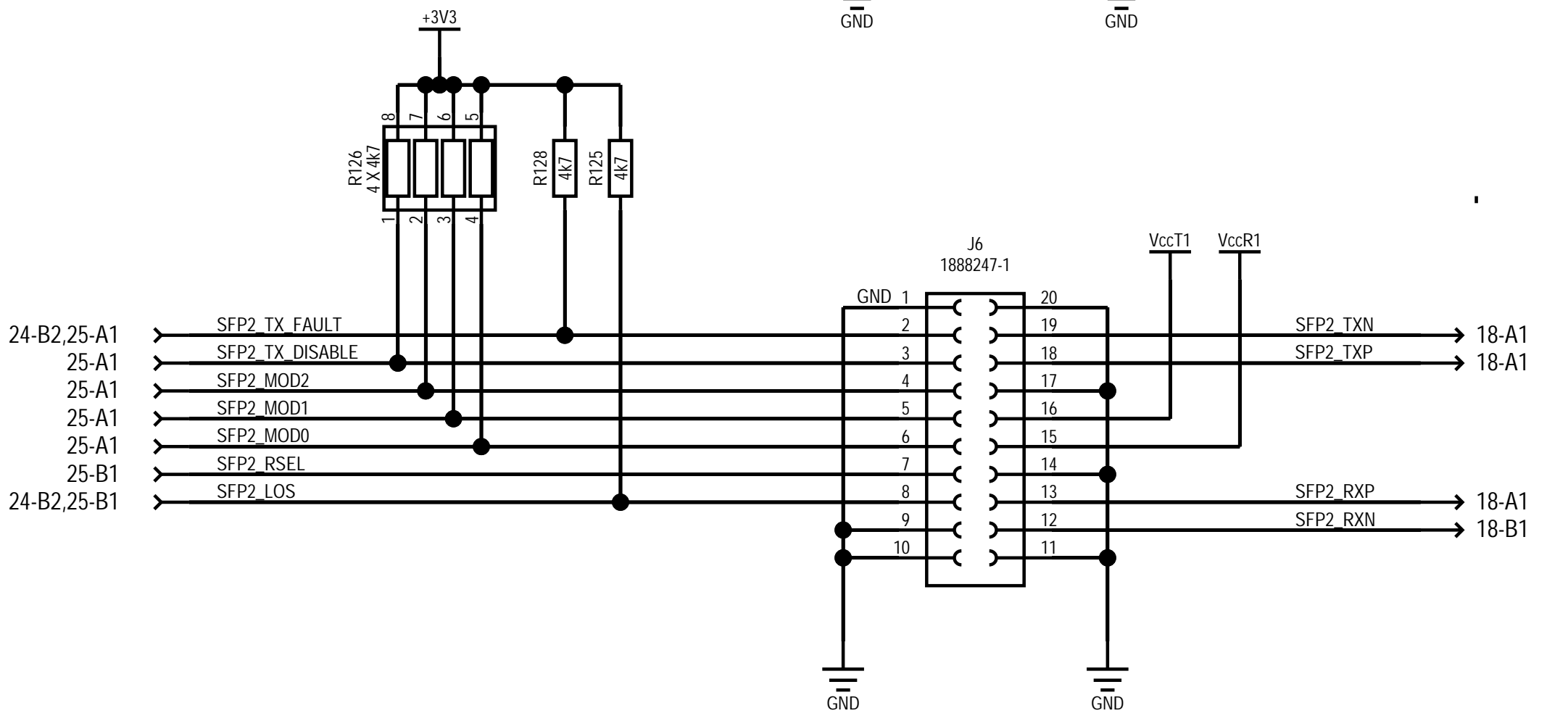
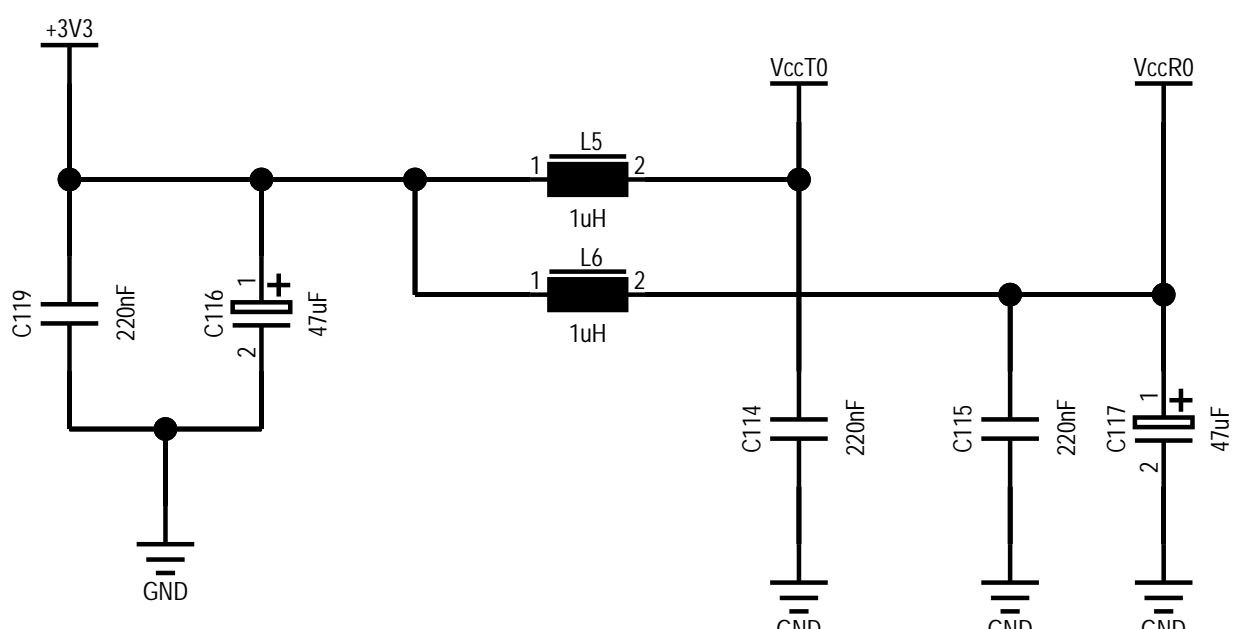
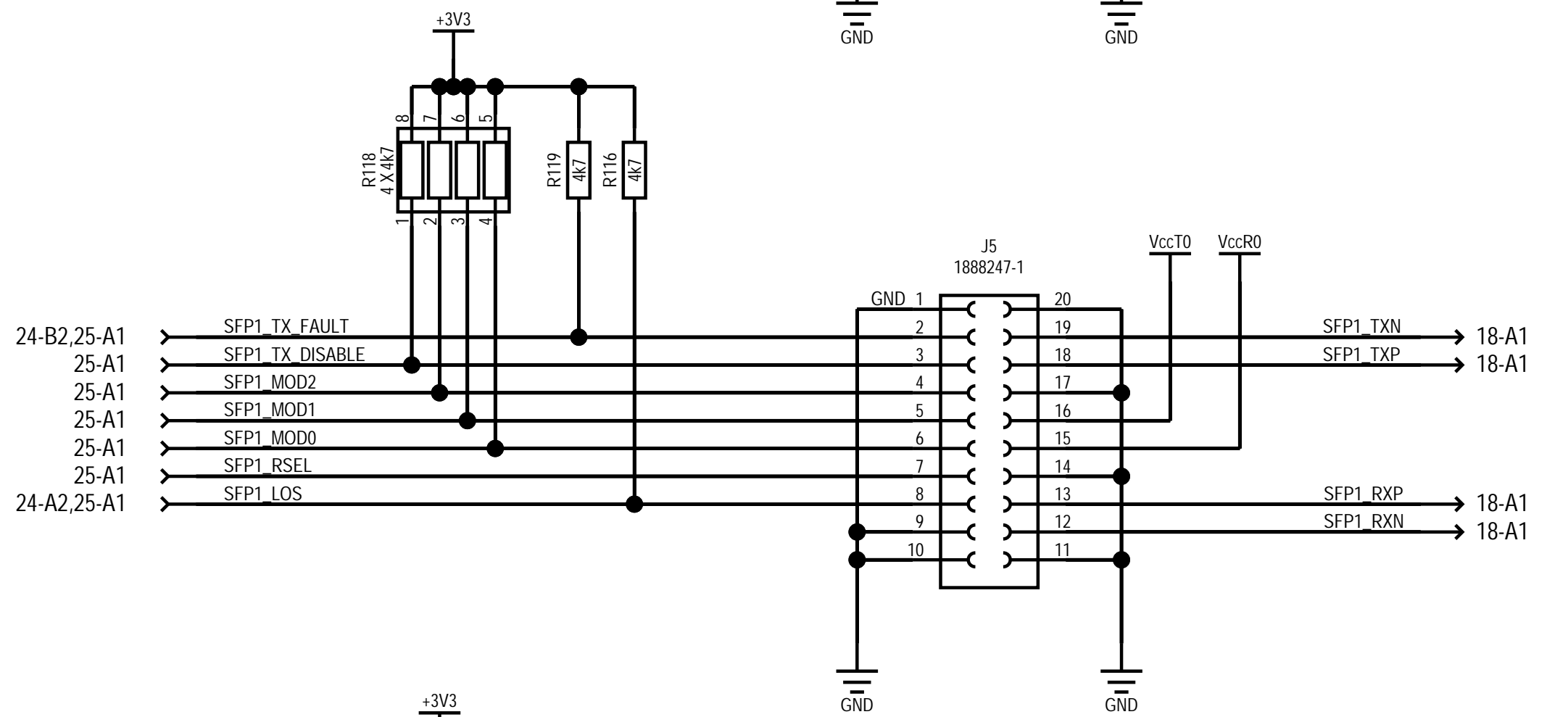
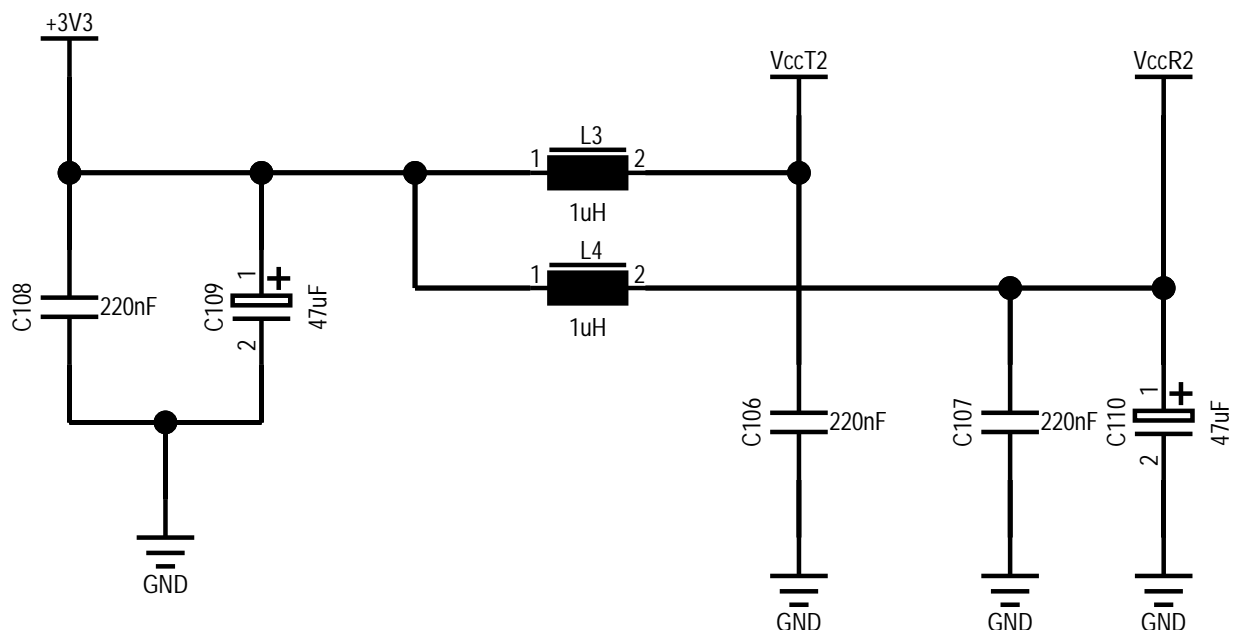
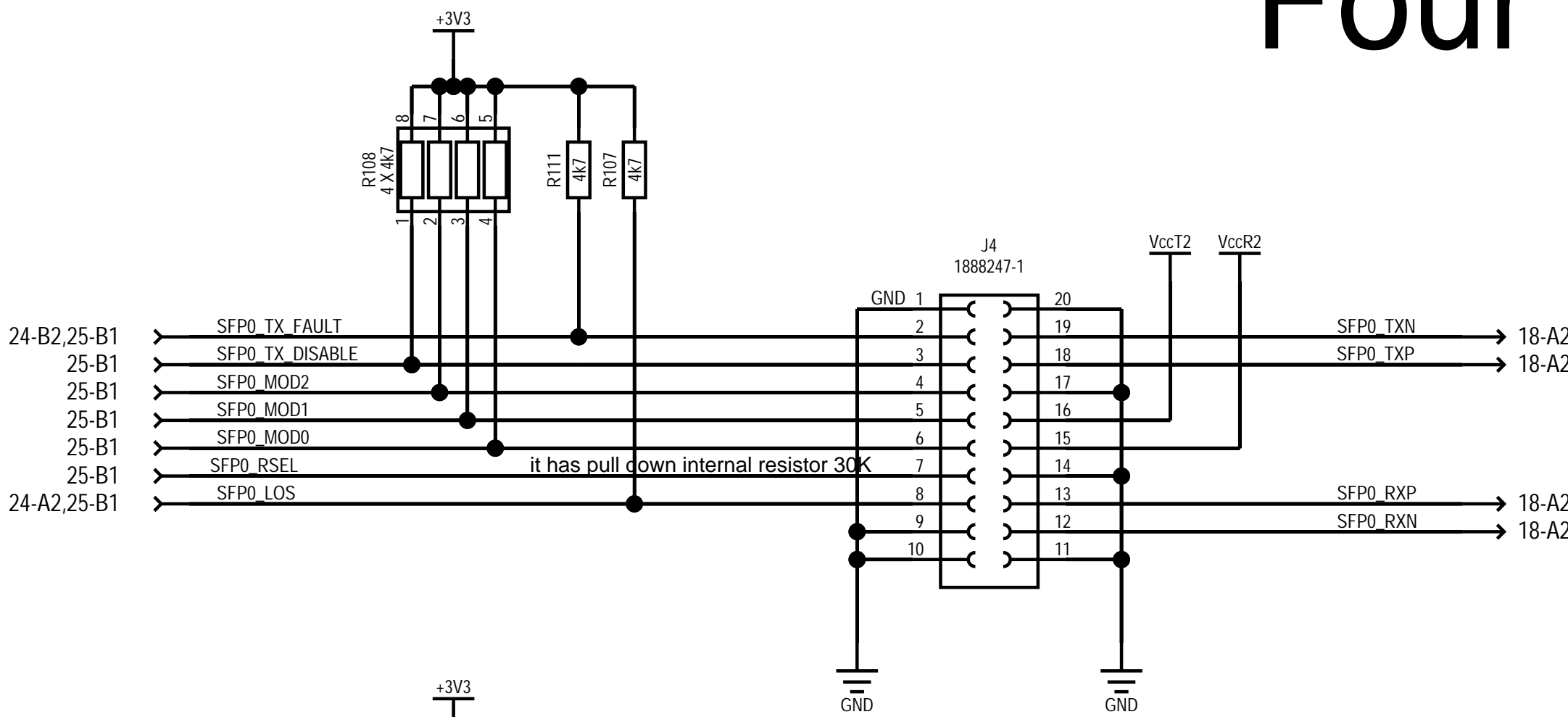


SPARE VIRTEX-5 BANKS

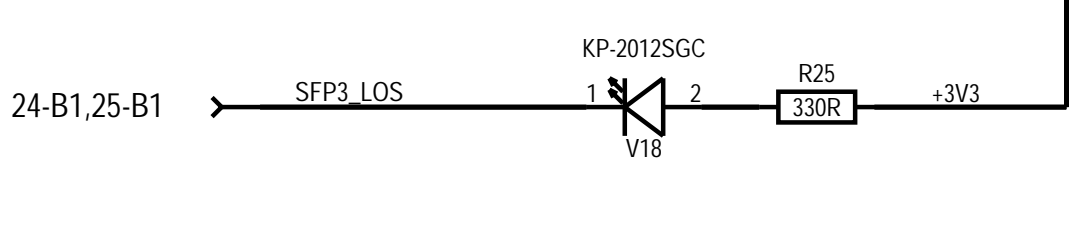
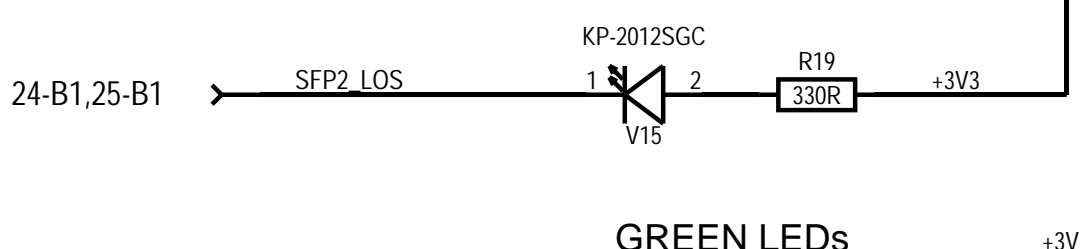
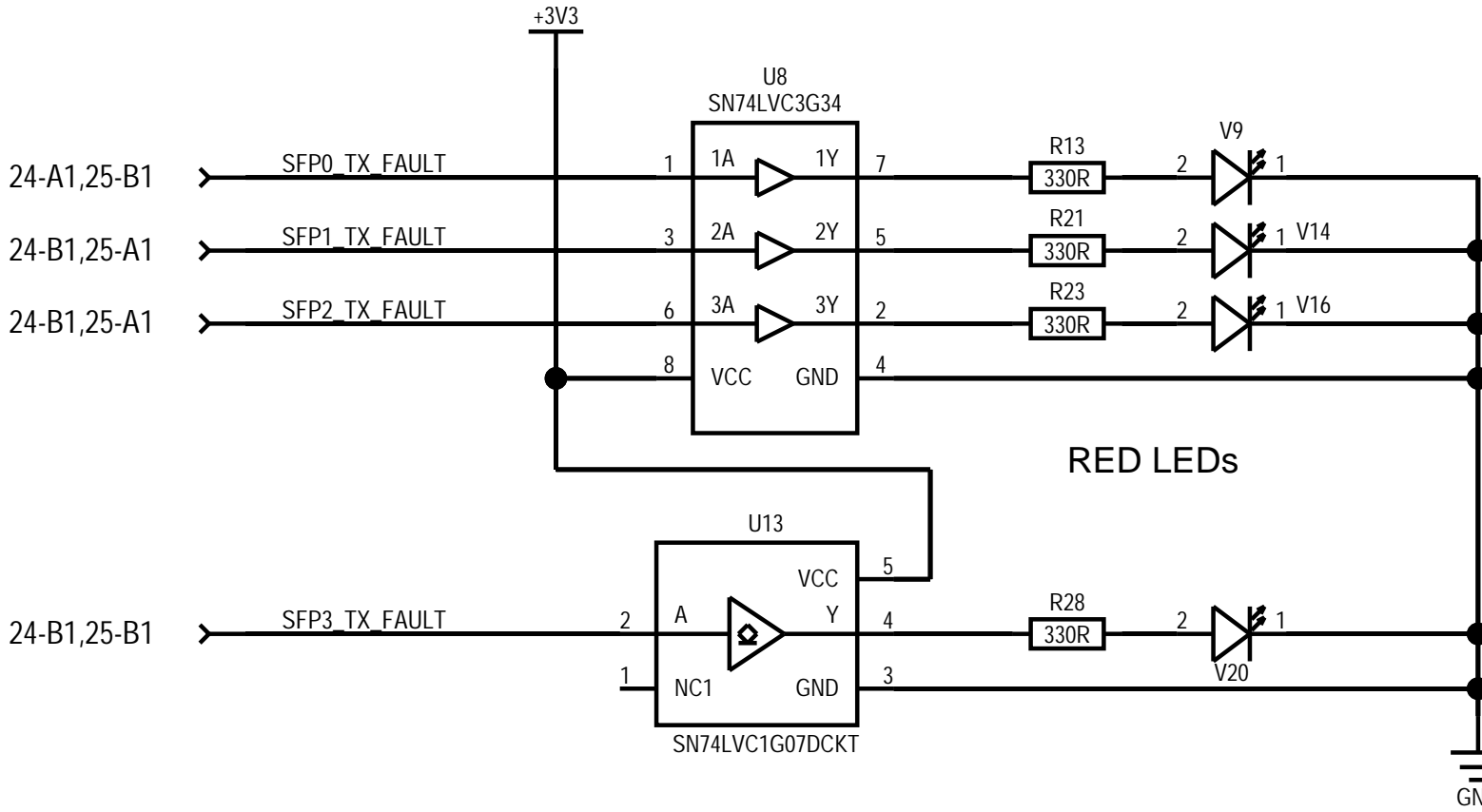
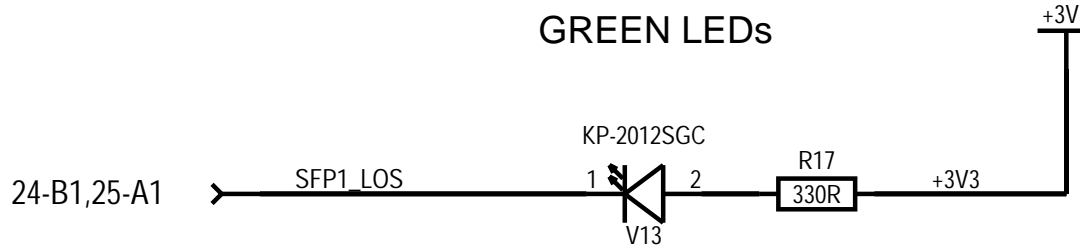
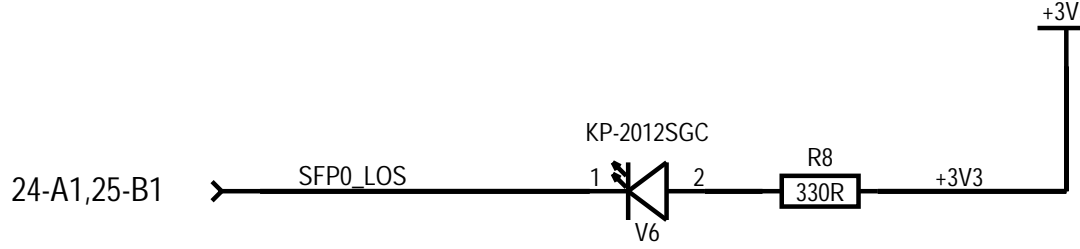


Developer:	Vetrov P.	Project:	FLASH Double DAMC		
		Schematic:	schematic2		
Drawn by:	Vetrov P.	Sheet:			
Layouter:	Vetrov P.	DESIGN- FEA	Notkestrasse 85		
Changed of sch:	Vetrov P.		D-22607 Hamburg		
Date Changed:	07.03.2012	PCB No:	8423	Rev:	02
Date of prod. data:		PCB name:	DAMC2_02	Sheet:	23 of 32

# Four SFP connectors

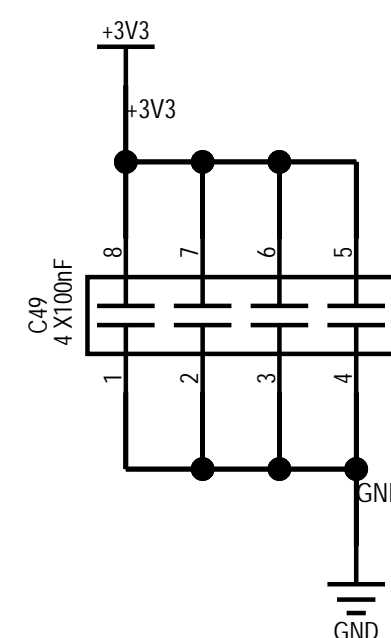


SET 1uH BEAD 1210!!!



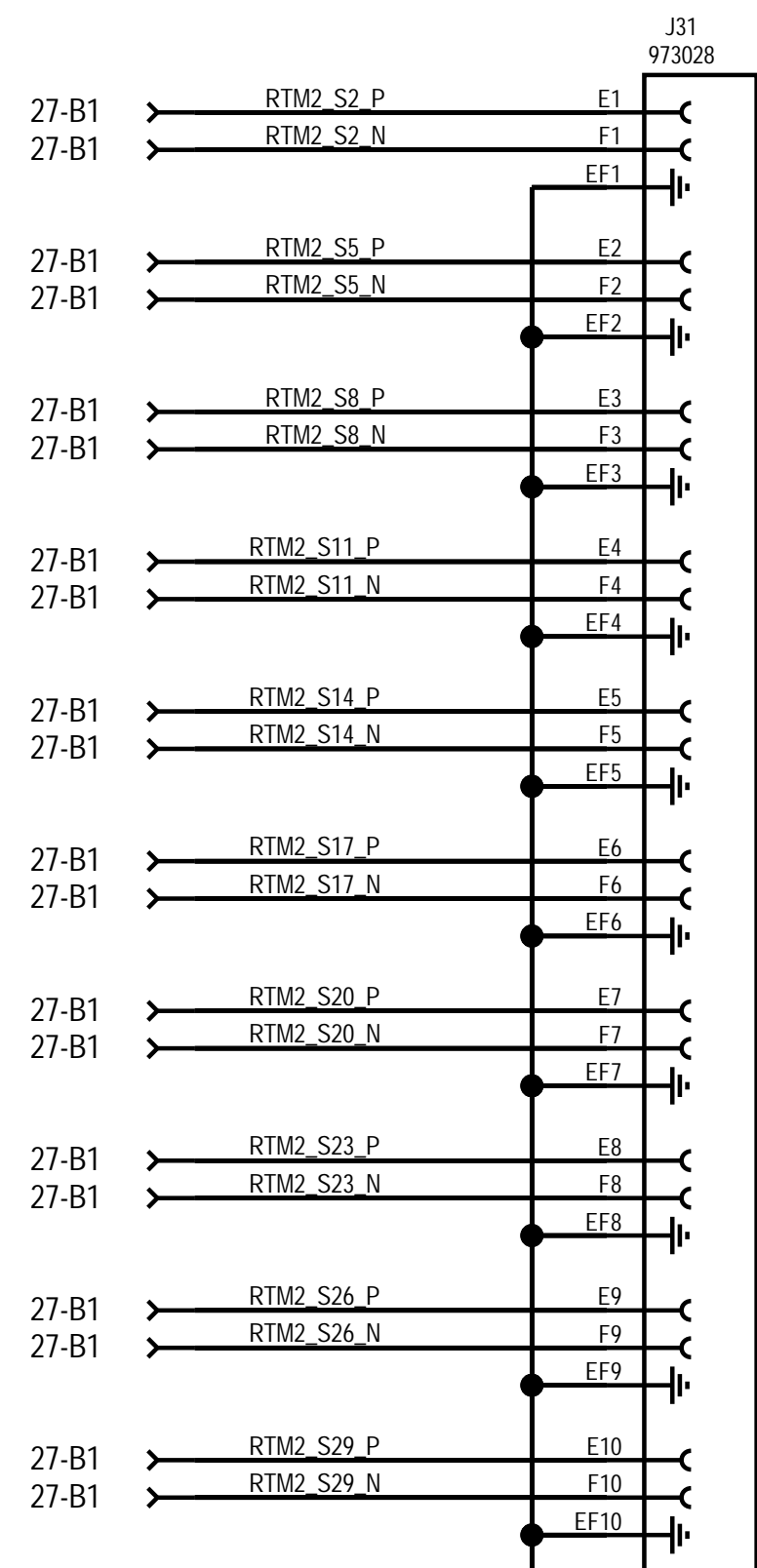
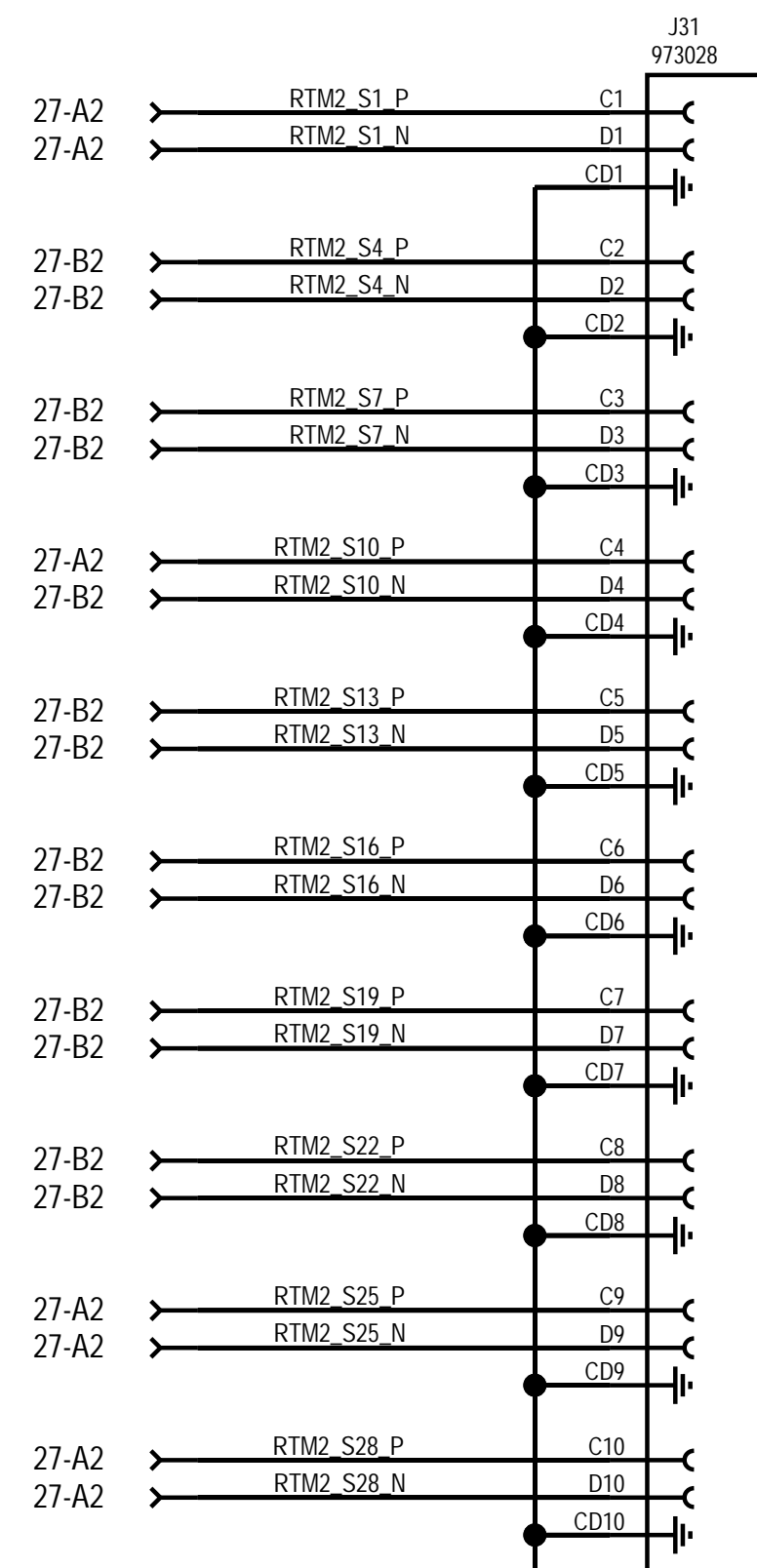
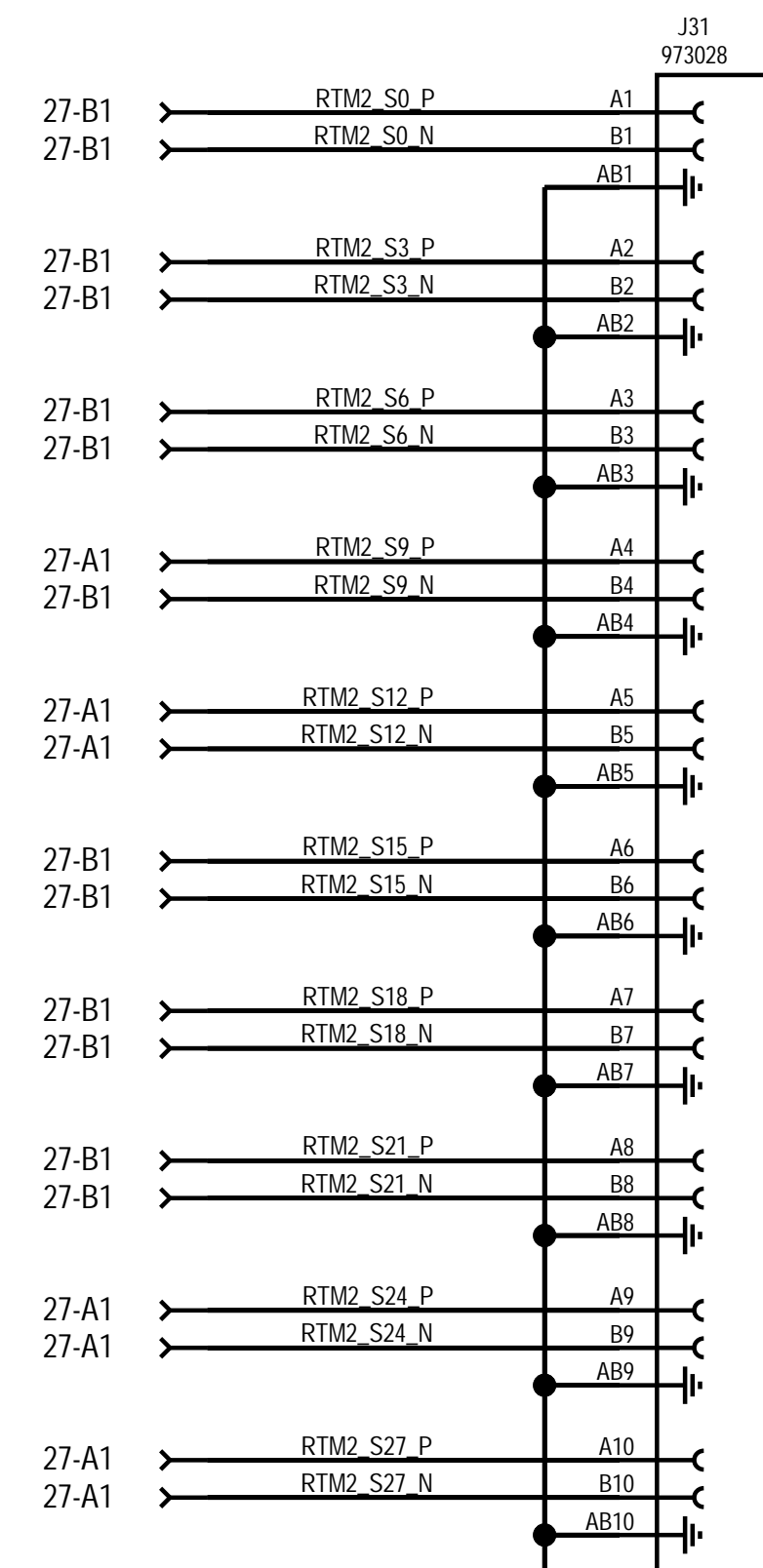
Developer:	Vetrov P.	Project:	FLASH Double DAMC
Drawn by:	Vetrov P.	Schematic:	schematic2
Layouter:	Vetrov P.	Sheet:	
Changed of sch:	Vetrov P.	DESIGNER:	FEA
Date Changed:	07.03.2012	PCB No:	8423
Date of prod. data:		PCB name:	DAMC2_02
		Rev:	02
		Size:	A3
		Sheet:	24 of 32

		XC5VLX50T-1FF1136C		+3V3	
24-B1,24-B2	➤ SFP1 TX_FAULT	E29	IO_L0P_15	VCCO_15	
24-B1	➤ SFP1 TX_DISABLE	F29	IO_L0N_15	VCCO_15	
24-B1	➤ SFP1 MOD2	P31	IO_L10P_CC_15	VCCO_15_2	
24-B1	➤ SFP1 MOD1	P30	IO_L10N_CC_15		
24-B1	➤ SFP1 MOD0	M31	IO_L11P_CC_15		
24-B1	➤ SFP1 RSEL	N30	IO_L11N_CC_15		
24-A2,24-B1	➤ SFP1 LOS	R28	IO_L12P_VRN_15		
24-B1,24-B2	➤ SFP2 TX_FAULT	R29	IO_L12N_VRP_15		
24-B1	➤ SFP2 TX_DISABLE	T31	IO_L13P_15		
24-B1	➤ SFP2 MOD2	R31	IO_L13N_15		
24-B1	➤ SFP2 MOD1	U30	IO_L14P_15		
24-B1	➤ SFP2 MOD0	T30	IO_L14N_VREF_15		
24-B1	➤ SFP2 RSEL	T28	IO_L15P_15		
24-B1,24-B2	➤ SFP2 LOS	T29	IO_L15N_15		
24-A1,24-B2	➤ SFP0 TX_FAULT	U27	IO_L16P_15		
24-A1	➤ SFP0 TX_DISABLE	U28	IO_L16N_15		
24-A1	➤ SFP0 MOD2	R26	IO_L17P_15		
24-A1	➤ SFP0 MOD1	R27	IO_L17N_15		
24-A1	➤ SFP0 MOD0	U26	IO_L18P_15		
24-A1	➤ SFP0 RSEL	T26	IO_L18N_15		
24-A1,24-A2	➤ SFP0 LOS	U25	IO_L19P_15		
24-B1,24-B2	➤ SFP3 TX_FAULT	T25	IO_L19N_15		
24-B1	➤ SFP3 TX_DISABLE	G30	IO_L1P_15		
24-B1	➤ SFP3 MOD2	F30	IO_L1N_15		
24-B1	➤ SFP3 MOD1	H29	IO_L2P_15		
24-B1	➤ SFP3 MOD0	J29	IO_L2N_15		
24-B1	➤ SFP3 RSEL	F31	IO_L3P_15		
24-B1,24-B2	➤ SFP3 LOS	E31	IO_L3N_15		
25-A2	➤ UDL_0	L29	IO_L4P_15		
25-B2	➤ UDL_1	K29	IO_L4N_VREF_15		
9-B2	➤ FPGA_RST	H30	IO_L5P_15		
8-B1	➤ F_SEL1_X	G31	IO_L5N_15		
8-B1	➤ F_SEL2_X	J30	IO_L6P_15		
9-B2	➤ UART_TX_FPGA	J31	IO_L6N_15		
9-B2	➤ UART_RX_FPGA	L30	IO_L7P_15		
14-B1	➤ SLP_S3	M30	IO_L7N_15		
8-B1	➤ OEA	N29	IO_L8P_CC_15		
25-B2	➤ UDL_2	P29	IO_L8N_CC_15		
25-B2	➤ UDL_3	K31	IO_L9P_CC_15		
25-B2	➤ UDL_4	L31	IO_L9N_CC_15		

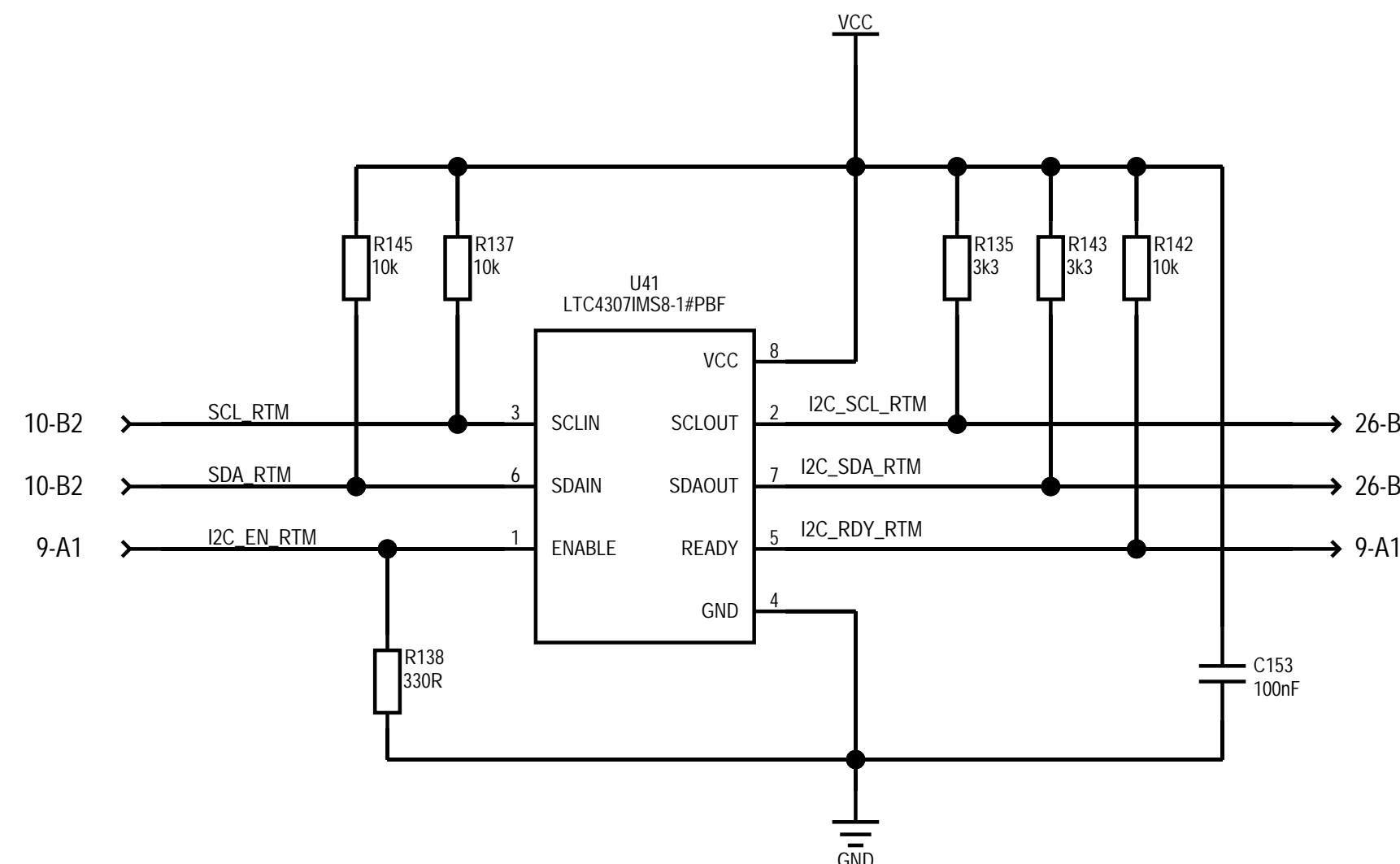
[illegible]

Developer:	Vetrov P.	Project:	FLASH Double DAMC				
		Schematic:	schematic2				
Drawn by:	Vetrov P.	Sheet:					
Layouter:	Vetrov P.	DESY- FEA	Notkestrasse 85				
Changed of sch:	Vetrov P.		D-22607 Hamburg				
Date Changed:	07.03.2012	PCB No:	8423	Rev:	02	Size:	A3
Date of prod. data:		PCB name:	DAMC2_02	Sheet:	25	of	32

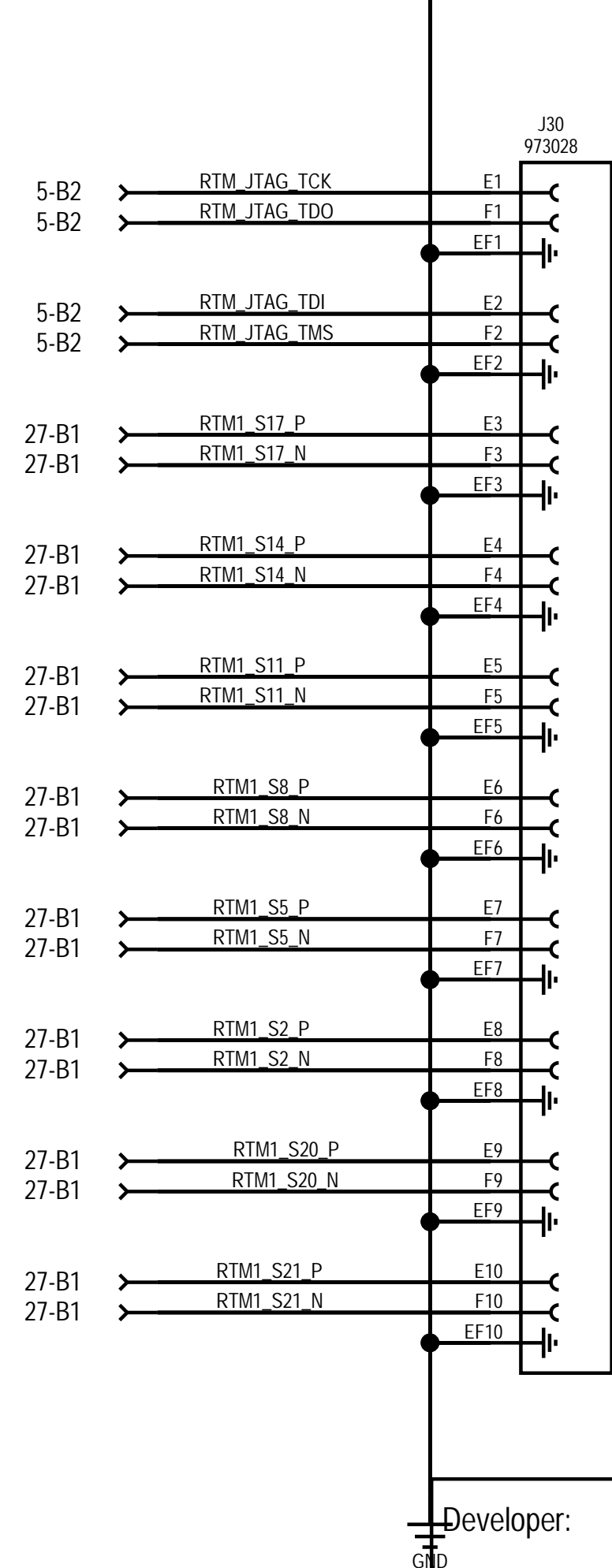
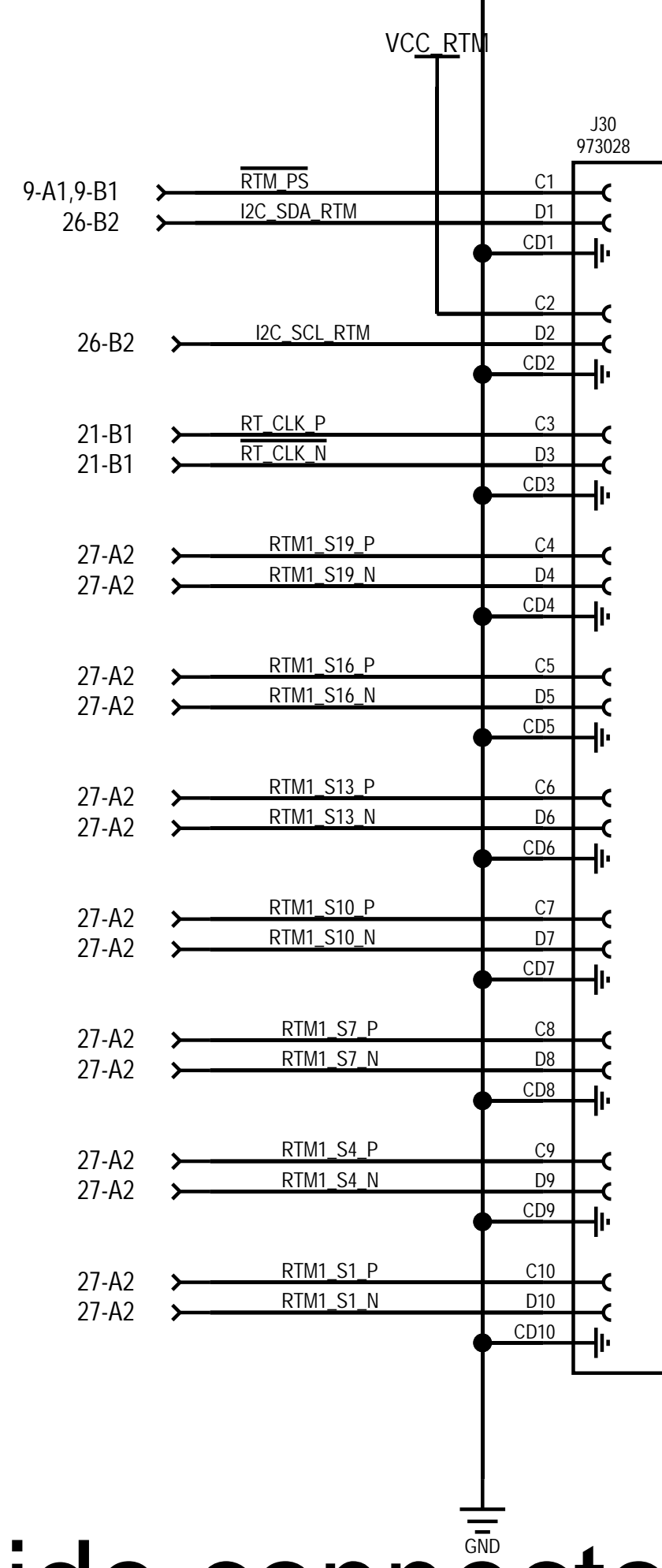
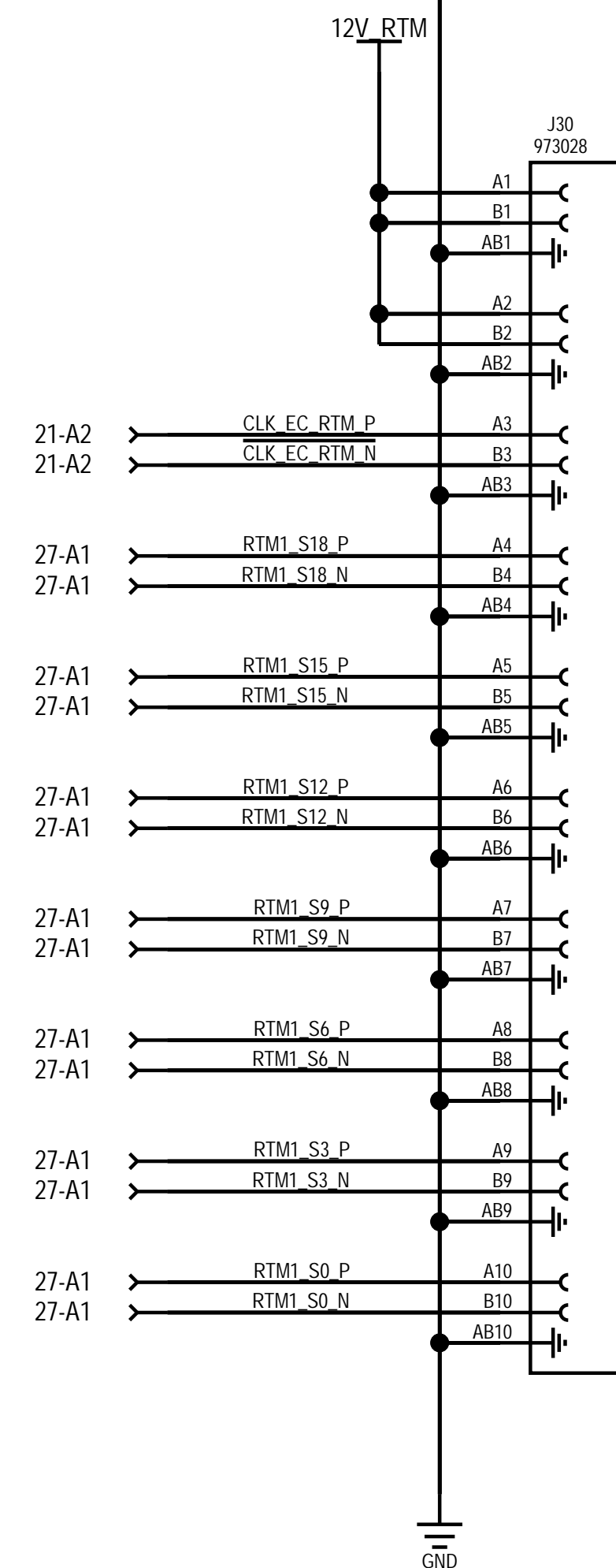
# Two connectors to RTM, 3 Amp/12V



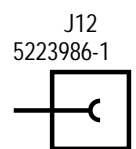
Top connector



Bottom connector

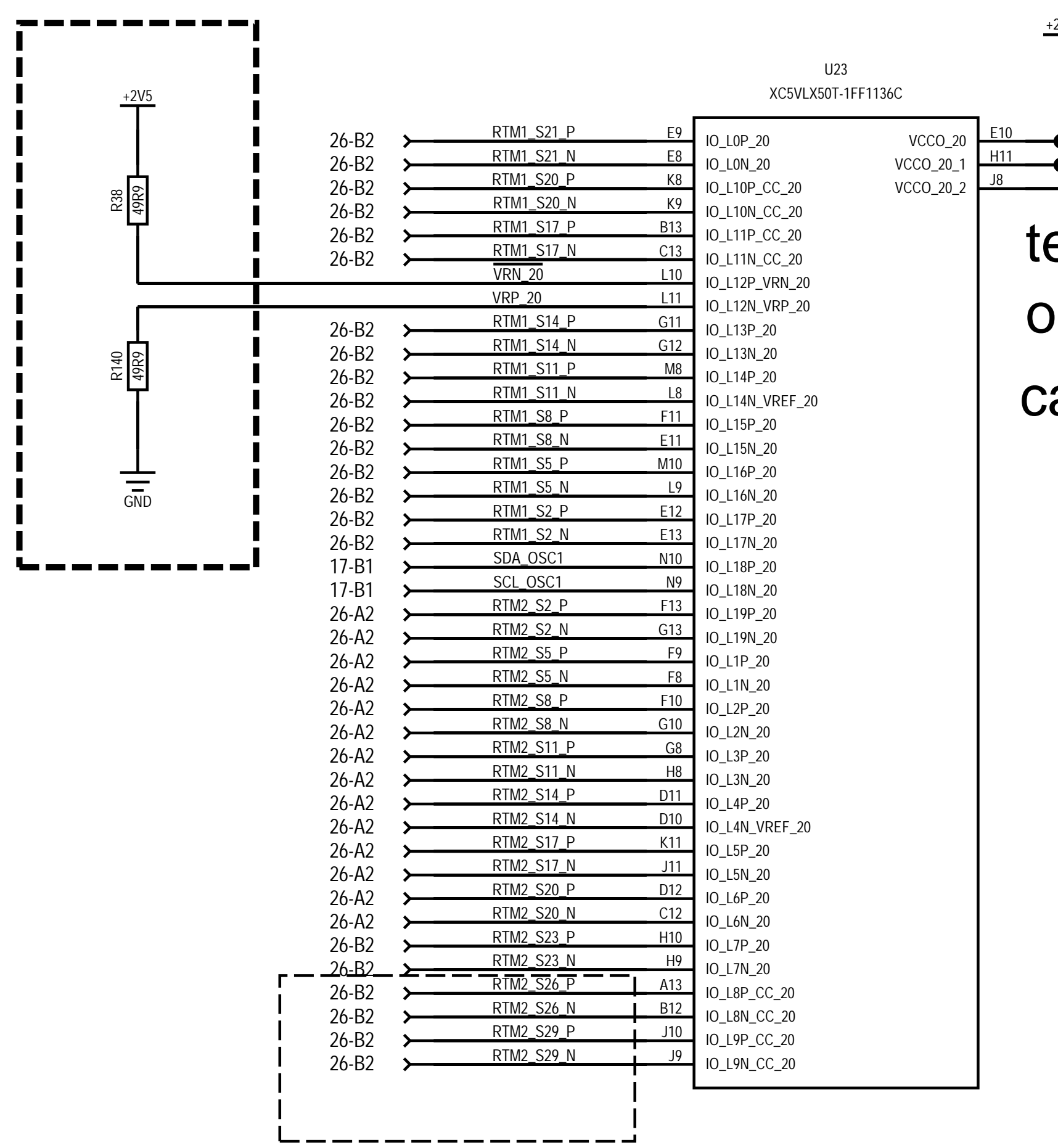
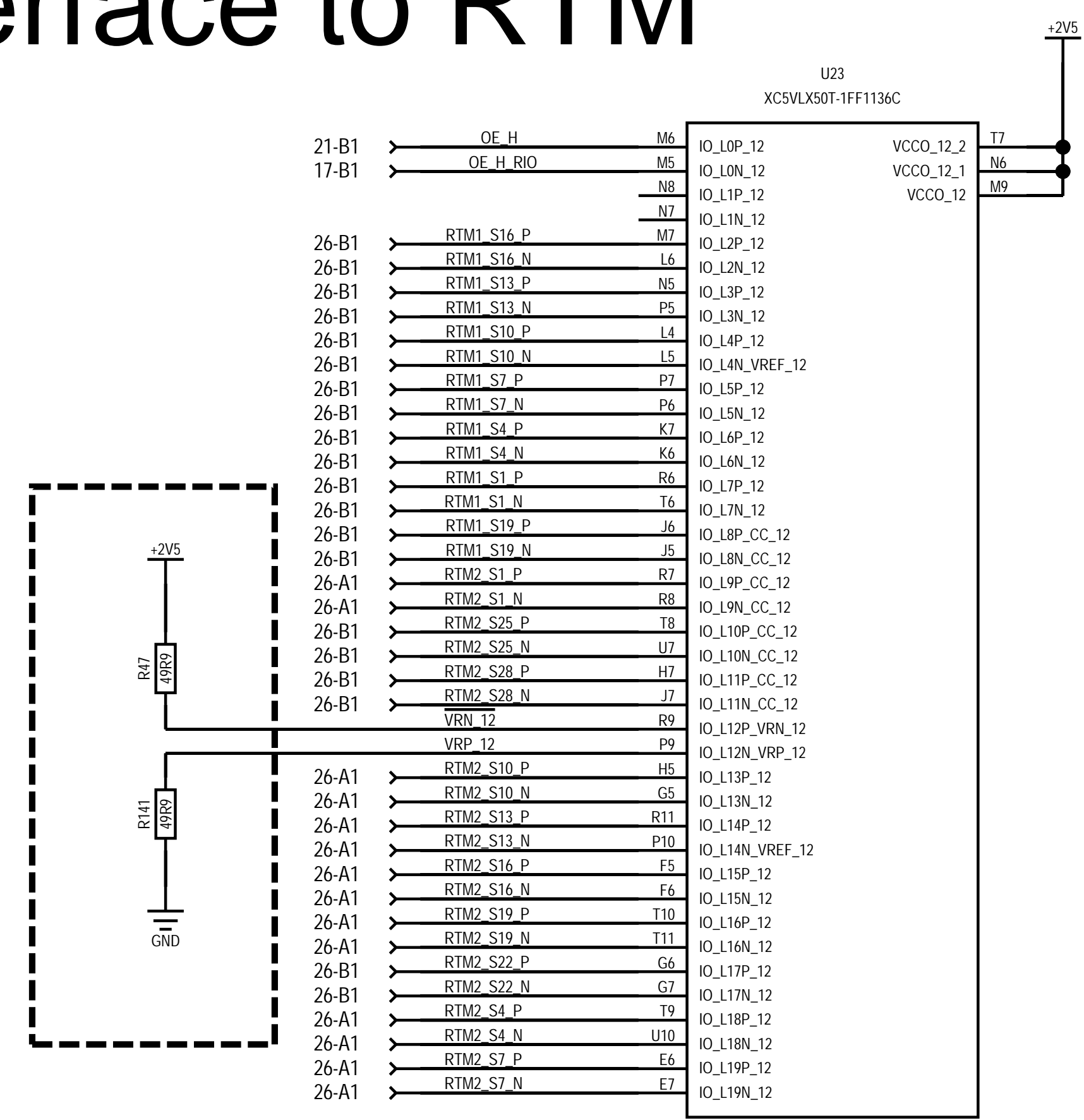
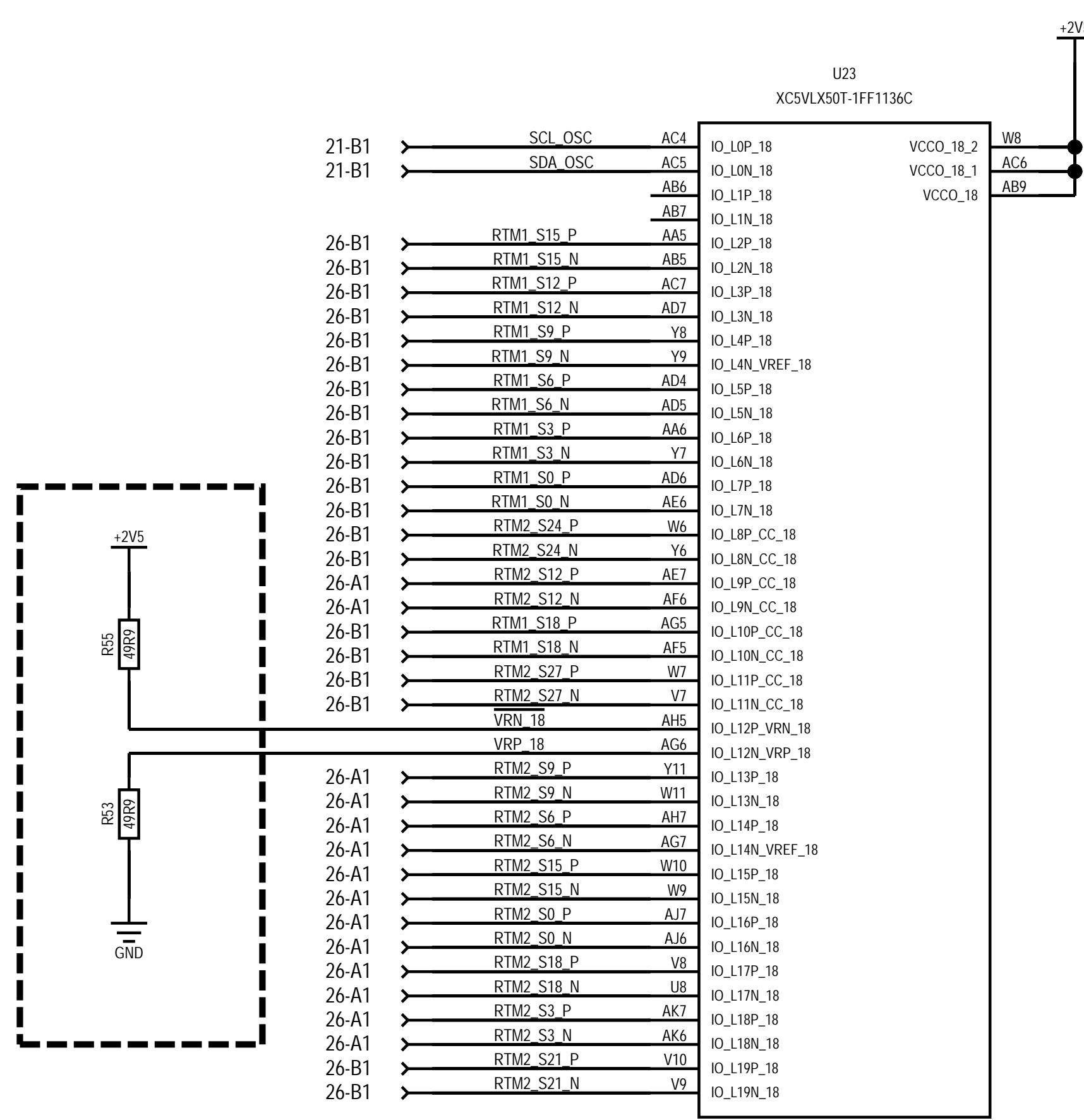


Guide connector

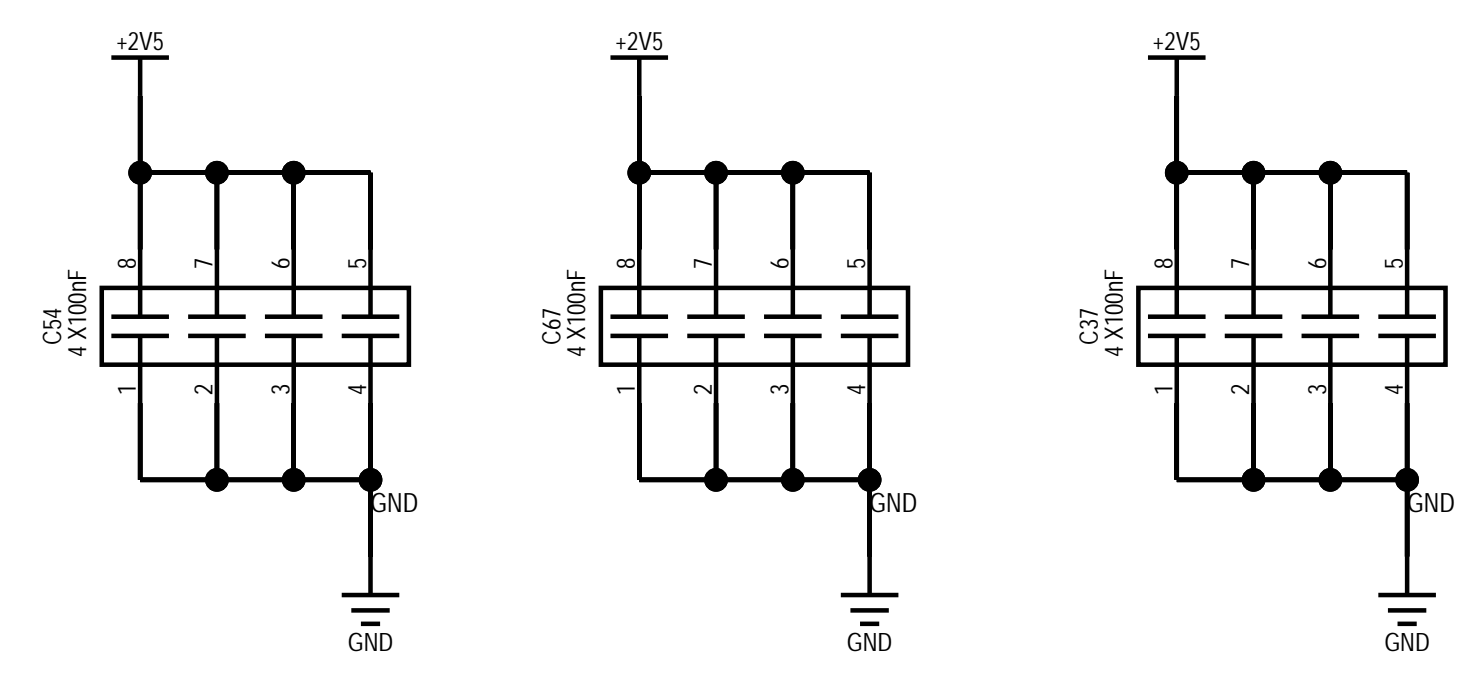


Developer:	Vetrov P.	Project:	FLASH Double DAMC		
Drawn by:	Vetrov P.	Schematic:	schematic2		
Layouter:	Vetrov P.	Sheet:			
Changed of sch:	Vetrov P.	DESIGN- FEA	Notkestrasse 85 D-22607 Hamburg		
Date Changed:	07.03.2012	PCB No:	8423	Rev:	02
Date of prod. data:		PCB name:	DAMC2_02	Size:	A3
				Sheet:	26 of 32

# 2V5 Interface to RTM



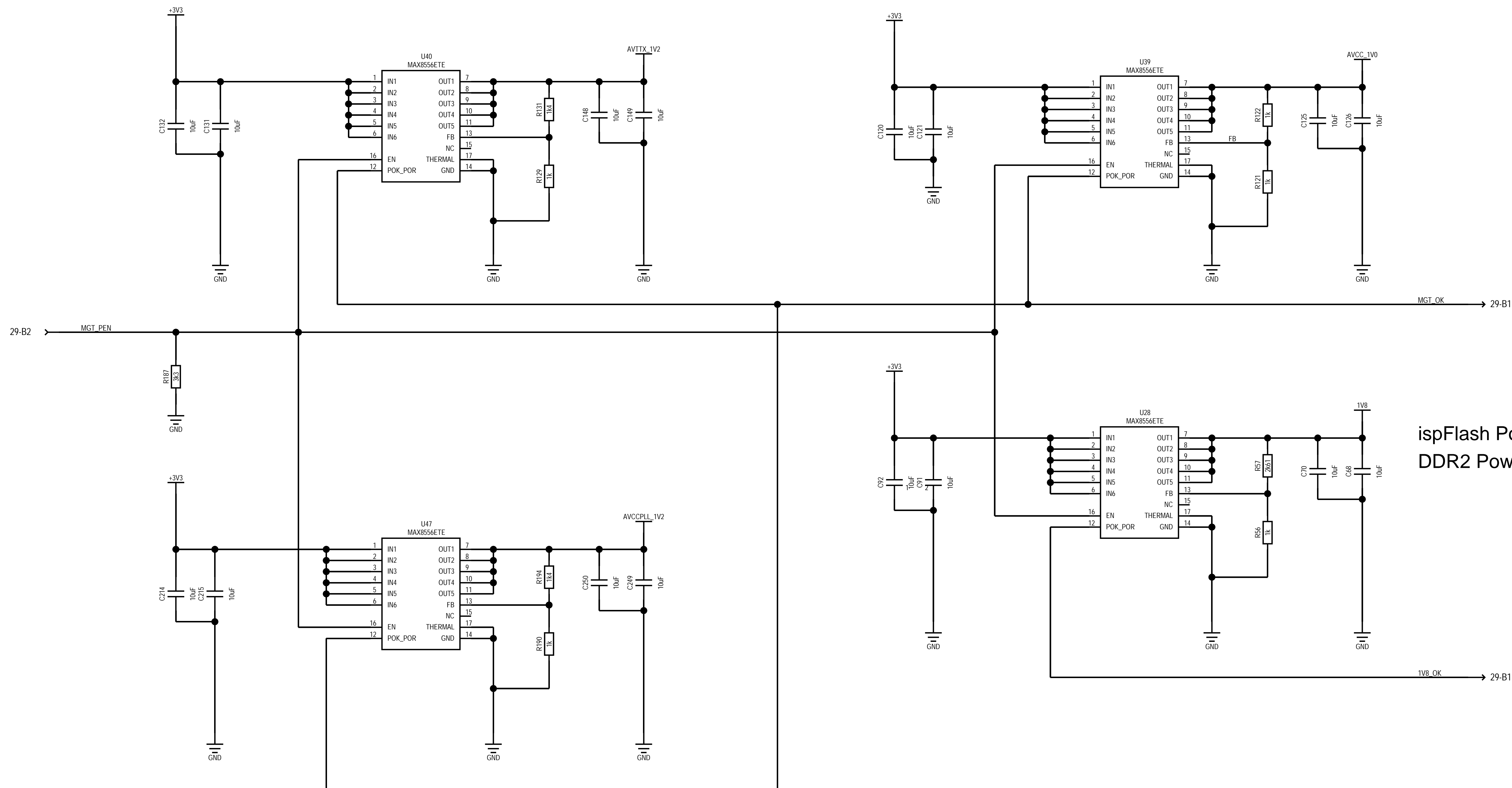
termination banks 12,18, 20!  
only one pair of Ref. Resistors  
can be used for



CLK for BLM\_RTM

Developer:	Vetrov P.	Project:	FLASH Double DAMC
Drawn by:	Vetrov P.	Schematic:	schematic2
Layouter:	Vetrov P.	Sheet:	
Changed of sch:	Vetrov P.	DESIGN- FEA	Notkestrasse 85 D-22607 Hamburg
Date Changed:	07.03.2012	PCB No:	8423
Date of prod. data:		PCB name:	DAMC2_02
Rev:	02	Size:	A3
Sheet:	27	of	32

# Power for GTP, DDR2 and ispFlash

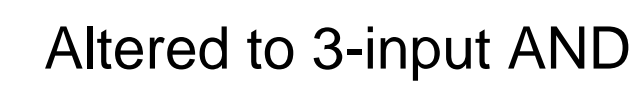


MAXIMUM Dropout Voltage is 0.1V if current is 4Ampers  
Sturt-up voltage rampe to VDD no longer than 500us

Developer:	Vetrov P.	Project:	FLASH Double DAMC		
		Schematic:	schematic2		
Drawn by:	Vetrov P.	Sheet:			
Layouter:	Vetrov P.	DESIGN- FEA	Notkestrasse 85		
Changed of sch:	Vetrov P.		D-22607 Hamburg		
Date Changed:	07.03.2012	PCB No:	8423	Rev:	02
Date of prod. data:		PCB name:	DAMC2_02	Size:	A3
				Sheet:	28 of 32

+3V3\_Payload = +3V3

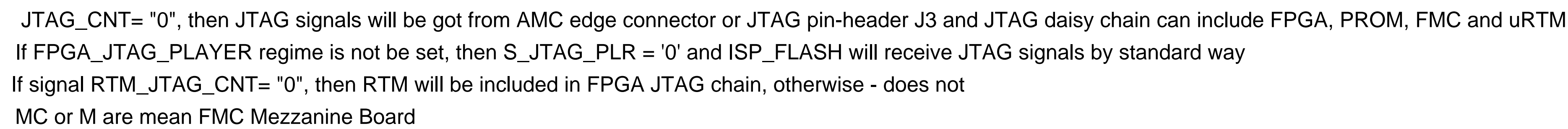
+3V3 MP = VCC



Developer:	Vetrov P.	Project: FLASH Double DAMC					
Drawn by:	Vetrov P.	Schematic: schematic2					
Layouter:	Vetrov P.	DESY- FEA Notkestrasse 85 D-22607 Hamburg					
Changed of sch:	Vetrov P.						
Date Changed:	07.03.2012	PCB No:	8423	Rev:	02	Size:	A3
Date of prod. data:		PCB name:	DAMC2_02	Sheet:	29	of	32



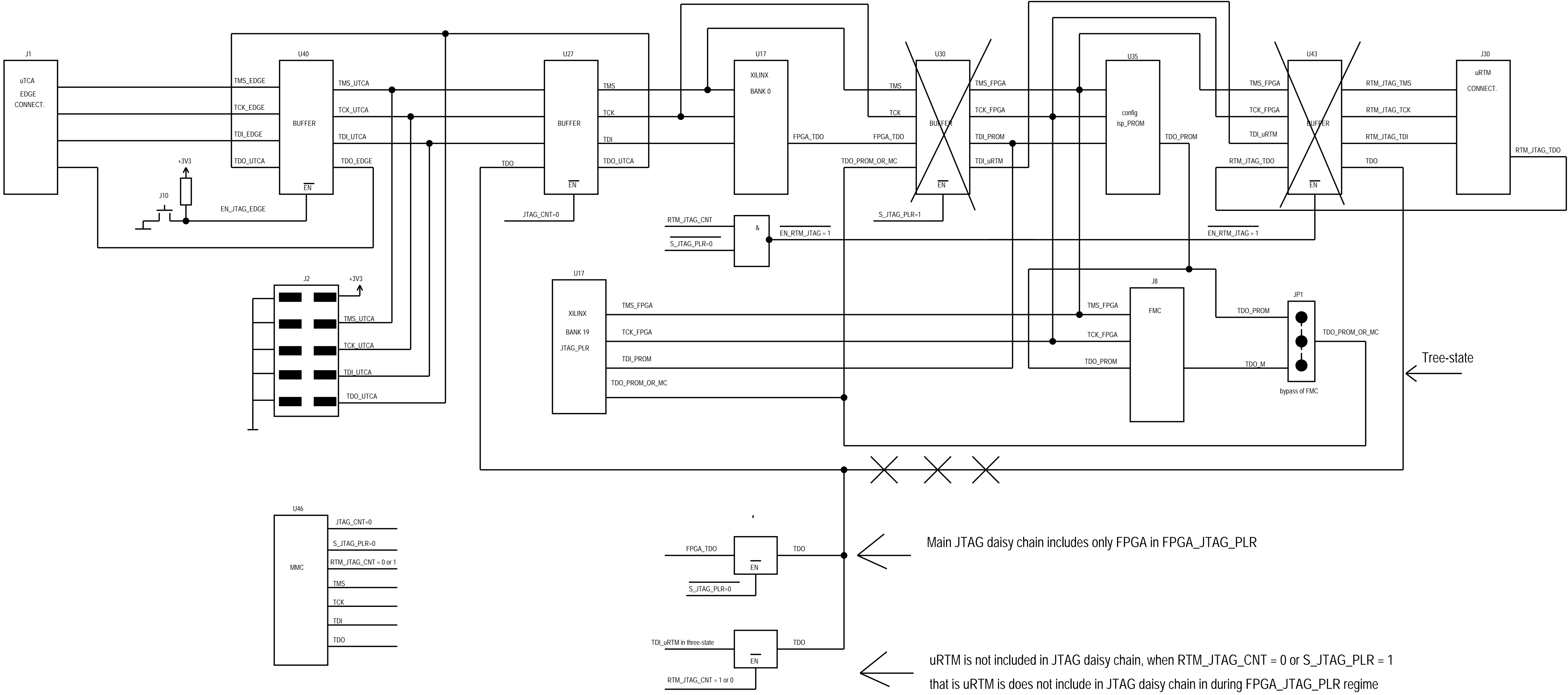
S\_JTAG\_PLR = 0, JTAG\_CNT = 0, RTM\_JTAG\_CNT = 1 or 0



Developer:	Vetrov P.	Project: FLASH Double DAMC					
Drawn by:	Vetrov P.	Schematic: schematic2					
Layouter:	Vetrov P.	DESY- FEA Notkestrasse 85 D-22607 Hamburg					
Changed of sch:	Vetrov P.						
Date Changed:	07.03.2012	PCB No:	8423	Rev:	02	Size:	A3
Date of prod. data:		PCB name:	DAMC2_02	Sheet:	30	of	32

# FPGA JTAG Daisy Chain\_V2 - FPGA\_JTAG\_PLAYER

S\_JTAG\_PLR = 1, JTAG\_CNT = 0, RTM\_JTAG\_CNT = 1 or 0

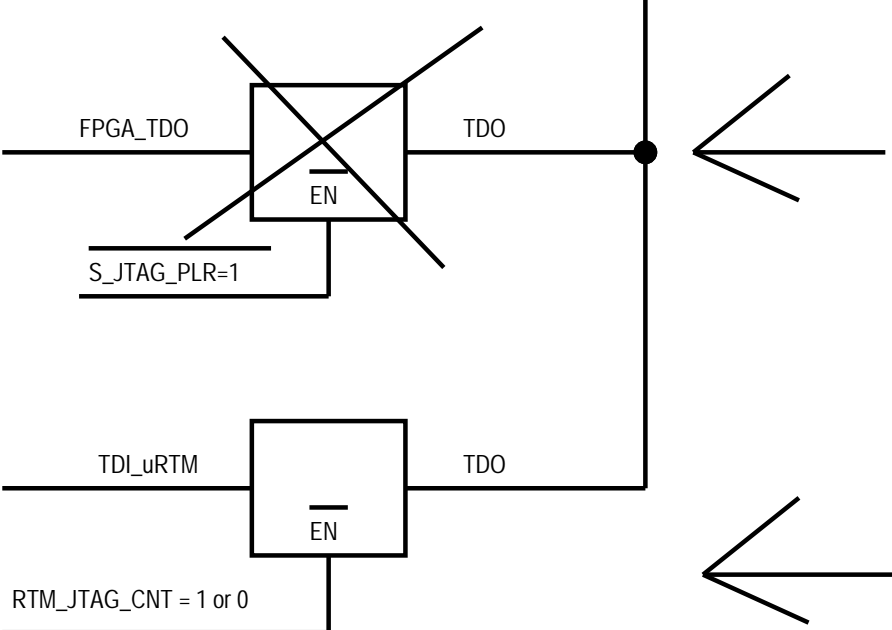
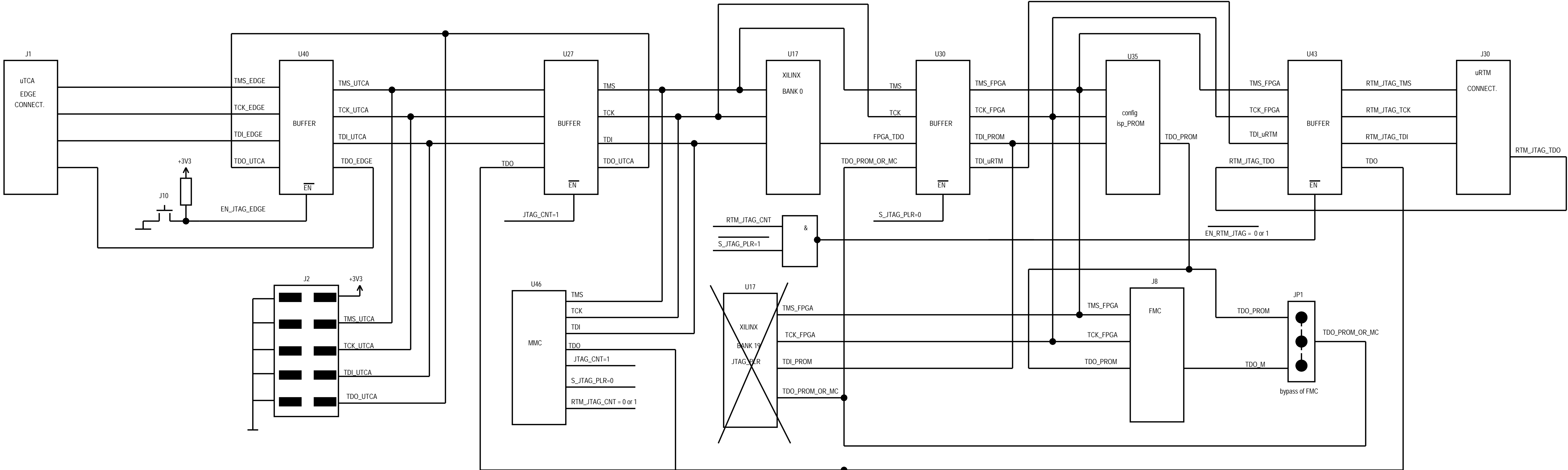


JTAG\_CNT= "0", then JTAG signals will be got from AMC edge connector or JTAG pin-header J3 and JTAG daisy chain can include FPGA, PROM, FMC and uRTM  
If FPGA\_JTAG\_PLAYER regime will be set, then S\_JTAG\_PLR = '1' and ISP\_FLASH and FMC will receive JTAG signals from FPGA  
If signal RTM\_JTAG\_CNT= "0", then RTM will be included in FPGA JTAG chain, otherwise - does not  
MC or M are mean FMC Mezzanine Board

Developer:	Vetrov P.	Project:	FLASH Double DAMC
Drawn by:	Vetrov P.	Schematic:	schematic2
Layer:	Vetrov P.	Sheet:	
Changed of sch:	Vetrov P.	DESIGN- FEA	Notkestrasse 85 D-22607 Hamburg
Date Changed:	07.03.2012	PCB No:	8423
Date of prod. data:		PCB name:	DAMC2_02
Rev:	02	Size:	A3
Sheet:	31	of	32

# FPGA JTAG Daisy Chain\_V3 - MMC JTAG Controller

S\_JTAG\_PLR = 0, JTAG\_CNT = 1, RTM\_JTAG\_CNT = 1 or 0



Main JTAG daisy chain includes only FPGA in FPGA\_JTAG\_PLR

uRTM is not included in JTAG daisy chain, when RTM\_JTAG\_CNT = 0 or S\_JTAG\_PLR = 1  
that is uRTM is does not include in JTAG daisy chain in during FPGA\_JTAG\_PLR regime

JTAG\_CNT= "1", then JTAG signals will be got from MMC and JTAG daisy chain can include FPGA, PROM, FMC and uRTM  
If FPGA\_JTAG\_PLAYER regime will not be set, then S\_JTAG\_PLR = '0'  
If signal RTM\_JTAG\_CNT= "0", then RTM will be included in FPGA JTAG chain, otherwise - does not  
MC or M are mean FMC Mezzanine Board  
JP1 is used for bypassing FMC board

Developer:	Vetrov P.	Project: FLASH Double DAMC				
		Schematic: schematic2				
Drawn by:	Vetrov P.	Sheet:				
Layouter:	Vetrov P.	DESY- FEA		Notkestrasse 85		
Changed of sch:	Vetrov P.	D-22607 Hamburg				
Date Changed:	07.03.2012	PCB No: 8423			Rev: 02	Size: A3
Date of prod. data:		PCB name: DAMC2_02			Sheet: 32 of 32	