Minutes of the TB and CC meeting (8.12.2011)

Location: Rm 5.21, AER 19
(2.1.2012 - CY)

1 Attendance list

WP76: D.Boukhelef, N.Coppola, B.Fernandes, P.Gessler, S.Esenov and C.Youngman.
LPD+TB: J.Coughlan, R.Halsall and T.Nicholl (EVO)
DSSC: T.Gerlach.
UCL: S.Cook, Ashley Joy, M.Postranecky, E.Motuk and M.Wing
FEB: I.Sheviakov and M.Zimmer
WP75: M.Kuster

The minutes, agenda, links to documents referenced and talks are reachable via:
http://www.xfel.eu/project/organization/work_packages/wp_76/daq/2d_pixel_detectors/meetings/ .

Actions are rendered bold. Items of importance are underlined.

If you do not have time or do not want to read the entire document, then skip to the summary and actions.

2 Manpower, actions and purpose of meeting – C.Youngman

Ashley Joy a UCL PhD student was welcomed. He will be working on simulation and CC configuration, etc.

Two WP76 positions have been recently filled: Kerstin Weger working on visualization (GUIs…) and Djelloul Boukhelef working on the PC-Layer (receiving and aggregating data, data and file formats, etc.). A third position was filled after the meeting by Andrea Parenti (device integrator: commercial low rate cameras, webcams…).

Three positions are advertised: an analogue engineer (Patrick's 75/76 team), PLC engineer for experiment and beamline control and a database designer. If you have good candidates please inform us or direct to http://www.xfel.eu/organization/job_offers/ .

Last meeting actions status:

1. *WP75 and 76 milestone reorganization, note defining WP76 interface for pnCCD detector, update of number of detectors foreseen and their sizes.*
   Milestones reorganized, **note in preparation**.
2. *Patrick should update us regularly on timing system CDR status to allow feedback.*
   The pre-CDR document was distributed just before the meeting. It should read and comments and queries sent to Patrick who will moderate and funnel the result to Kay Rehlich. **The final CDR document needs vetting by us, and other parties, before approval.**
3. *There is a bi-weekly FPGA expert group meeting, all people interested should be on the email list, if you should be then send email to Patrick.*
   Done.
4. *Patrick will organize an additional bi-weekly EVO meeting to coordinate and track development discussions (interface definition, use of same modules, etc.) concerning CC, FEE and TB. The suggestion is Wed 11:00 CET.*
   Done.
5. *Need to check the LPD test module requirements for the prototype CC board.*
   Done, LPD are currently using the PC3461M test board for FEM testing.
6. *When and what is needed for CC-FEE tests needs coordinating – at Patrick's bi-weekly meeting?*
   Immediate usage requirements done: LPD are happy with the PC3461M, DSSC received a MTCA4+TR-X1+CC for tests (APD crate system taken to Mannheim and setup by Patrick and Thomas ~ 20.12.2011), and AGIPD have no requirement. **Longer term plan for CC test systems needed.**
7. *M.Kuster should specify when CC systems will be needed at external light sources.*
   Discussed – no time schedule derived.
8. *Manfred should work out details of supplying 6 additional DAMC2s and give us the suggestion a.s.a.p.*
   Done, see Patrick's talk.
9. *Final CC RTM hardware design is scheduled for Q2/3, how does this fit with the DAMC2 functionality update list? The CC side functionality DAMC2 update list has been given to the FEA, but no other group has submitted their requirements, we should review our list and submit again, expecting to receive the updated DAMC2 for the final RTM hardware stage. Manfred should outline the when/how solution.*
   Done, see Manfred's talk.
10. *LPD and DSSC do not need the 1 bit 4.5MHz VETO decision notification message, they need the 99.31MHz encoded version only. AGIPD should confirm whether they need it or not.*
    See next action – the 4.5MHz yes/no notification has been removed from the VETO spec.

11. *After feedback, from FEE developers, generate an updated VETO specification and work plan.*
    The VETO specification was distributed by Patrick on 21.12.2011. It should be read, commented on and confirmed.
12. *WP76 need 2 demonstrator boards for slice test, i.e. one more!*
    Two boards will be manufactured for use in the slice test.
13. *The demonstrator firmware requirements needed for the slice test must be specified.*
    Initial requirements we specified after the meeting.
14. *The requirement of specifying data formats and configuration requirements was detailed. This applies to all sub-systems: FEEs, TB and CC and will be coordinated by WP76.*
    The data formats and there configuration still need to be worked on. Djelloul, as PCL responsible s/w person, will be bound into the process.
15. *The measured storage cell loss at AGIPD is sufficiently large to require correction, which means that the storage time of data per cell will have to be sent with the data. The best way to do accomplish this has to be defined in discussion on Peter's return.*
    See Peter Goettlicher's talk.

The aims of this meeting are listed below, see summary of meeting for results and other points arising:

- Check component status and delivery schedules
- Check work plan

3 Summary of TB, CC and FEE FPGA meetings – P.Gessler

Bi-weekly FPGA meeting for CC, TB and FEE participants organized and now going well. Minutes and slides from meeting can be found at the following URL:

The clock jitter for DSSC seems to be less critical than thought, but the CC jitter should be kept as low as possible. A CC test setup will sent to Mannheim immediately after the meeting for FEE tests.

Preparations of CC tests with FEEs: LPD are happy with the CC prototype, AGIPD do not need a board yet, and DSSC will get the test system (CC and DAMC2) including crate for test purposes.

WP76 is participating in the EU CRISP project with ESRF, DESY and other institutes on DAQ and data management issues. The idea is to organize a workshop and FPGA UDP stack implementers (Igor, Rob and Thomas) should participate. There are a number of open issues like 10 to 40GE migration, TCP modules, iWARP, etc., which are on the road map for future developments.

The VETO specification was not ready for the meeting, but will be distributed shortly.

Erdem, Patrick and Thomas performed tests on the CC and X1 timing board signal distribution quality in the MTCA4 crate yesterday. Preliminary results: at >100MHz ~20ps

jitter; at 10MHz ~300ps. But the measurement setup and the 1.3GHz generation are not optimal. The large jitter seems to be driven by a 345kHz contribution. The setup has to be improved and more measurements made. More final reports will be distribute through the FPGA wiki later.

The 2U MTCA4 crate development. **Front air intake and output on the slide. Important point to discuss the rack design with Kay Rehlich - thought not to be a problem, but needs checking.**

The DESY-FEA RTM exerciser board was described. Provide for RTM testing of the board without crate and associated I2C bus connect from DAMC2 type modeul. The board would allow USB bus to drive the I2C bus. The PCB cost is however prohibitive and it was decided to move to an intermediate solution using the commercial RTM extender board for the time being – suggestions for cheaper solutions are welcome!

The XFEL timing system CDR (Conceptual Design Report) appeared just before the meeting. Sam asked about the bunch pattern - worry is that the bunch pattern index has been forgotten about. **It is clear that we all have to read the timing CDR and get changes or improvements made where necessary - all our requests should be funnelled through Patrick who is one of the authors**. According to XFEL work practise a CDR is followed by a Technical Design Report (TDR) after ~6 months.

4 C&C status – E.Motuk

The CC status was reviewed. The number and functionality of firmware modules has not changed. Note that the 4.5 MHz level distribution of the VETO is no longer supported. The smoke test problems reported at the last meeting were due to soldering problems with the DC/DC converter on the first board. The second board had a soldering problem with the I2C address resistor. The remaining two PCBs are now being prepared for use.

The clock distribution functionality of the RTM has been tested using the on board oscillator and the MCH PLL as source. Connectivity with the DAMC2 has been verified, the FPGA sees clocks and test signals generated by the RTM. Fast clock (~100MHz) and data signal generation and transfer have been tested on all output channels using evaluation boards. Long term tests using two evaluation board sinks show no errors.

Further RTM tests were made yesterday in AER19. The 375kHz peak seen on the frequency analyser when looking at the clock signal is the switching frequency of the DC/DC converted. On the other CC RTM with a different DC/DC convert a different switching frequency is seen. P.Goettlicher will suggest suppression of noise methods in his talk. The 67kHz periodic noise seen on clocks at UCL seems to be coming from field pickup on the scope probes - it was not seen by using BNC probes. More tests are needed.

Wiki pages written:

- how to use the CC RTM
- changes and revisions
- requirements for the next DAMC2 upgrade

The requirement update for DAMC2 have been sent to Manfred.

Schedule:

- test and clock quality measurements: Now-End of year.
- tests against new timing CDR - Jan 2012
- testing with FEEs – from now
- development of next revision - Q2/2012

The LPD does not need a real RTM board yet, but want to test with the modules. Sam and Erdem should discuss and decide. Aim is to test protocols and signals sent by CC, ideally on the bench.

Planning of the experiment hutches has started and the length of the FEE-CC connection cable needs re-measuring. The current tested length of 5m using coiled Cat5 cable is too short. **FEE-CC cable length test using a prototype board in a realistic environment (PETRA3 instrument to control room hutch) needs to be organized.** As always the longest length possible should be aimed for – use Cat6 or higher cable.

5 FEA status – M.Zimmer

Twenty DAMC2 boards are with their owners and another ten, identical, boards are being produced – partially at the request of the TB+CC+FEE community. Unfortunately the price estimate made by the producers was a factor of two under the final price!

The 14.12.2011 meeting at DESY to, hopefully, discuss final version will be held at DESY. Expect a new version by the summer of 2012. The TB+CC+FEE community have submitted their updates, but many groups have not so far done so. See slides 3+4 for some information about upgrades requested.

External users: CERN (CMS and ATCA) will not follow the MTCA4 standard. SLAC will use the DAMC2 and possibly Cornell. Commercial DAMC2 like boards will be offered by TEWS. A TEWS Spartan6 FPGA version is being pushed by SLAC who require less powerful boards well suited to the Spartan6 FPGA series. There are probably many users at XFEL that could exist with a lower performance board. A longish discussion of Spartan LVDS problems ensued.

The status of the additional order of (original) DAMC2 boards and an update of the modifications agreed to at the 14.12.2011 meeting should be distributed a.s.a.p.

6 AGIPD FEE status (and powering, etc.) – P.Goettlicher

LV and HV supply requirements were reviewed. AGIPD is still aiming for external power supplies with voltage stabilization/regulation in the FEE modules, which avoids DC/DC at the FEE with its associated converter noise. External supplies with ~10m cables should be feasible regarding voltage drop – source voltage remote sensing is preferred. Slide 3 showed the voltage and power requirements for 1/16 (a module) of the 1Mpxl – note that each module needs an isolated ground. LV current modulation due to ON/OFF powering of the electronics with the train delivery cycle produces voltage and current fluctuations as a function of time and the power supply has to handle this (~1%) current change gracefully. **An initial set of requirements for LV and HV individually and generally (control bus, 19”…) were given – finalized sets will be provided by Peter by the 17.2.2011 milestone and WP76 will make a recommendation for AGIPD.** Iseg/Wiener and Caen are two producers with a known light-source and HEP track record who offer supplies in

the ballpark of the requirements. The LV and HV discussion only applies to AGIPD; LPD and DSSC are working on their own h/w solutions (LPD: Steve Burge. DSSC: Carsten Hansen) – the control issues should be addressed by the control interface software.
A ferrite bead for removing switching frequency peaks was suggested as a (bulky) solution to the DC/DC converter noise problem described in Erdem's talk.

AGIPD ideas on the interlock were defined, these are in line with practise at the ZEUS experiments MVD silicon detector and similar detectors at LHC – all power injection into sensitive areas, here the FEE, is removed after a timeout. The timeout allows smooth ramp down, if possible. **WP76 is expected to provide an interlock solution/concept and AGIPD the requirements. Again LPD and DSSC must be compliant with this solution – or suggest a better one!**

Peter reviewed the storage cell leakage (repeated the last meetings information.) **The conclusion was that the correction (calibration, cell leakage correction…) will be done initially in the PCL: WP76 provide the calibration framework and WP75 will organize the algorithm for the detector.** Similar schemes can be in place for LPD and DSSC.

7 LPD FEE status – J.Coughlan

Five FEMs already in use and 20 in manufacture expect in Jan/Feb.

Collaboration has been informally asked to take LPD super module or a quadrant to LCLS by March/April 2012.

- want to test ASICs with XFEL energies
- some interest to do some science with it
- will use a Diamond development of the control software
- Tim is working on firmware control to get LPD ready for SLAC?

Weekly meetings of LPD with WP75 - this is the place where interlocks are probably discussed.

Plan and schedule:

- test FEM
- LCLS preparation
- migrating to Ethernet control system
- work on firmware including dynamic VETO
- plan on getting the liblpd.so from Tim at the beginning of February for integration with exfelSuite, see Sergey's talk.

The TWELL-2011 Valencia conference paper has been accepted for publication.

8 DSSC FEE status – T.Gerlach

The test system used to measure the following signal quality parameters was shown:

- ADC clock is OK
- control (STart...) now runnig at 99MHz should be OK needs measuring
- PLL jitter - what was the statement about different production batches?
- TX lanes on 10GE system - see clean eyes after changing some MTA parameters

- ADC data capturing clock. (1/2 of 800MHz) looks poor, not understood - termination?

The FPGA modules are being worked on: CC emulation etc., but most problems are IO board issues and these have priority.

Next steps:
- DSSC power regulator tests with DESY people.
- solve ADC capture clock
- ASIC data capture tests
- general firmware
- test with CC and DAMC2 board as soon as test crate in Mannheim

9 VETO specification and discussion – P.Gessler

The updated VETO specification was distributed after the meeting on the 21.12.2011 all FEE experts (and others) are requested to read it and provide feedback at the next FPGA meeting(?).

10 TB status – J.Coughlan

The TB demonstrator will not be available at XFEL until end June 2012. The design engineer, Senerath, is retiring end of March, by which time as much as possible of the ATCA circuit design, docs and tests will be ready. Ed Freeman has gradually been taking over the work since November. The drawing office engineer doing the PCB routing remains the same and an additional firmware developer has been allocated to the project since November.

The principle delay results from the PCB routing which is demanding, but is converging (slide 3) as can been seen by the comparison of the original rats nest (slide 14) from the last meeting and now (slides 5 thru 11). The aim is to have the PCB in manufacture in Feb, 6 boards will be made.

The additional 3 months delay will cause a slight hick-up regarding the slice test. The delivery schedule was summarized as:
- PCB out to manufacture Feb. (was end Nov)
- Purchase components for 6 boards. Last parts in Feb.
- Assembly of 2 boards with delivery in March.
- Tests at RAL (min ~2 months)
- Aim for 1 board to XFEL May/June (was April)
- Manufacture 2 + 2 more
- Preparing FPGA Firmware in parallel (see Rob's talk)

What are WP76 Firmware Requirements for Initial Slice Tests? This was the case of the missing email – a more substantial description was produced after the meeting by Chris and Rob and can be found on the website. The basic requirement is to use the TB demonstrator to inject video pattern and/or downloaded images into the slice test with single or multiple links which requires time synchronization and the ability to configure IP and MAC address lists, etc.

Train Builder paper is published (TWEPP-11 conference) JINST 2011_JINST_6_C11029

http://dx.doi.org/10.1088/1748-0221/6/11/C11029

11 TB and FEE firmware status – R.Halsall

Rob reviewed who was working on the various project TB and FEM projects. The on-the-fly video pattern generation module developed for testing was described.

Rob is enjoying himself with the UDP firmware development; using wire direct UDP which allows senders to write directly into the user space of application programs saving copy operations. This and data formatting using trailer format overwrite may be useful. **We need some coordination to ensure that data transfer and formats converge for the slice tests, issues: with and without vendor specific features, train specific metadata added to the image data, etc.**

12 Software status – S.Esenov

Sergey described the responsibility split between WP76 (Sergey) and STFC (Tim) concerning the s/w interface to FEM and TB f/w. The baseline is that Tim will provide a libFEM.so allowing Sergey's device to drive configuration and data taking of single FEMs. Multiple FEMs, i.e. Mpxl LPDs, will be handled by a composite device. The TB interface will be based on the FEM interface. In an email exchange after the meeting the functionality of libFEM was described, it is based on commercial (Basler, Andor…) camera interface APIs.

The time scale for libFEM.so device integration is constrained by vacations to start in February.

13 Summary of meeting

The immediate time schedule looks like:

- FEE expert feedback concerning VETO specification upgrade Jan 2012
- Submit TB demonstration PCB for manufacture Feb. 2012
- Integration of FEM software interface starts Feb 2012
- Continued CC RTM prototype testing against FEEs, Q1-Q2 2012
- Integrate TB demonstration prototype boards into slice test end June 2012
- Finalize CC RTM hardware design Q2-Q3/2012

14 The Actions

The list of actions:

1. **The final CDR document needs vetting by us, and other parties, before approval.**
2. **Longer term plan for CC test system needed.**
3. **Front air intake and output on the slide. Important point to discuss the rack design with Kay Rehlich - thought not to be a problem, but needs checking.**
4. **FEE-CC cable length test using a prototype board in a realistic environment (PETRA3 instrument to control room hutch) needs to be organized**

5. **The status of the additional order of (original) DAMC2 boards and an update of the modifications agreed to at the 14.12.2011 meeting should be distributed a.s.a.p.**

6. **An initial set of requirements for LV and HV individually and generally (control bus, 19"…) were given – finalized sets will be provided by Peter by the 17.2.2011 milestone and WP76 will make a recommendation for AGIPD and WP76 will pay for 1 x 1Mpxl.**

7. **WP76 is expected to provide an interlock solution/concept and AGIPD the requirements. Again LPD and DSSC must be compliant with this solution – or suggest a better one!**

8. **The conclusion was that the correction (calibration, cell leakage correction…) will be done initially in the PCL: WP76 provide the calibration framework and WP75 will organize the algorithm for the detector.**

9. **The updated VETO specification was distributed after the meeting on the 21.12.2011 all FEE experts (and others) are requested to read it and provide feedback at the next FPGA meeting(?).**

10. **We need some coordination to ensure that data transfer and formats converge for the slice tests, issues: with and without vendor specific features, train specific metadata added to the image data, etc.**

15 AoB

The next meeting will be held in Hamburg on 19th April 2012. If you have problems with this date please notify CY by mid-January.