Minutes of the Train Builder meeting (2.7.2009)

C.Youngman 2.7.2009 (last revised 4.7.2009)

1 Attendance list

UCL: M.Postranecky and M. Wing.
DESY-FEA: I.Sheviakov.
LPD detector and TB: J.Coughlan.
AGIPD detector and DESY-FEB: P.Goettlicher.
DSSC detector: A.Kugel. and T.Gerlach
WP76: S.Esenov and C.Youngman.

The minutes (actions in bold), agenda and talks are reachable via:
http://xfel.desy.de/project_group/work_packages/photon_beam_systems/wp_76_daq__control/train_builder/ .

2 Introduction

M.Wing reported that a post-doc student had been acquired. He will work ~50%(?) of hist time on C&C and TB hardware related issues (with STFC) support.

Follow up points from last meeting:

- The 11th May IKRC (In-Kind Review Committee) recommended both TB and C&C projects.
- In-kind funding has not worked for both projects. The priority is now to get both moved to direct contracts. The quicker the better! **C.Youngman will push this next week and keep people informed.**
- M.Zimmer wanted to know how many PHY chips would be needed. The following requirements exist: 16 (TB+LPD Q1/2010), 40 (LPD Q1/2011), and 10 (DSSC). **P.Goettlicher will provide the numbers for AGIPD.**
- The cleanness of the XFEL timing clock distributed to instruments has been resolved, see talk below.

3 100MHz clock cleanness – P.Goettlicher

The XFEL timing group have finally agreed to provide a glitch free continuous clock from the Timing Receiver board (i.e. input to the C&C). The frequency will be in the range 100kHz – few MHz. The final frequency be fixed later (maybe years) when the timing group and clock users agree on its value.

P.Goettlicher was nominated as our representative in the decision making body. He should inform us of who else is on this committee and how it intends to make the decision. Our preference is 5MHz.

See the AGIPD FEE section for a discussion of what frequency should be generated and sent to the FEE modules.

4 10 GE status – I.Sheviakov

Using the XPM test system FPGA-FPGA and FPGA-PC UDP bandwidths of 98% and 70%, respectively, have been measured. A bit transmission error rate (BTE) of 10^{-15} was measured when operating the test system in the temperature range 20 - 70°C. The same BTE is also seen for different layouts. These numbers are excellent and sufficient for our needs.

The layout for a two PHY chips on FMC mezzanine has been finalized, see slides for details. Components on the FMC are 2 x VXC8486, 2 x SFP+ (incl. cage) and DC-DC power converter and filter. A connector pin allocation was recommended.
IPMI support should also be present to support interrogation and identification of what is on the mezzanine. The ability to interrogate EPROM form the carrier would be sufficient.

Work has started on testing a 50 MHz ADC system – a requirement for the AGIPD FEE. Test waveforms are inputted into a single ADC channel and the resulting digitized result are stored to DDR2 memory via a Vertex 5VFX70T FPGA. First results are encouraging.

Issues and plans where discussed. The two PHY/SFP+ FMC mezzanine design will be used as basic building blocks for the TB and LPD and AGIPD FEE systems. DSSC will use it as a fallback solution – they expect a high end Vertex 6 FPGA to be available which should be able to directly drive the SFP+ module. When the FPGA would be available is not known at the moment.
The first prototype version of the FMC would be available for testing in the next few months.

5 Software status – C.Youngman

The software concept for XFEL DAQ and control was briefly presented. The intention is to provide tight standalone implementations of for each experiment, where an experiment is defined to be all the sub-systems required to make a measurement, e.g a 2D pixel detector, other required detectors, beam line and machine systems, etc.

Software development has started based on Glassfish applications servers and NetBeans IDE. These solutions address issues like: deployment, configuration, resource management, accelerated coding, etc. At the moment the application client container is seen as a required building block for most applications, which, amongst other things, guarantees web start-ability (used by the Job Control). Although EE5 features are used the solutions aimed for are not restricted to Java.

A dummy system based on the requirements of AGIPD has been constructed following the above concepts; see slides for details and description of the simplified run control test system.

During the next few weeks work would concentrate on the AGIPD dummy system. A video conference should be targeted for the end of July to inform offsite groups.

6 TB status – J.Coughlan

The TB development was reviewed at the 11th May IKRC and the project recommended. Problems associated with UK in-kind contributions remain – a solution is required.

Tests of memory interfaces using FPGA evaluation boards continue. Both hard core embedded memory controllers and soft core Multi-Port Memory Controllers are being investigated. The aim has been to understand the maximum throughput for varying clock speeds, data block sizes, numbers of DMA engines used, single r/w access and concurrent r/w access. A number of non-understood features have been identified, e.g. different single r/w rates as a function of engines used, a drop from the expected maximum throughput when increasing the number of engines above 2, etc. These observations have been queried with the manufacturer, once resolved it should allow a meaningful optimization to be performed. No show stoppers are currently seen.

Work has been continuing on understanding and designing the FPGA to cross point switch implementation. Rob has been looking into the re-establish clock synchronization recovery time after breaking the link (moving to the next switch position) by using an FPGA evaluation board and emulating the break using: ML507, GTX SATA data source, and loopback with and without external connection. Reconnect times of 5-6µs appear to be required but it may be possible to switch very quickly without loosing synchronization. More tests are being prepared. A ML523 evaluation board has been ordered which will allow improved measurements.

7 AGIPD FEE status – P.Goettlicher

No significant changes have been made since the last meeting.

Parameters of the C&C delivered continuous “100MHz” clock were discussed. Requirements of the 2D pixel detectors are:

- AGIPD = as close to 100MHz as possible but slightly less
- DSSC = 95 to 100MHz, m = 1 please.
- LPD = ideally 100MHz , lower if required.

M.Postranecky will look at the datasheets of the PLL he favours using and produce a table about what frequencies can be delivered.

8 DSSC FEE status – T.Gerlach

A schematic of the current sensor module layout, mainboard and DAQ module were shown, see the slides. The mainboard is based around a Vertex 6 (!) FPGA and shows input C&C lines, JTAG connections and interconnections to the DAQ module. The clock, control and status signals used were listed.

The MPRACE development, used in previous applications developed by the group, is being used to test PLL and 10GE characteristics. If possible the Vertex 6 will be used to directly drive the SFP+ module making the use of a PHY chip obsolete. The DESY FEA PHY/SFP+ development will be used if the direct solution is not available.

Open questions and issues: C&C timing specs and event telegram specs from the timing system.

9 LPD FEE status – J.Coughlan

The Front End Module (FEM) card revision resulting from the move to flat panels and power changes has been completed. The new mechanical layout of a 16 module detector was shown.

As recommended at the XDAC review the LPD has implemented a 10 deep Veto/Trigger ASIC buffer. This opportunity has been used to add functionality in that the Veto/Trigger input signal is now a 4-8 bit word, which allows use for additional purposes. Interestingly AGIPD were asked by the XDAC review committee to look into a 2 deep buffer.

Next steps include fixing the FEE detector signal interface, working on the pcb schematic capture, and designing logic for control and data path for the Veto/Triggered ASIC design.

10 C&C status – M.Postranecky

Now that Timing Receiver board delivery of a glitch free continuous clock has been guaranteed by the XFEL timing group design can proceed (even if the precise frequency has not yet been defined.)

Note was taken that LPD and AGIPD may have different length Veto/Trigger buffers with correspondingly different signal latencies.

The master and slave board design has been reviewed. Of the alternatives presented, see slides, the "single integrated card" solution was chosen as the most economic.

Tyco Electronics Stacked RJ45 Modular Jacks for AdvancedTCA have been ordered. At the last meeting there was uncertainty about whether the plug batteries could really be purchased.

Open issues:

- **The FEE groups should decide where the fast signal lines are isolated. The general feeling was that this should be done at the detector head - this needs to be confirmed by the FEE experts (or counter proposals made and justified).**
- **As stated previously Martin will look at the datasheets of the PLL he favours using and produce a table about what frequencies can be delivered.**

11 AOB

Andreas was thanked for organizing the meeting and for testing whether the people attending could reconfigure from DHCP to static IP addressing on their laptops.

The format of the meeting was discussed – it should continue in its present form with quarterly meetings.

The next meeting will be on Thursday, 22nd Oct 2009 in DESY.