# Minutes of the Train Builder meeting (20.1.2011)

Location: conference room 12, building 68, Rutherford Lab, England.
(22.1.2011 - CY)



## 1 Attendance list

WP76: N.Coppola, D.Wilson and C.Youngman.
LPD+TB: B.Halsall, J.Coughlan, C.Day, T,Nicholls and XX
AGIPG: P.Goettlicher
DSSC: T.Gerlach.
UCL: S.Cook, E.Motuk, M.Postranecky, M.Warren and M.Wing

The minutes, agenda and talks are reachable via:
http://www.xfel.eu/project/organization/work_packages/wp_76/daq/2d_pixel_detectors/meetings/ .

**Actions are rendered bold.** Items of importance are underlined.

If you do not have time or do not want to read entire document, then skip to the summary and actions.

## 2 Welcome and site information – J.Coughlan

Organizational issues and welcome.

## 3 Last meeting actions and purpose of meeting – C.Youngman

Last meeting action status:

- **1.** *Get consecutive digitisations measurements made by STRUCK FADC board*. Work with the STRUCK board was delayed by RTM development – see Dana's talk .
- **2.** *Send the cost of the single crate DAQ xTCA for Physics equipment to Matthew*. The costs were: Schroff 6 slot crate 2058€, CPU 1382€, MCH 2142€ and disk carrier 324€.
- **3.** *A decision is required from UCL on whether they can provide the firmware modules for sending and receiving over the telegram data and strobe lines.* The firmware was prepared and given to Kay – there has been no feedback. We must put the firmware module into the DESY FPGA expert forum registry and UCL must participate (UCL video conference?) in the meetings.

- **4.** *An offline discussion and decision concerning the possibility using TB for Medipix3 is needed.* Discussions (us: JC, MZ and CY; them: David Pennicard) resulted in the decision not to use the TB for Medipix3 readout as their requirements can be satisfied by a multi NIC PC readout system (the 10Gbps link count is low ~3.)
- **5.** *Manfred should retransmit the list of number of PHYs ordered by which group. The groups should send back an update of the numbers required.* This was done see FEA talk slide 2 – there were no replies. See Manfred's slides.

The aims of this meeting are listed below, see summary of meeting for results:

- Review of progress, open issues, etc.
- Would like to have a discussion of TB development issues: concepts for larger than 1 Mpxl detectors, and roadmap of development including dates when decisions have to be made, e.g. use of Vertex 7, final card design, etc.
- Review time schedules both TB and CC and discuss how these fit with the detector plans (see slide 8 of this talk).
- The next progress report for the UCL CC contract has to be written – its contents will depend on today's update.

# 4 TB status – J.Coughlan

An 8 link ATCA demonstrator will be built. The 4 link MTCA demonstrator will not be built. This decision is based on: proving techniques (memory, X-point, etc.) on development boards have been completed, layout and routing on MTCA are restrictively tight for the demonstrator functionality, as is the PCB thickness limit (1.6mm). Therefore we go straight to ATCA form factor required by the final design.

The 8 link demonstrator design is shown on slide 5. The 8 link demonstrator board can be used in a number of configurations: 4 in 4 out (loop back and small scale tests), 8 in or 8 out (two such boards linked over the Z2 backplane = ½ Mpxl detector), etc.

The status of the ATCA demonstrator is:

- Concentrating initially on layout of the FE unit :
- FE Circuit schematics ~ complete.
- In parallel PCB layout and routing is in progress
- Starting with conservative pcb build based on LPD FEM design.
- Investigating options using blind vias (incremental pcb build ; 2 x 8 layers)
- Trying to add QDRII SRAM as a test for Image Manipulation Unit.

Possible configurations for 1 and 2 Mpxl detectors, based on the ATCA and using conservative technological assumptions, were reviewed on slides 11 thru 14. Larger systems using higher density, coming technologies, in single and multiple crates were reviewed on slides 18 and 19. A development roadmap was shown on slide 20. The Nov. 2010 updated TB schedule was shown on slide 21. ATCA demonstrator testing starts end of Q3/2011.

Technology developments include:

- Doubling the number of optical links per unit real estate
- Use of Xilinx FPGA Vertex 7
- Increased lane speed 3.125 to 6.25Gbps
- Increased memory speeds

Additional discussion items:

- Board power requirements are expected to be ~100W, i.e. below the 200W limit.
- On-the-fly data formatting – there is a need to understand what data formatting is required and possible. **A working group on data formats should be initiated with the detector groups.**
- Maximum fibre lengths – the option of connecting FEEs to the TB located in the Balcony computer services rooms should not be forgotten. The distance required is ~100m.
- The Requirement of having an in crate processor board for configuration needs to be understood, where could it go, or can the master FPGA run a soft core OS connected to Ethernet connected through the backplane (requires Hub).
- **Producing a short 1-2 slide roadmap note for input into the next XDAC should be aimed at (JC, CY and MK WP75).**

It is clear that the ATCA demonstrator can be used to provide 1Mpxl readout system which should buy time before having to decide on a final board design and technologies in 2012. It is assumed that the demonstrator board will be used in detector tests 2012-2014.

Discussion with JC after meeting: WP76 would like to have 1-2 ATCA demonstrator board for driving packets into the slice test equipment to be purchased in 2011. The functionality required: synchronized sending of data on links, configuration of inter gap delay, configuration of IP end points, etc. This will allow testing multi NIC switch performance functionality.

# 5 TB cross-point switch – R. Halsall

Rob confirmed that simple UDP protocols will be supported FEE (for LPD = FEM) to TB and TB to PClayer. Other protocols are possible and may be used.

The payload format of UDP packets sent from the FEM to TB data was described. Verification of integrity (in train) and train delimit require identifier and count fields per packet (i.e. UDP header), any detector metadata, then the pixel data. Packet aggregation into the TB output link memory and then to the PC layer are shown in slide 7 and 8, respectively. Error detection, flagging and recovery were discussed – these problems should be resolved as in other detectors.

The 10Gbps UDP transfer protocol is being implemented by Rob, the third implementation after Igor and Thomas! Rob's schedule:

- Local Link UDP XAUI Block – In progress
- Prepare for LPD FEM Testing…
- Combine with ML510 TB Emulation
- Work on TB -> PC protocol

# 6 FEA status – P.Goettlicher (for M.Zimmer and I.Sheviakov)

Vitesse PHY status: 160 PHYs were ordered (minimal quantity) 4 used for FMC modules, 156 still available. Current distribution foresees:

- 112 Units required (counted by Chris):
- 12 TB (Q1/2010) ... From XFEL budget
- 40 LPD (Q1/2011) ...
- 10 DSSC From detector budget
- 50 AGIPD

This was the allocation required for the contracted 1Mpxl detectors with their train builders. **It is necessary to plan the production of finished FMCs, this must be organized as an action.**

The first batch of 20 DAMC2 MTCA4 boards is now available (and tested). Boards are being distributed to their end users. WP76 and UCL have 1 each. Please check slides 4 and 5 for the test and known problem list. - unfortunately some small bugs, but NO showstoppers. Early Feedback for next Revision is highly welcome.

An all in MTCA4 for Physics crate, cpu, hub, disk, graphics card, and extenders is now available from NAT (slide 8) – the cost is 5555 k€.

The high error rate seen on the dual fibre link FMC delivered to STFC reported at the last meeting was investigated and found to result from a small break in one line of a differential XAUI pair.

# 7 MTCA4 Phys crate and STRUCK SIS8300 status – D.Wilson

Work with the STRUCK board was delayed by RTM development and STRUCK delivery delays. Next step is to connect the RTM with the correct power on protocol.

Setting up the MTCA4: OS installation on CPU and IPMI command line and graphics tools NATview foir interrogating the board content of the crate was described. The aim is to have a standard setup defined on a distributable media, e.g. USB stick. This installation could be of use to UCL – provided it works.

The current status of the STRUCK RTM for APD were described. WP76 now has two MTCA4 Schroff crate systems, 2 STRUCK boards, 1 DAMC2 and 1 TR board.

At the next DESY FPGA meeting the blocks required by each user of the STRUCK board has been requested (improved coordination of firmware development?).

# 8 C&C status – E.Motuk

The current status was summarized:

- Software for design (Allegro ConceptHDL) are available and the workflow for production of PCBs has been setup.
- The PCB test card (PC3461M) for testing bussed data telegram and Fast signal transmit and receive is designed and is in manufacture and assembly. The board could be used by other groups if required.
- The schematic entry design of the prototype RTM for the CC has started. This board will be used as a test bed for CC functionality. A Schroff xTCA crate system has been acquired and setup for testing RTM and DAMC2.

The DAMC2 firmware blocks currently anticipated were defined: receive telegram, fast message transmit, register block, external trigger and PCIe blocks.

Now that the DAMC2 is onsite and the TR board will arrive soon work with these systems can begin. Documentation and and any experience from other groups will be appreciate. **Erdem should be placed on the DESY FPGA expert email list and attend the meetings.**

The immediate schedule for PC3461M, RTM and DAMC2 boards was shown (slide 16). Usage of CC in detector tests with detector tests should also be discussed with WP75, see actions.

# 9 LPD FEE status – J.Coughlan

Issues solved since the last meeting:

- The size limitation of 256MB when accessing DDR2 memory has been overcome by setting the correct controller parameter – thanks go to the Xilinx for their help. Now working with 512MB and will look at 1GB soon.

The FEE FEM (h/w, s/w and firmware development) is almost ready! The status was summarized, as below, with pictures of the delivered FEM board.

- LPD DAQ status
  - ASIC. Wafers being diced at CERN. 150 chips expected at RAL end of Jan.
  - Super Module (1/16 = 1 FEE link) tests at RAL not before Q2/2011
- FEE (FEM) card design (Saeed Taghavi, Chris Day)
  - First 2 FEM cards received this week.
  - Not powered yet.
  - Test cards are also ready.
- FPGA Firmware & Embedded S/W (Rob Halsall, Sam Cook, John Coughlan)
  - ASIC Slow controls interface tested on dev board.
  - ASIC Fast controls interface tested in simulation.
  - PPC Memory Controller is now working with 512 MByte DDR2 SODIMMs.

# 10 DSSC FEE status – T.Gerlach

Issues solved since the last meeting:

- The 10Gbps link connection problems reported were solved – the TX and RX lines had been swapped. Now the link works as expected.
- PPL jitter problems were fixed by using the correct, undocumented, setup parameter. Now 800MHz frequencies can be accurately generated from the 100MHz distributed clock.

IO board schematics and routing are done. Manufacture of the flexible PCB with 50 micron conductors has been tested and appears to be useable. A summary of next steps was given, show stoppers were not present.

# 11 AGIPD FEE status – P.Goettlicher

Issues addressed since last meeting

- Circuit design of modules continues
- ASIC prototypes being used to test random access cell addressing for VETO usage

Investigations of reducing the readout size by selecting only pixel regions around areas of interest for readout are being made. Which regions would be selected in calibration runs. Will this really be useful??

Larger than 1 Mpxl configurations were shown – due to the quadrant back the number of CC links scales less quickly than the number of modules, see slide 3.

Data format and ordering potential where summarized in slide 4.

# 12 Software status – C.Youngman

The work of Krzysztof Wrona and Burkhard Heisen for DM are coming into the DAQ software environment, not just the configuration which was the initial track. JavaFX is no longer a good

candidate for GUI and Qt is being looked at. The Java only DAQ software solution also is changing and C++/boost is, again through the DM developments, a possible solution. In short, many changes are envisaged - more at the next meeting.

# 13 Summary of meeting

TB, CC and detector FEE work is progressing – no show stoppers are seen. The LPD is expected to provide the first working super module system.

The TB demonstrator board will be produced as an ATCA board, rather than micro-TCA.

The CC group receieved their first DAMC2 and will get a TR board next week.

The discussion of TB development issues: concepts for larger than 1 Mpxl detectors, and roadmap of development including dates when decisions have to be made, e.g. use of Vertex 7, final card design, etc. were held and will be documented see action 3.

Reviewing time schedules for both TB and CC and discussing how these fit with the detector development is planned (action 1).

# 14 Actions

The list of actions:

- **1. It was agreed to organize, in the near future, a meeting (EVO…) with Marcus Kuester (WP75) to coordinate TB, CC and detector test requirements.**
- **2. A working group on data formats should be initiated with the detector groups.**
- **3. Producing a short 1-2 slide roadmap note for input into the next XDAC should be aimed at (JC, CY and MK WP75).**
- **4. It is necessary to plan the production of finished FMCs, this must be organized as an action.**
- **5. Erdem should be placed on the DESY FPGA expert email list and attend the meetings.**
- **6. Document data format as understood now for discussion at the next meeting.**

# 15 AoB

The next meeting will be held in Hamburg on 5.May.2011 (date to be confirmed).