# Common timing and control system

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XFEL timing structure
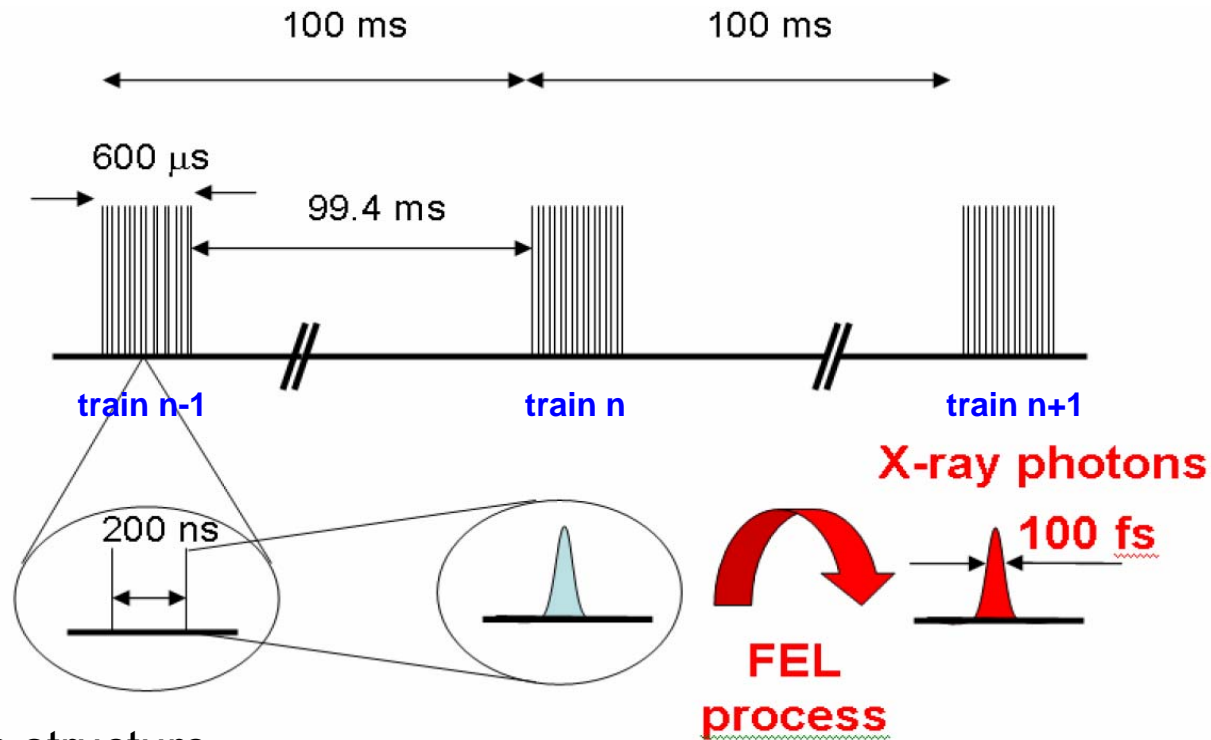
- ▌ Bunch structure
  - ▐ 10 Hz repetition rate, 30Hz option talked about.
  - ▐ 5 MHz e-bunch rate (200ns)
  - ▐ Fixed RF 600µs flat top = 3000 e-bunches
  - ▐ E_{beam} = 17.5 GeV, max = 22 GeV
 - ▐ Photon bunches produced when e-bunch pass FEL undulator

Beam distribution

■ Beam lines

   ■ 5 beam lines planned, SASE 1,2+3 at XFEL startup.

   ■ All lines receive photons concurrently

   ■ 2-3 detectors per line, one gets beam

   ■ Flat top kicker splits e-beam, requires 20µs = 100 bunches (no dump)

   ■ Fast kicker removes single bunches (e.g. during flat top change)

   ■ Electron gun can generate any bunch pattern

   ■ Max ~1500 bunches per line (max dump energy)
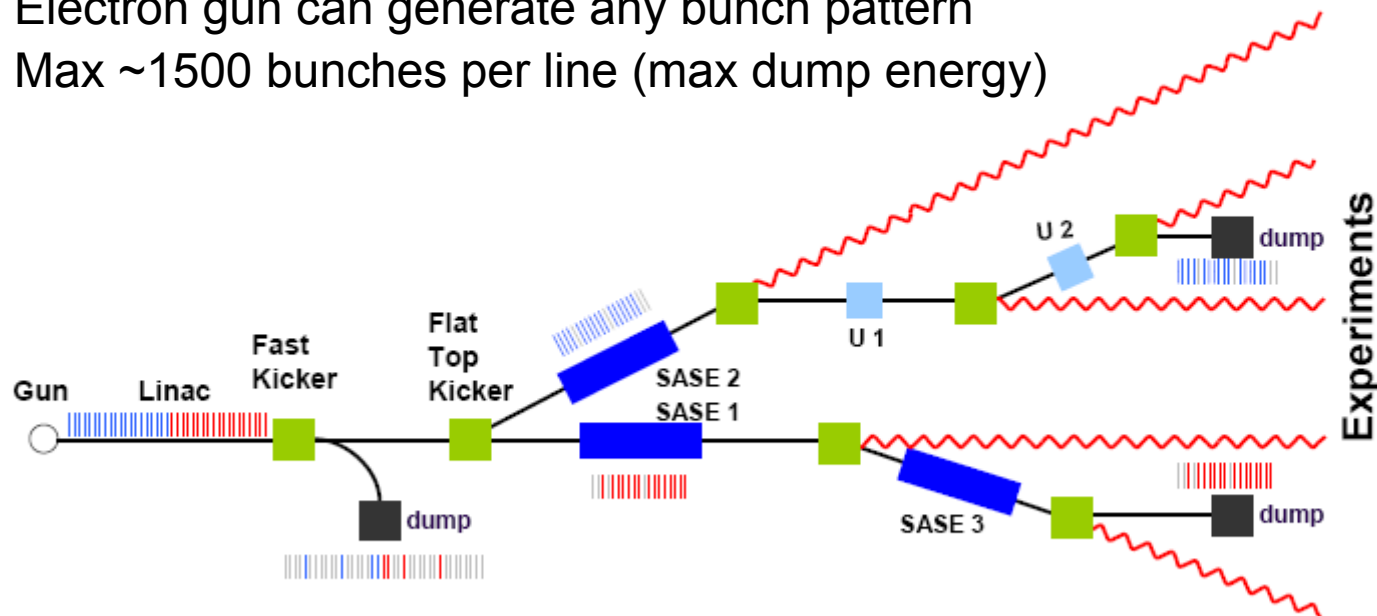
Timing signal generation and distribution
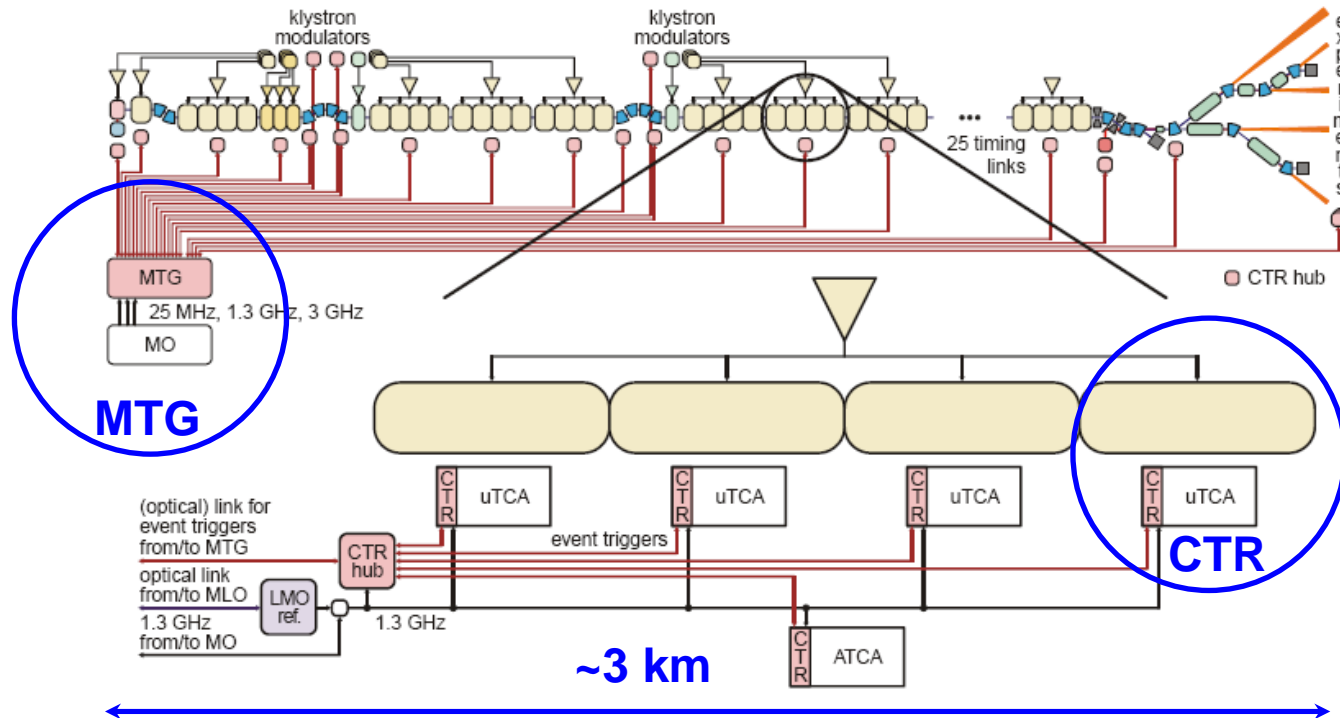
- Master Timing Generator (MTG) generates 25MHz, 1.3GHz, 3GHz
- MTG signals driven through fibre to Clock and Timing Relays (CTR)
- CTRs are used electron beam, but also in photon beam line for expts.
- Experiments Timing receivers (TR) receive signals at the experiment
- By measuring round trip times and delay offsetting at the TRs triggers are generated with correct absolute time.
- Triggers must be sent advanced in time by > largest delay to CTR/TR

Timing hardware implementation for XFEL

- TR being implemented as an AMC board.
    - Coordination Kay Rehlich head of MCS4 DESY group
    - Collaboration with Stockholm group – new to TCA and AMC hardware
    - Petr Vetrov (FEA M.Zimmer's group) contact for AMC development
- Documentation
    - General discussion paper (included) otherwise none
- Status
    - pre-prototype test of chipset stability done – results OK
    - prototype expect spring 2009

Vetrov board, but not the TR

Hardware: xTCA

AdvancedMC™

Timing receiver board size

AdvancedTCA

μTCA™
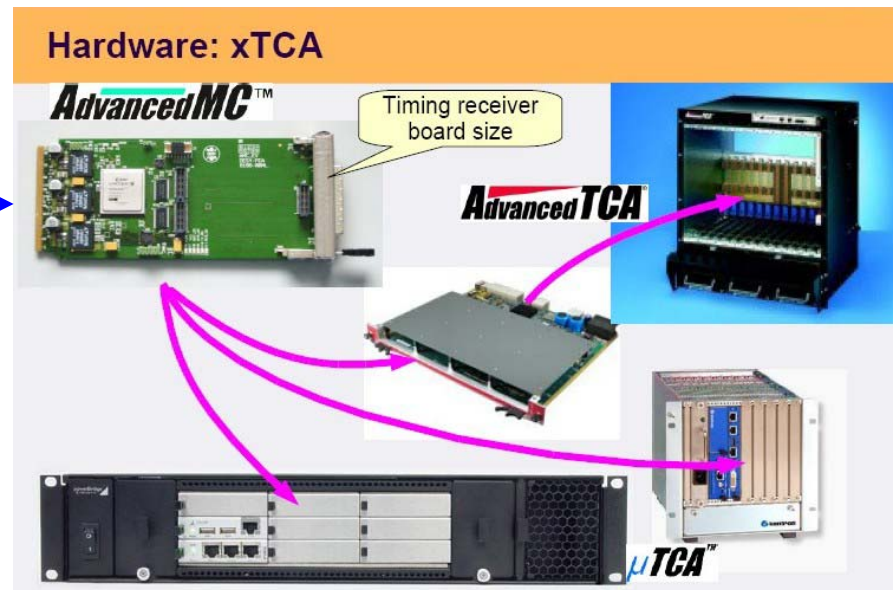
Timing signal handling

Timing schematic of
e-machine RF events

klystron hv transformer

approx. 15 ms

rf drive

0.8 ms

rf within cavities

bunch trigger

start piezo

start beam

'read out'
to front
ends

start rf

rf pulse type send to
front end electronics

start hv bouncer

start klystron hv transformer

event trigger, indicating rf pulse type
broadcast by master timing generator

'read out' at
rf pulse end

e

Start bunch train
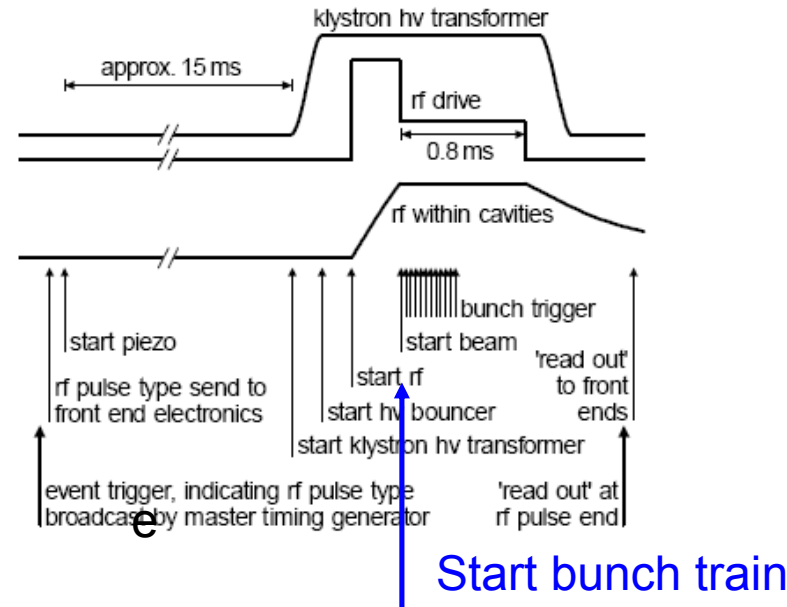
- The TR generates a trigger when an schedule action happens
  - Single pulse TLT (as on) on
  - Interrupt can be generated (PCIe backplane) on a blade in the AMC crate
- An event trigger is a trigger plus accompanying data (telegram)
  - To get the telegram content must read after interrupt (also LAN distributed)
- On FLASH TR Manchester coding used to encode trigger and data onto clock
- Accuracy of trigger is in pico-sec range = satisfies detector ns requirement

Control signals required by pixel detectors

■ Signals sent to front ends (continuously)
- ■ Start bunch train (from timing system)
- ■ delivered bunch frequency (nominally 5MHz, from timing system)
- ■ standard 5MHz clock
- ■ fast veto (external veto)
- ■ busy (e.g. from TB)
- ■ anything else?

■ Configuration Information sent to from end (before each train)
- ■ Train number (from timing system)
- ■ Bunch pattern (timing system telegram or LAN?)
- ■ Calibration patterns (e.g. pedestal triggers in empty bunches, others)
- ■ anything else?

■ Signals sent back from front end
- ■ none?
- ■ Data sent to TB must contain Train number for event integrity checks

Control signal implementation
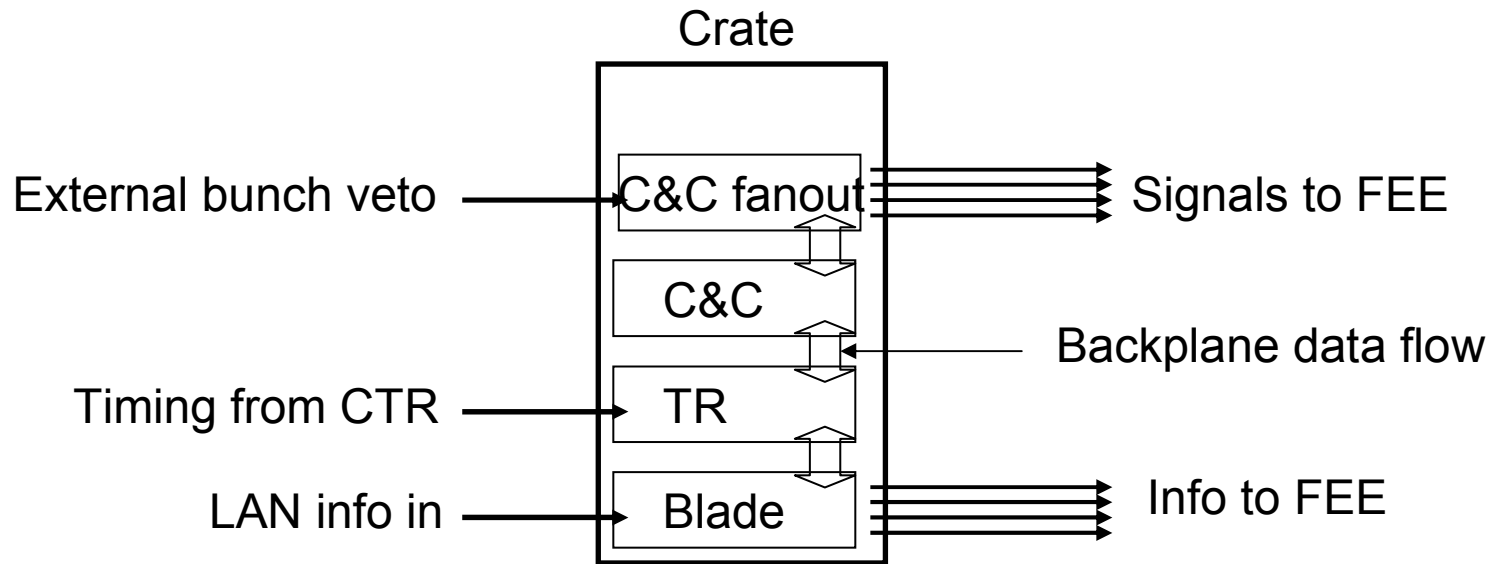
- TR = XFEL AMC timing board
- C&C = clock and control card (additional clock generation, delays, …)
- C&C fanout = fans out C&C signals to FEE
- Blade = receives LAN info (Calibration patterns, etc) also telegrams from TR (bunch pattern) and distributes to FEE (either LAN or via C&C)

Running detectors at other light sources

- 2D detectors will be taken to other light sources
  - during prototype phase for tests
  - as final detectors

- Other sources
  - FLASH = 5 Hz and 800 bunches at 25 MHz
  - LCLS = 120 Hz
  - Spring8 = 120 Hz and a few bunches (?)
  - PSI, PETRA 3, etc. = ??
  - …

- Should build a timing interface/control which allows integrating to time (+ DAQ)
  - Have checked there is interest from K.Rehlich (FLASH)

How to proceed (1)

■ Looking for a group who will collaborate on building the detector interface to timing system(s) "Control signal implementation"
- ■ Need to get to the bottom of Rehlich's TR
- ■ Need an agreement with all detectors about cable, protocols, etc.
- ■ Need a spec. of the final system

■ Need full understanding of how system will work at other light sources
- ■ how to interface to other timing systems
- ■ data readout to backend; not just IP protocols – maybe not at LCLS

■ Timescales
- ■ no timing system prototype before Spring 2009
- ■ interact with Rehlich to get precise information/documentation timing.
- ■ need to get a specification of detector interface written

MVD slow control at ZEUS.

- Micro Vertex Detector slow control (PC+CANbus) at ZEUS
  - HV, LV
    - Controlled (configuration, on, off, …) and monitored by PC (each 512 channels)
  - Temperature, Humidity
    - Sensors monitored by PC (~100 channels)
  - Cooling
    - embedded PLD monitored: P, T, H, water pump, valves, ... (~10)
    - Controlled (on, off) and monitored by PC
    - warning and error thresholds settable from PC
    - if error switch off cooling and open alarm contact to interlock
  - Interlock
    - PLD/SPS monitored, inputs (cooling, switches, no control PC deadmans handle) close/open (OK/Alarm) OR'd. (~4)
    - Switch HV and LV crates off on alarm
  - Switches
    - Bimetal temp switches (4)
    - Emergency off switch (1)
- Pixel detectors may have additional requirements
  - Vacuum
    - assume controlled and monitored (P) by PC
    - assume Input into interlock

Size and number of subcomponents matches those of 1Mpixel detectors

Slow control ideas

- Follow same ideas
  - Use IP as field bus (instead of CANbus at MVD)
  - Use PC to monitor and control.
  - Independent interlock system (not part of cooling system which are often sold with such functionality) manually bridge inputs which are not required i.e. during testing phase.
  - Use similar FSM software to turn on/off system, allows "HV on only when LV on" type clauses.
  - Means that: cooling and vacuum systems need to provide open/close inputs to interlock when status OK/ALARM

- Do not repeat same mistakes
  - Allow state of inputs and mask driving off (alarm set mask) to be read!
  - Power distribution 3-phase monitor no phase if any phase is missing – might not be part of the system.
  - …

- Software
  - Look at OPC over TCP for connections to components (must be linux)
  - Need control and monitoring functionality

Slow control ideas

- Who is responsible for what
  - HV and LV = single common solution
  - Interlock = single common solution
  - Cooling = detector specific, but common sw and interlock APIs
  - Vacuum = detector specific, but common sw and interlock APIs
  - FEE sensors (temp, humidity, …) = detector specific, but common sw API. Could have interlock inputs but more likely to be sw.

- Unknowns
  - Non FEE sensors = could use common IO device, if needed.

- Manpower
  - MVD SC implementation required during 1year:
    - 0.3 coordinators
    - 2 man team to build CANbus interface and program custom LV hardware from scratch
    - 1.5 programmers (interface to: HV Iseg, interlock EASY30, cooling, LV)
    - 0.25 electrical technician produce NIM&TTL to OPEN/CLOSE plus simple logic modules
  - 2D pixel if everything of the shelf
    - 1-2 years of phycists programmer for selecting/testing and integrating
    - If custom interlock then some el. Technician time required.
    -

- Software
  - OPC over TCP for connections to subcomponents
  - Need control and monitoring functionality on PC

Example HV and LV implementation

- As and exercise
  - Asked for and received initial specification of HV+LV requirements
  - Looked at what was on the market
  - Looked at our requirements (floating, crate solutions, IP, etc.)
  - Asked principle HEP power supply manufacturers for implementations
    - ISEG/Wiener = MVD supplier = good experience w.r.t. modification, first release of ISEG hardware usually interesting, documentation interesting.
    - CAEN = usually more expensive
  - So far received reply from ISEG/Wiener, CAEN working on it

Initial HPAD HV+LV spec. sent to ISEG/Wiener and CAEN Aug 2008

Guesstimate of LV power supply requirements for 1Mpixel HPAD detector:

	Nr. channels	V range	I per channel	ID
ASIC	4	5 thru 8V	1A	A
	4	12 thru 14V	1A	B
	32	1.25 thru 2.5V	40A	C
	32	2.5 thru 3.5V	10A	D
Analogue	16	-1 thru -2.5V	1.6A	E
	16	1.8 thru 3V	4.5A	F
	16	5 thru 8V	2A	G
Digital	16	1 thru 5V	20A	H
	16	1 thru 5V	20A	I

Guesstimate of HV power supply requirements for 1Mpixel HPAD detector:

	Nr. channels	V range	I per channel	ID
Sensors	16	0 thru -600V	few mA	K

Answer from ISEG/Wiener – MPOD ≤ 10A chans, MDH+PL > 10A chans

MPOD modules	Number	Single price	Total price	IDs used
MPV 8015	1	1765	1765	A
MPV 8008	8	1613	12904	B+F+G
MPV 8008n	2	1613	3226	E
1EHS F010n_805	1	3380	3380	K

MPOD crates	Number	Single price	Total price	
MPOD EC-LV	1	3600	3600	B+E+F+G
MPOD Mini HV	1	2790	2790	K+A

modules	Number	Single price	Total price	IDs used
MDH	32	670	21440	C+H+I

crates	Number	Single price	Total price	
PL512	5	2600	13000	
PL 508 EX	1	1900	1900	

Grand total price 64005

Better is 6xPL512 rather than 5+PL508
Better is 2xMPOD EC-R rather than 2 different MPOD crates

Iseg/Wiener MPOD

MPOD is a crate containing LV and HV power modules.

HV = ISEG (internally CANbus)
LV = Wiener (USB)

Plus a network interface.

Note that PLxxx are crate supplies for Wiener LV modules only.

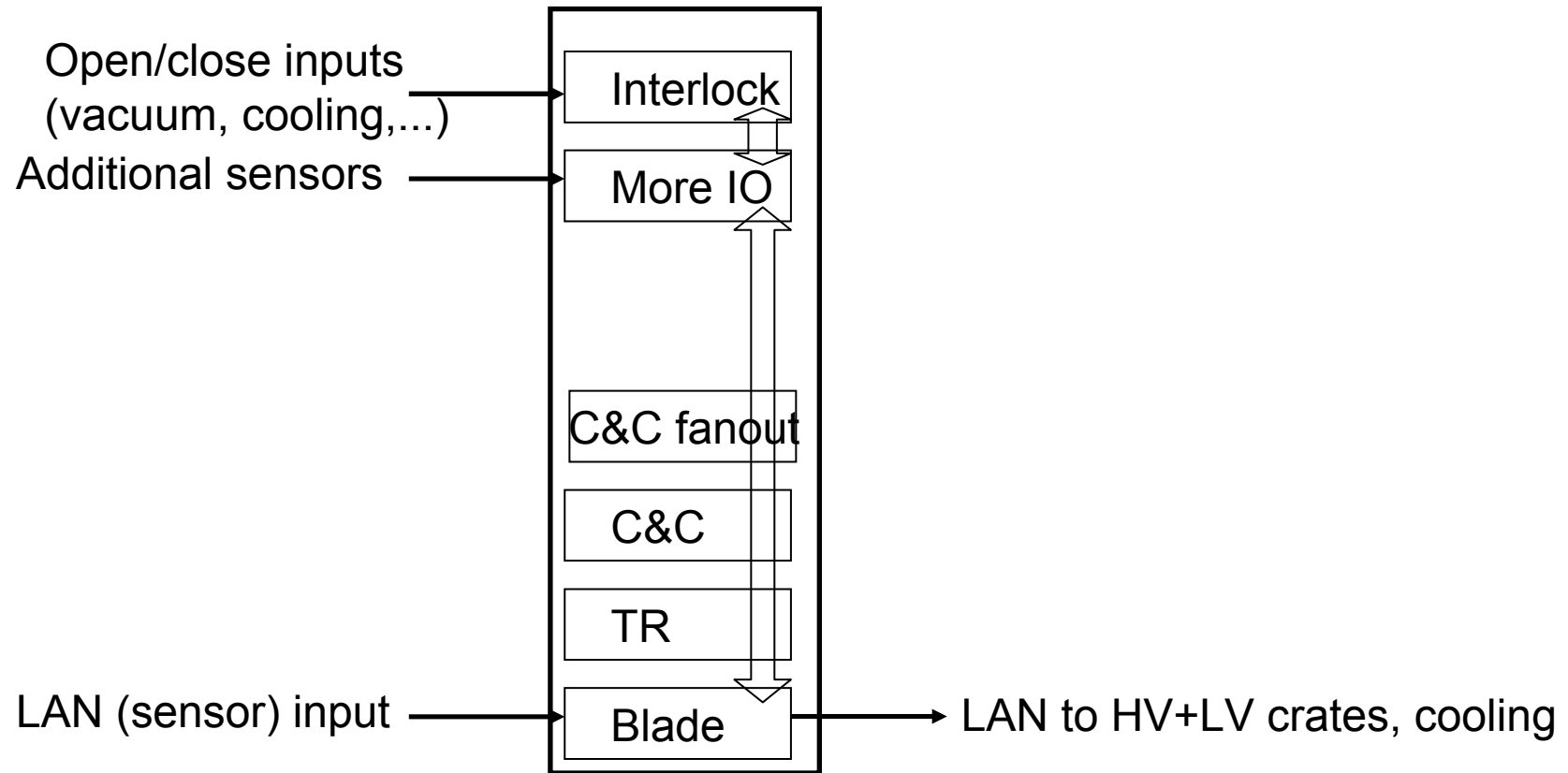## MPOD only if 20 and 40A channels are treated as an increased nr. of 10A chans

MPOD modules	Number	Single price	Total price	IDs used
MPV 8015	1	1765	1765	A
MPV 8008	8+8+16=32	1613	51616	B+F+G
MPV 8008n	2	1613	3226	E
1EHS F010n_805	1	3380	3380	K

MPOD crates	Number	Single price	Total price	
MPOD EC-LV	4	3600	14400	…
MPOD Mini HV	1	2790	2790	K+

Grand total price 77177

The MPOD only solution costs 13000 € more

Slow contol implementation

Open/close inputs
(vacuum, cooling,...)

Interlock

Additional sensors

More IO

C&C fanout

C&C

TR

LAN (sensor) input

Blade

LAN to HV+LV crates, cooling

How to proceed (2)

- Do detectors agree with the basic concept - IP fieldbus, PC monitor, etc.?
  - *Discussion needed, starting at the Oct. HPAD collab. meeting in PSI.*
  - Are people happy with "who is responsible for what"?
- Unrealistic to assume that detector HV and LV requirements are defined
  - will borrow small system (MPOD and CAEN?)
  - look at product and software, do some tests
  - hardware needed otherwise nothing gets done
- Decide what the interlock implementation is.
- Is a separate IO system needed for non FEE sensors?
- Do additional requirements exist
- Who does the common side work?
  - WP76, but need more manpower
- Have budgeted money for 2008 (blade, HV+LV test units)
- Timescales
  - need defining.
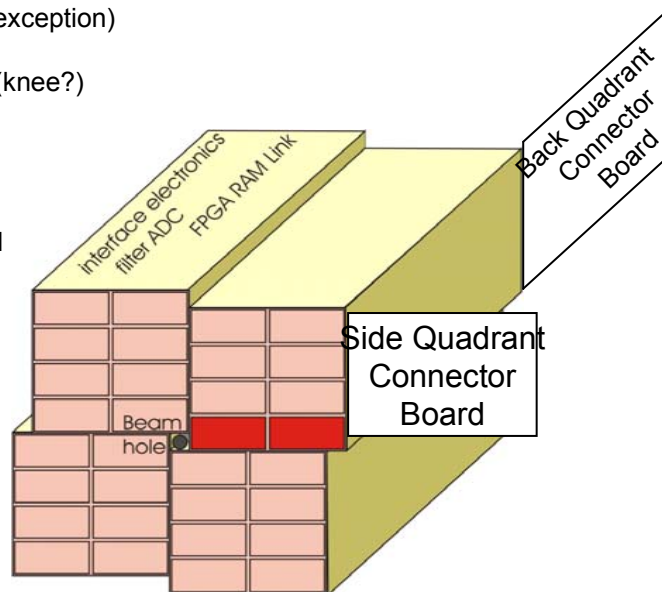 - would be useful to be testable during prototyping of detectors

Conclusions

- … see how to proceed slides

Spare slides

Sensor HV (values from deliverable example EHQ F005x_106):
- 32 HV channels (1cable per sensor)
- other guard ring voltages needed?
- Vmax = 500V (might be +ve or -ve)
- ΔV settable/readable = 10mV
- Imax = 10mA (sensor = 200 µA i.e. no rad. leakage current)
- ΔI readable = 200nA
- ΔI trip settable = ?
- Safety loop (ramp down on exception)
- Vripple ≤10mV
- V ramp speed = ? settable (knee?)
- 16 channels per board
- crate based supplies
- cable connects at SQCB
- V output floating
- needed for DQM and control

ASIC, ADC and interface LV (MPV 80XX series 50A/board):
- ?? LV channels
- Polarity/Voltages/Currents required: +?V/?A, -?V/?A
- V, I, limits, ramps, etc. settable
- V ripple ≤10mV
- Large currents (250A/quad)
- 2 crate needed, if 10A/50W per channel - check?
- safety loop ?
- cable connects at SQCB (ASIC) and BQCB (ADC + interface)
- needed for DQM, control

Interlock:
-Inputs open/close = OK/alarm
- ?? Input channels
- interlock (cooling, HV and LV, …) so that if:
   cooling fails, or
   temperature outside limits, or
   humidity outside limits, or
   emergency off switch, or
   watchdog failed, or
   slow control software off
  then HV and LV are powered off.
- PLD or SPS system required, must be independent all other PLD
- other conditions: HV on only if LV on, etc (at interlock or software).
- needed for DQM (all input states) and control

Humidity:
- ?? channels
- where are they and who reads them out – microProc
- needed for DQM

Temperature:
- at least 32 channels
- where are they and who reads them out – microProc
- values readout every train store in TINE and data archive
- needed for DQM and interlock.

Cooling:
- Environmental parameters (P, T, H …)
- needed for DQM, control (warning & error limits) and interlock

Vacuum pump:
- ?? Channels (P)
- needed for DQM, control and interlock

Interface electronics
filter ADC   FPGA RAM Link

Back Quadrant Connector Board

Side Quadrant Connector Board

Beam hole

Switches:
- Bimetal strip switches into interlock – needed/where?
- Emergency off switch into interlock.
- needed for DQM and interlock

Indicators:
- LEDs on boards when power ON
- Flashing lights like "magnets on"

Quadrant microProc:
- TCP receives next train setup information and distributes to FEE
- Readout temperature and humidity sensors? (anything else?)
- needed for DQM and control (via TCP)

Peter's 31.7.2008 guesstimate of quadrant power supply requirements
= initial specification

	Nr. channels	V range	I per channel
ASIC	1	5 thru 8V	1A
	1	12 thru 14V	1A
	8	1.25 thru 2.5V	40A
	8	2.5 thru 3.5V	10A
Analogue	4	-1 thru -2.5V	1.6A
	4	1.8 thru 3V	4.5A
	4	5 thru 8V	2A
Digital	4	1 thru 5V	20A
	4	1 thru 5V	20A

Guesstimate of quadrant sensor power supply requirements
= initial specification

	Nr. channels	V range	I per channel
Sensors	8	0 thru -600V	few mA
Guards	0	-	-