Minutes of the Train Builder meeting (4.12.2008)

C.Youngman 8.12.2008 (last revised 17.12.2008)

1 Attendance list

UCL: M.Warren, M.Postranecky and M. Wing.
DESY-FEA: M.Zimmer and I.Sheviakov.
LPD detector and TB: J.Coughlan.
AGIPD detector and DESY-FEB: P.Goettlicher.
DEPFET detector: A.Kugel.
XFEL: I.Ramos (1D detectors) and J.Gruenert (photon diagnostics).
WP76: S.Esenov and C.Youngman.

The minutes, agenda and talks are reachable via:
http://xfel.desy.de/project_group/work_packages/photon_beam_systems/wp_76_daq__control/train_builder/

2 Aim of meeting

The aim was to get an update of the: train builder, 2D pixel FEE, 10GE, and C&C status. In particular feedback from the recent Timing and C&C meetings and an update of the time line for the train builder and C&C projects were targeted. Actions are highlighted in **bold** text.

3 AGIPD (formerly HPAD) FEE status – P.Goettlicher

AGIPD's expectation w.r.t. control was restated. The control consists of: C&C (signals and clocks driving the FEE DAQ) and slow control (monitoring and control of HV, LV, temperatures, vacuum, etc. components). The run control (RC) is responsible for configuration (incl. FEE LAN), run sequencing and overall control of C&C and slow control sub-layers. RC sits above the C&C and slow control. No control functions pass through the backend. This view of the world was agreed to.

A detailed first look at the data format from the individual readout modules (16 per 1Mpixel detector) was shown assuming UDP FEE to TB transfer protocol. Train specific data sent by a module could be formatted into two record types:

- a single leading record containing meta data describing the module data of the train, and
- 16x400 (=6400) pixel data records per module and per train, containing meta data describing the pixels in the record and the pixel data payload.

The 9216 byte size proposed for both records was the same as was the 952 bytes of unused space. The other FEE detector experts thought that the proposal was a workable starting point.

The "who is responsible for what at run start" list was reviewed:

- The run start configuration (candidates are: IP address allocations, bunch patterns (to be indexed), storage cell constants, etc.) is distributed by the RC PC (or blade) down to FEE using LAN connections.
- The FEE is not responsible for sending run start configuration data to the backend. This has to be done from the control PC (or blade) to the PC layer downstream of the train builder.

There were no objections to this.

A number of "per train in-run" new and known configuration issues were raised:

- The bunch pattern index to be used must arrive early enough (old: 10-15ms should be enough – it should not be forgotten. AK)
- On receiving the "start train" timing trigger all train gap (staggered) processing stages, ADC-Format/Transmit, also stop. When the run ends there will be a requirement of flushing data out (~2 extra start trains). When the run begins there is no requirement of transmitting data for ~2 start trains. Logic to handle this must be foreseen.

At the next train builder meeting a generic definition of the data format based on the proposal of Peter should be available. (Ed. Was this the conclusion?)

The AGIPD time line was show, see Table 1.

4 LPD FEE status – J.Coughlan

Digital version of ASIC now put back, otherwise no changes. Roughly same time schedule as with AGIPD. FEE micro-controller standard Ethernet connection is currently 100Mbit/s, this may go to 1Gbit/s during the FEE development period. See first two slides.

Although the LPD and TB are both using the same pool of people, the projects are not coupled. More manpower is needed and is being looked for.

5 DEPFET FEE status – A.Kugel

DEPFET has been approved and the official launch will be in Jan/2009. In spite of this the FEE development continues!

The status is roughly the same as at the Nov. Timing/C&C meeting. Two important feedbacks are:

- The Need to test the microBlaze as a soft core controller embedded in the FPGA. Need to ensure that no time critical features exist w.r.t. in-run configuration, etc.
- **Peter Goettlicher, as the onsite FEE expert, was delegated the task of ask the timing people for confirmation that the 5MHz PLL derived TR board clock is "clean" and has no glitches.**

DEPFET time schedule for FEE related work is shown in Table 1.

The design tools used were described, see slides for AK. FEB uses: Xdesigner, Exhibition from Mentor, HyperLynx, and more(?). STFC uses: Cadense for schematic capture and PCB (Alegris(?) is PCB tool), which should match HyperLynx input. FPGA: Xilinx ISE, EDK generating netlists. HDL experience, but may be moving away from HDL. There could be some advantages if the same tools are used.

Remote download of firmware is required. Ethernet down loads are supported by Xilinx PPC cores. How to debug was also touched on, as was whether and which embedded hard cores or soft core processors (and OS) to use.

The DEPFET proposal for the format of data sent to the train builder was reviewed. The data word format will look different to that of AGIPD. TB must reorder in time and location, how can DEPFET, or any other detector, specific data handling code be made available to the train builder?

The last slide summary of open questions should be addressed (resolved) at the next meeting.

6 FEE discussion

Time milestones for the FEE, TB and C&C developments are shown in Table 1. I've not found a recent time line for LPD – the statement is that it is compatible to AGIPD. What the table shows is that the C&C evaluation board prototype should be available for testing against detector FEE developments as of Q3/2010, before this date sequencers will be required at the FEEs. The first prototype full board TB will be available Q2/2012, before this date UDP based readout interfaces will have to send data directly to PCs.

Table 1 FEE, TB and C&C time lines (in one table)

State	AGIPD	DEPFET	LPD	TB	C&C
FPGA test-mezzanine		Q1/2009			
Configuration/Monitoring Software („user interface" of FPGA)		Q4/2009			

Prototype 1 sensor + ASIC	12/2009				
C&C evaluation board prototype					Q3/2010
Definition of readout format		Q1/2010			
TB demonstrator board tests				Q4/2010	
Prototype 1 module + ASIC	10/2010				
Full 1 module + ASIC + ADC + 10GE	11/2010				
10G Output to TB		Q4/2010			
TB first full prototype board available				Q2/2012	
C&C final board tests					Q2/2012
Full Quadrant	Q3/2012				
Full Detektor		Q3/2013			

7 10GE status – M.Zimmer

The XPM PCB for 10GE development testing should arrive soon and allow tests during December. Coding and simulation of the required VHDL software blocks on the Virtex5 ML510 is underway. The development schedule foreseen is:

- December - January 2009: Electronic check of XPM module, finish XAUI and MDIO protocol implementation, and Start Tests with 10GEthernet transmission.
- February - April 2009: Implementation of 10G – UDP communication with PC, optimization of programmable parameters via error monitoring, and implementation of the full scale readout state machine from data input to PC with maximum bandwidth.

A FEA contribution to RTM of the TB was discussed. A number of open questions exist (form factor, interface definitions, power…) which need resolving before any development can start. What FEA could provided (without FPGA implementation) is: help with interface specifications, schematics and layouts, PCB production, tests, and sharing VHDL code modules developed already for AGIPD, etc..

8 Train Builder status – J.Coughlan

The TB in-kind proposal has been reworked following the Nov. timing meeting decisions (LAN only connection to C&C – no signal cables) and depending on modifications resulting from the RTM work allocation (defining a FEA contribution) decisions should be ready for submission by the end of this year.

The TB project has two phases: 1) develop a AMC format demonstrator board to prove the design, and 2) design and build the final TB. The TB demonstrator board development and tests are scheduled for completion Q4/2010, and the TB designs (form factors, final FPGA, ½ or 1 Mpixel board, etc.) will be reviewed. The first full board prototype is scheduled for Q2/2012.The TB AMC demonstrator board is not expected to be useful for the prototype detectors. Sharing the software and tools used is useful.

The current status of the TB development preparation was reviewed:

- Quotes for xTCA (M.Zimmer xTCA system; crate, CPU etc.) hardware have been obtained, the intension is to buy the same equipment.

- PICMG trade consortium for xTCA development joined; now reading full TCA specs.
- Initial component selection FPGA (V5 FX70T FF1136), Crosspoint switch (Mindspeed M21141)
- Important memory decision open: SORDIMMs or DRAMs. DIMMS are significantly cheaper. Start looking at memory interface options.
- Decided to go ahead with FMC VITA57 mezzanine for Opto TRx plug (high performance samtec connector) on modules to AMC demonstrator board. Test boards without detectors use loopback tests.
- Getting a generic AMC FEA board is proving difficult as they are already sold out; a new version is being prepared as some components are no longer available.
- MMU micro controller – need to know which micro to use where software is known to exits. **Manfred Zimmer would find out what was used and the lifetime of the software used/assumed.**

The next steps will be to start working on the design layouts for the various boards.

Note that there is a US firm producing dual SFP+ on a mezzanine and an AMC, which might be worth looking at but probably is uses a proprietary protocol (AMC and mezzanine can only be sold (and work) together.)

Aspects of using the same development tools and sharing modules developed were also discussed – see last slide.

9 TB, RTM and other discussion points

The decision on whether the RTM as originally foreseen depends our side development results and technology developments. A decision should be made in 2010 – no RTM developments are required in 2009 (check again in Q3-4/2010 for funding 2011/12).

Sharing software and using the best versions would be very useful. The LHC experience was not good, but collaborative tool development is going on (M.Warren). Obvious recommendations: do not recommend using obscure tools, keep linux on the blades and not in the FPGA, and set up a twiki for sharing software.

10 C&C status – M.Postranecky

The in-kind C&C proposal is being prepared and should be submitted by the end of the year. Like the TB, the C&C has a two phase development: 1) an evaluation board prototype which should be useable by the FEE detectors, and 2) the final system implementation.

The fast signal and clock requirements of the C&C system were reviewed. Note that the configuration of the FEE will be performed through micro-processors using a network protocol like TCP.

The start and stop (encoded) trigger signals will be synchronised to the 100MHz clock. The veto pulse is synchronized, as soon as possible, to 100MHz clock and distributed to

FEE. It was agreed that all the fast signal cables will have the same length. No immediate decision was made to the suggestion of having no delays at the output of the C&C slave. The 5MHz clock no glitch open question remains – it should be resolved by P.Goettlicher, see above.

How to implement the fan-outs and fan-ins is being thought through. Hanging a module off the FEE, which would reduce the number of C&C slave boards, was not liked. The problem of finding a high density reliable connector (HDMI…) was discussed, no decision was made and C&C group will keep looking for a solution.

The following questions were put and answers (a.) given:

1) TRIGGER "Telegram" from TR : same line / different lines for TRIGGER, Train ID, Bunch Pattern ?? Bunch Pattern or Pattern ID ? (Pattern ID look-up table on C+C ??)
   a. connection between TR and backplane; telegram IDs must be inserted into the telegram; what happens if the tables are changed.

2) FEE feedback line : Status only (e.g.. Normally floating high, pulled low by FEE when powered), or will contain information (e.g.. go high when 'busy' or 'error') ??
   a. Keep simple, no information.

3) External clock input at other test sites : - 20 MHz range ?? Always use internal 100MHz clock or PLL to different clock ??
   a. use PLL fast clock (e.g. 1-20MHz)

4) Bunch Veto signal – how fast / latency ??
   a. bunch veto synchronized to 100MHz clock, see above.

5) Calibration Pattern ?? (pre-loaded into a memory on C+C ??)
   a. It is distributed by LAN from the run control.

6) Veto Disable Pattern ??
   a. veto disable pattern is used to prevent the veto rejecting a required pulse, e.g. a calibration pulse. It is distributed by LAN from the run control.

7) 100 MHz clock output : - max. jitter ?? - programmable delay / step size ??
   a. decision must come from those who use the clock.

8) Output Clock / Start/Stop pulses phase relationship : - only adjustable on C+C Master, i.e. same for all FEEs ?? - same cable length for all FEEs ?? - or individual delay adjustments on each C+C FanOut => more complex FanOuts ??
   a. Use same cable lengths.

9) Connection between C+C Master and FanOuts : - on custom backplane all signals / FEE feedbacks only ?? use single or double FanOut layer ??
   a. The C&C group should decide.

10) C+C FanOut cards : - separate power on backplane => not TCA-intelligent cards ?? separate 'dumb' FanOut cards and crate ?? on / near detector => fewer cables ??
   a. Using the 3.3V, which is always on, is thought not to be a good idea.

11) LVDS connectors : - RJ45 – bulky, 4-pairs only, but can use 2x LEDsDouble-stack RJ45 – availability / height ?? HDMI - size / more signal pairs / more grounds/shielding ?? Double stack HDMI - size ?? mini-HDMI ??

a. The C&C group are asked to find a solution.

12) Is there any C&C System interface to MPS (Machine Protection System) ?

a. No, the MPS will be driven from the blade/PC.

11 Software discussion

The software situation was described. More about this at the next meeting.

12 AOB

The next meeting will be at DESY on the 26th March.