XFEL clock and control system

In kind contribution proposal

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Development and delivery of a clock and control system for 2D detectors compatible with timing structures of light sources around the world

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Introduction

Future light sources will require large 2D Megapixel detectors in order to measure precisely the diffractive patterns of the various objects to be placed in the beam-lines. Several designs of detectors exist which will also be placed in the various light sources around the world: XFEL, LCLS, Spring8, etc.. The detectors are based on different pixel technologies, but for purposes of providing clock and control data should be similar although some differences will exist. The accelerators have very different beam structures such as the frequency or intensity of interaction and therefore having one clock and control system which interfaces each accelerator to the detectors is a challenging R&D project. Therefore, a flexible clock and control system is needed which can provide the interface between the different accelerators and different detectors and also to the common data acquisition system.

The high energy physics group at University College London (UCL) proposes to design and deliver a common system which will oversee passing control, clock and configuration data for the Megapixel detectors at whichever light source they are used. The system will exploit the advances in data handling provided by the new Telecommunication Crate Architecture (TCA) standards, AdvancedTCA and MicroTCA. This will be compatible with the XFEL timing system and the data acquisition system (or train builder) which also both plan to use the TCA architecture.

The current system design has evolved from meetings and discussions with the XFEL DAQ WP76 group, the UK Science and Technology Facilities Council (STFC) group designing the train builder and the XFEL timing system group.

The work is split into two phases so as to be compatible with the detector development and the time-line for the train builder system. The project is to start on 1st January 2009 and run for 4.5 years until June 2013, or until the XFEL and detectors are complete. Phase 1 will involve building a prototype system which will be tested with prototype detectors and will be completed within 2 years. Phase 2 will be the development of the final clock and control system and integration with the detectors by 2013.

Clock and control system

Schematic of data flow

A schematic of the data flow for the readout and passing of clock and control (C&C) data for a Megapixel detector is shown in Figure 1. Each detector will be split into (e.g. 16) sub-units for the purposes of readout and C&C data. The data acquisition (DAQ) system

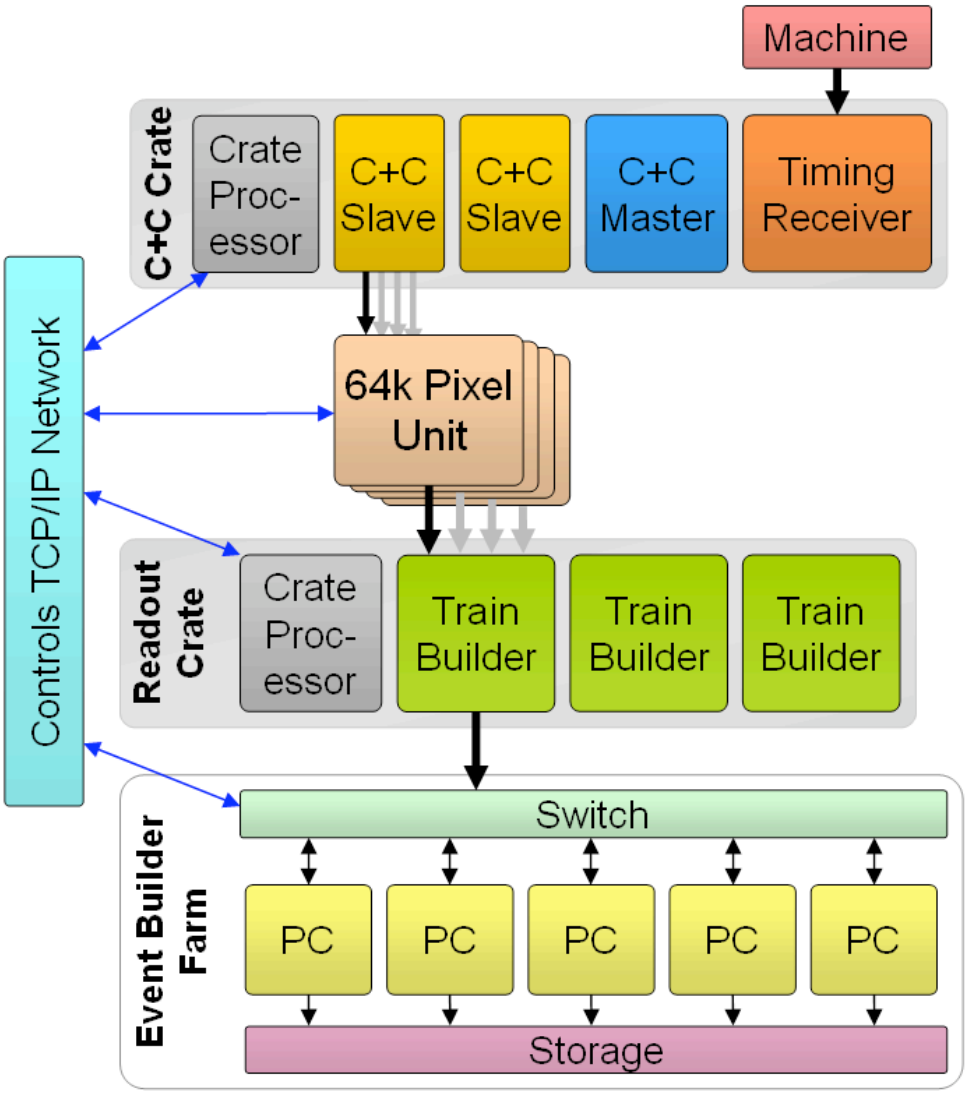

Figure 1: Schematic of readout and C&C data flow

consists of readout crates containing processor boards (Train Builder) which will collect the data and pass on to an event builder PC farm. The design and construction of the Train Builder is a separate and parallel in kind proposal from the STFC Technology

division. As this schematic indicates, the C&C system is the interface between the accelerator and the detector. The C&C system is also linked to the Train Builder via the network. The C&C crate, like the readout crate, is assumed to be a MicroTCA crate containing several Advanced Mezzanine Cards (AMCs). A timing receiver card (being designed and built by DESY) will be housed in the C&C crate and will receive timing information from the accelerator. The C&C system has a hierarchical structure with two types of boards, a Master and a Slave. A more detailed schematic of the C&C system is shown in Figure 2.

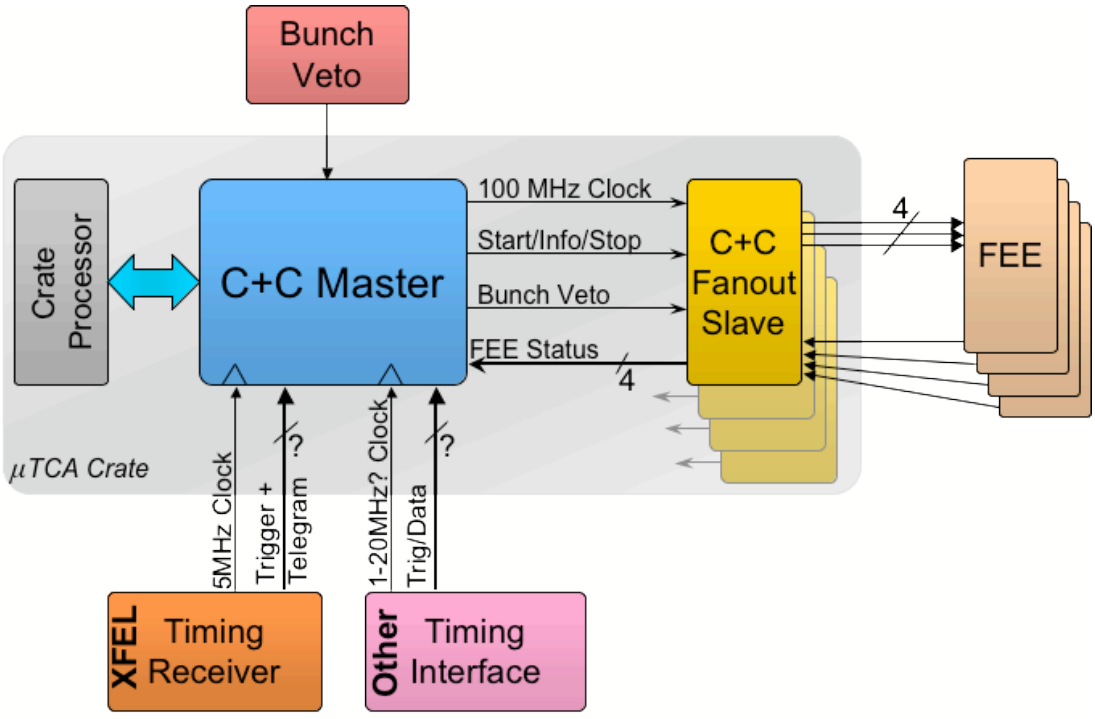

Figure 2: Overview design of the clock and control system

The C&C Master will be a high-functionality card which will link to a bunch veto signal, the crate processor, the timing receiver and numerous Slaves. It will also have an interface to other accelerators which will have (potentially very) different timing and bunch structures. The advantage of this structure is that only one complex (and costly) Master card will be needed per detector and the space-intensive connectors needed to fan-out signals to the detector will be on many simple (and cheaper) Slave boards. A typical scenario for a Megapixel detector is to have it split into 16 units for readout and C&C purposes; these detector units would then be served by 4 Slaves each with 4 connections, served by 1 Master. Communication between the Master and Slave would probably be via the crate's backplane. Both the Master and Slave cards are foreseen to be built in the AMC format which is standard for MicroTCA crates and the XFEL timing group. Depending on the simplicity of the Slave, such board form factors may be over-engineering and far simpler standards will be considered. It may also make sense to have the Slave on the detector to reduce the number of long cables from the C&C crate. More

technical details, explanations of the various signals indicated in Figure 2, and the overall functionality of the C&C system are given in the next section.

Functionality of system

The requirements and functionality of the C&C system are given below. These requirements were the result of a two-day meeting in November 2008 in DESY with the WP76 manager, XFEL timing group and train builder group.

1) To receive, process and store timing signals from the timing receiver (TR) housed in the same crate. The timing signals are:
   - 5 MHz bunch CLOCK (for 200 ns bunch spacing);
   - Bunch train TRIGGER, a single pulse sent by the TR to the C&C Master ~15 ms before the start of each bunch train;
   - Event Number = TRAIN ID, i.e. a unique number/identifier for the train;
   - BUNCH PATTERN or Bunch PATTERN ID, i.e. a unique identifier for the various bunch patterns which may be chosen by the user.
2) To receive BUNCH VETO, a hardware-generated pulse to indicate that the current bunch is to be ignored by the detector.
3) To receive STATUS / ERROR (and possibly BUSY) from each front-end electronics (FEE) board.
4) To distribute three fast lines to each FEE:
   - 100 MHz un-interrupted clock, phase-locked to 5 MHz bunch CLOCK;
   - START pulse, followed by TRAIN ID, followed by PATTERN ID, followed by STOP signal;
   - BUNCH VETO signal.
5) To process any BUSY information from the crate controller to stop the following START pulse.
6) To generate all timing signals in stand-alone mode without the TR.
7) To synchronise to other light sources' timing systems, i.e. to accept external CLOCK and possibly TRIGGER at different frequencies.
8) To provide diagnostic and visual indication of CLOCK, TRIGGER, etc. performance and presence or absence of any FEE.

Programme of work

The programme of work, summarised in the GANTT chart, is split into two phases: the first phase is the major development work, producing a prototype system, followed by a second phase of system production and integration. More details of each phase are as follows:

Phase 1:

- Initially a development board will be purchased and firmware written to allow the detectors to use this so that the front-end can be interfaced to the C&C system.

This will provide the detectors with a simple trigger and decouples firmware and hardware development at an early stage to allow both to proceed in parallel. Firmware will be continually developed throughout the project.

- During this time, a major design effort will plan the Master and Slave C&C interface boards leading to a prototype system. This prototype will have a large fraction of the functionality of the final system so that prototype detectors, expected towards the end of 2010, will be able to use it. The boards will be manufactured with sufficient numbers for each detector, lab and spares.
- After manufacture, the boards will be tested and integrated with the prototype detectors and into test stands in the respective labs.

Phase 2:

- The Master and Slave boards will be re-designed incorporating any problems found during testing and integration with the detectors and possibly making denser. The final Master and Slave boards will then be put into production with sufficient numbers for each detector and appropriate numbers of spares.
- As in Phase 1, firmware development will continue for the whole period.
- Finally lab tests and integration with the detectors will be done.

Resources requested

Phase 1: Clock and control prototype system

	Task	FTE	Cost (k€)
Staff effort	Project management	0.2	
	Design	1.0	
	PCB layout, basic tests and management	0.9	
	Test	0.4	
	Firmware	1.0	
	MicroTCA integration	0.5	
	Integration with prototype detectors	0.5	
	Staff total	**4.5**	
Equipment	MicroTCA system		10
	Development board		1
	Prototype Master board (10 off)		25
	Prototype Slave board (10 off)		5
	Cables and connectors		2
	Equipment total		**43**

Phase 2: Final clock and control system

	Task	FTE	Cost (k€)
Staff effort	Project management	0.2	
	Design	0.5	
	PCB layout basic tests and management	0.5	
	Test	0.4	
	Firmware	0.7	
	System integration	0.8	
	Staff total	**3.1**	
Equipment	Final Master board (10 off)		25
	Final Slave board (50 off)		25
	Equipment total		**50**

Notes

- The effort for PCB layout basic tests and management will come from STFC Technology division: 1.3 FTE for the engineering effort and 0.1 FTE for management.
- All other effort will be from UCL, a total of 6.2 FTE, of which 0.4 FTE is for project management and the rest for engineering and project effort.
- The prototype boards in Phase 1 should have most of the functionality of the final system. They will therefore be made available to the various labs and detectors for integration and test purposes.
- The final system assumes providing a Master clock and control card plus spares to each of the three detectors. The number of Slaves services each of the three detectors assuming 64 front-ends, equivalent to a 4 Megapixel detector, with spares included.
- No travel expenses are assumed as per the XFEL rules for in kind contributions(?)

Project schedule, milestones and deliverables

Project schedule

GANTT chart (Clock and control system for 2D Megapixel detectors)

	Task name	Start date	End date	2009				2010				2011				2012				2013	
				Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2
1	Phase 1	2009-01-01	2010-12-31																		
2	Trigger dev board	2009-01-01	2009-09-30																		
3	Firmware	2009-01-01	2010-12-30																		
4	Design	2009-01-01	2009-09-30																		
5	PCB layout	2009-10-01	2010-03-31																		
6	Manufacture	2010-04-01	2010-04-30																		
7	Test	2010-04-30	2010-08-16																		
8	Detector integration	2010-08-16	2010-12-31																		
9	Phase 2	2011-01-01	2013-07-01																		
10	Firmware	2011-01-01	2013-07-01																		
11	Design	2011-01-01	2011-06-30																		
12	PCB layout	2011-07-01	2011-12-30																		
13	Manufacture	2012-01-01	2012-03-30																		
14	Test	2012-03-31	2012-10-01																		
15	Integration with detectors	2012-10-01	2013-07-01																		

Figure 3: Overview of schedule for clock and control system

Milestones

- Development board with trigger (Oct 2009)
- Clock and control system design review (Oct 2009)
- Prototype clock and control Master and Slave boards at UCL (May 2010)
- Clock and control system technical review (July 2011)
- Production clock and control systems at UCL (April 2012)

Deliverables

- *Phase 1*: Report on design and functionality of clock and control system (Aug 2010)
- *Phase 1*: Prototype clock and control system used by prototype detectors (Dec 2010)
- *Phase 2*: Full clock and control system delivered to 2D Megapixel detector (Jun 2013)

Competences of applicants

The UCL high energy physics group has a wealth of experience in delivering clock and control (and data acquisition) systems for particle physics detectors either a single instrument or to control several different types of detector. We have experience providing clock and control systems for the ZEUS experiment at HERA, the ATLAS experiment at the LHC and the CALICE R&D programme. The latter in particular has a similar complexity to the proposal here as the system consists of several detectors which have to be interfaced to different accelerator structures depending on the test-beam to be used.

The management, design, testing and integration will be carried out by UCL. The PCB layout will be done by the STFC Technology division who are responsible for the train builder project and have specialist groups for PCB development.

The project will be managed by Dr Matthew Wing from UCL with a start date of 1st January 2009 to run until June 2013, or as dictated by XFEL requirements.

Related projects and collaboration

Close collaboration between UCL and the related projects has already started. The STFC Technology group is planning to develop the train builder system and will also contribute to this proposal. Discussions have also started with the DESY and Stockholm groups responsible for the XFEL timing system. All of this has been done in consultation with the WP76 manager.