LPD FEE status

Current Status. No change from Slides from Nov meeting.
Time schedule.

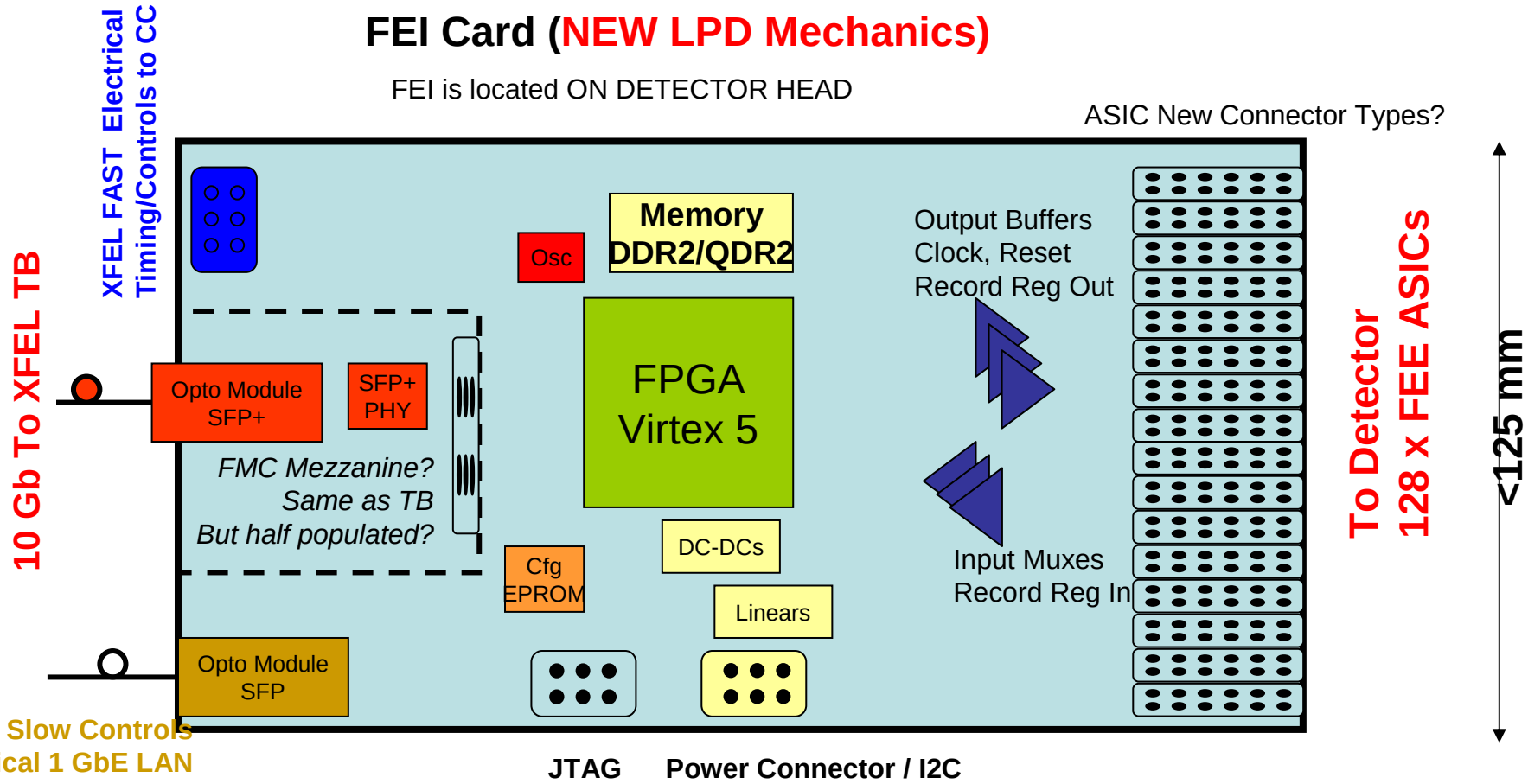
Consequences Nov meeting. LPD satisfied with conclusions.

Open Issues. Lots internal to LPD!
Connectors to C&C.
Common TCA Blade and LAN interface. Fast Eth 100 Mbps Elec

John Coughlan.

FEI Card (NEW LPD Mechanics)

FEI is located ON DETECTOR HEAD



Comments: Attempt to show the basic elements and interfaces Drawing is NOT to scale

FPGA larger Virtex 5 FX70T / LX110T package FF1136
No more merging between cards.
RAM/FIFO to smooth data flow from asics to link

Readout – Opto SFP+ 10 Gbps Optical link direct to Train builder.
Fast controls link to CC card
LAN 1 GbE for Slow Controls interfaced to mTCA processor card

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XFEL DAQ Meeting DESY Dec 4 2008

Spare Slides

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Train Builder status

Original plan from Cosener's House meeting

Draft proposal document (for XFEL In Kind Contribution) sent to Chris.

Schedule
Phase 1 Demonstrator on AMC 2009/10
Phase 2 Full Systems (½ MPix on ATCA baseline tbd) 2011/13

Estimate of resources and costs for both phases.

STFC ready to start.
Funding committees go more slowly. Proposals with XFEL backing will help to push along.

Preparations See slide.

Consequences Nov meeting. TB only has LAN interface. No C&C links.

Open Issues. Lots!
Phase 1 AMC MMU Microcontroller? Use DESY for s/w support.
Get DESY AMC to start TCA s/w?

"RTM" too early to make decision on phase 2 implementation

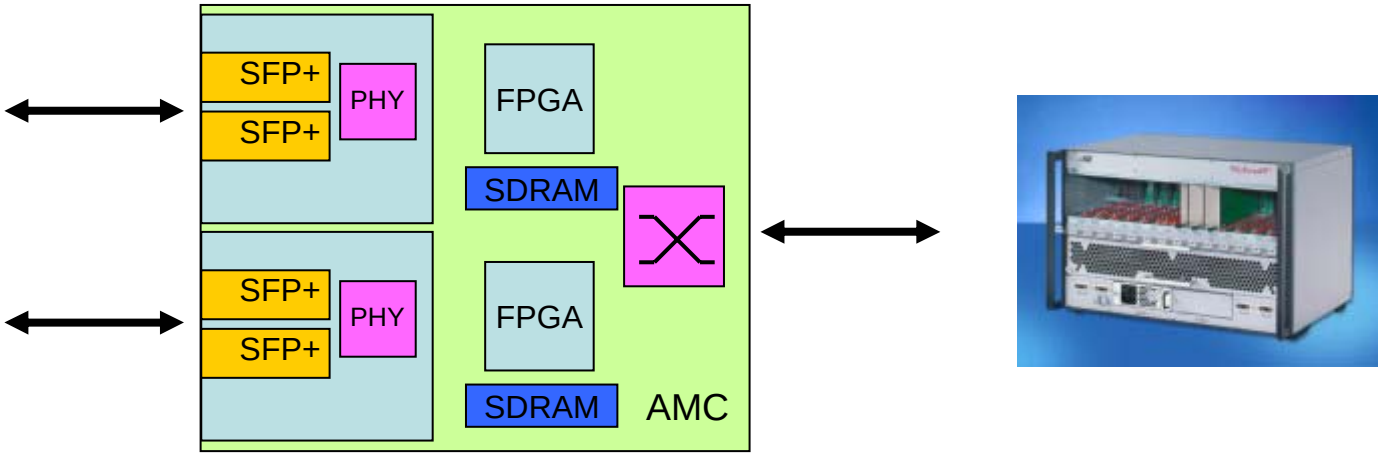
But 10 GbE TCP (UDP) development is needed.

"Shared" FPGA designs. See slide

Train Builder Development Plan Proposal

1. Start with FPGA and Crosspoint Switch **development boards**.
   Investigate Memory interfaces.
   Serial Protocols. Aurora protocol switching.
   Get experience with driving Crosspoint switches.

2. **Demonstrator AMC card with CrossPoint**. Prototype system using MicroTCA crate.
10 Gb designs from DESY. Consider Optical Mezzanine on AMC?



3. Full **ATCA board Prototypes**.

4. Full **ATCA board Production**

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Train Builder preparations

Obtained UK quotes on same mTCA kit as per DESY (all except disk)

Joined PICMG. Got full TCA specs. Reading…
And VITA57 FMC mezzanine spec.

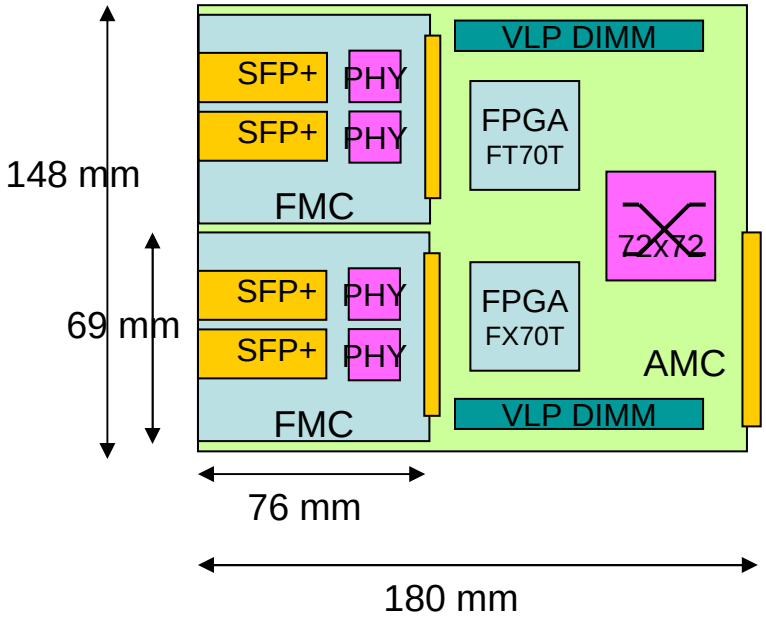
FPGA Dev boards Ordered ML510, ML507.

Phase 1 AMC Demonstrator
Not much done yet…engineer only starting to have time on this…
Played with some alternatives to ppt layout (but ended up back to same)
Evaluated candidate components and packages
FPGAs (V5 FX70T FF1136)
Crosspoint (Mindspeed M21141)
Memory? SORDIMMs vs DRAMs important decisions
Go ahead with FMC VITA57 mezzanine (for Opto TRx modules.)
Started to look at FPGA memory interface options.

Next steps
Challenging pcb layout. Paper rats nest with pin outs for FPGA, Crosspoint, AMC, FMC conns.
Start with critical routing of fast serial links. (using all 16 rocket i/o on each FPGA, and Crosspoint)
And then memory i/o
Get PCB design office involved. Put target components in libraries.
Prototype FPGA design to guide pcb layout. (Aurora channel to memory controller)
Open issue. MMU Microcontroller want to use same as DESY for s/w support. Will it be AVR (or ARM based?)

Obtain a DESY AMC to get started with s/w?

40 % Scaling



Side 1?
MMU controller
Clock sources
JTAG conns, buffers
DC-DC
Linear
Test points, leds etc

Side 2?
Platform Flash
EEPROM
SRAMs (s/w)?

Options??
V5 TXT
RXAUI
Dual SFP+
SDRAMs vs DIMMs
Xilinx V6

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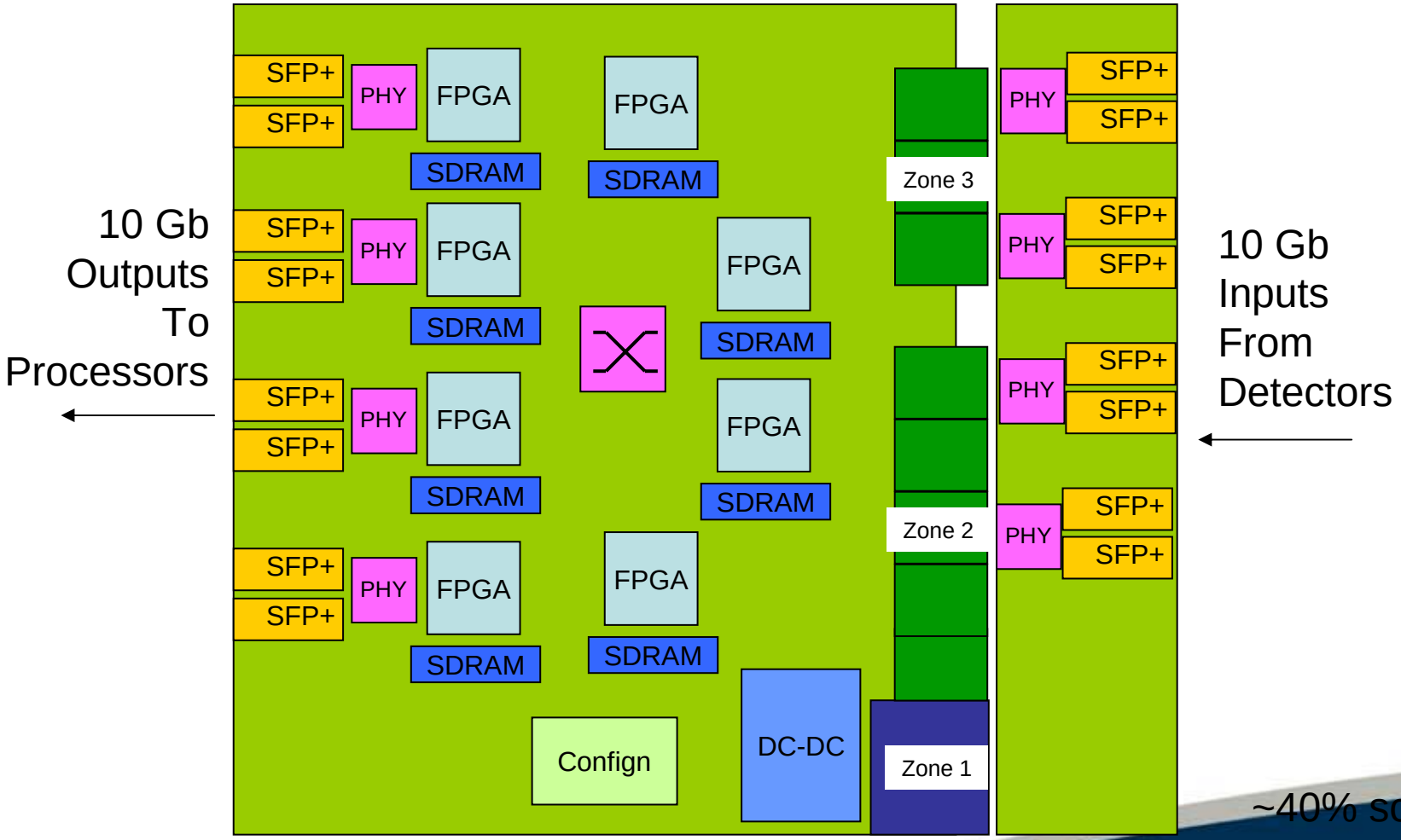
½ MPix Train Builder baseline. Matched to 2D 8 x FEI outputs

“Simplest” Train Builder Implementation. All FPGA / No Mezzanines.



~40% scaling

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“Shared” FPGA Designs

I’ve not thought deeply about this, but….

Design flow at RAL

Train Builder baseline targeting Xilinx Virtex 5 (later to Virtex 6?)

Windows based tools
Xilinx ISE 10.1 top level design
Xilinx EDK embedded blocks (imported netlists into ISE)
Standalone Lib, C language
Precision Synthesis
(*Mentor HDL Designer wrapper*)

Plan Ahead (floor planning)
Subversion code management

Interfacing Modules:
Suggest using Xilinx **Local Link** protocol for interfacing from Serial Links to TB cores.
Simple frame based protocol.
Mainstream for interfacing Xilinx IP cores (and 3rd party?)

Other issues :
Understand module resource usage. Need more headroom. Floor planning?
Common tools and synchronising (major) tool updates
Script driven flows to ensure common parameters and options eg P&R
Design repositories. Bitfiles, Netlists, Source files. Servers. Bookkeeping
Licensing issues if commercial IP cores, OS’es, Intellectual Property issues