XFEL 2D Pixel Clock and Control System

Train Builder Meeting, DESY

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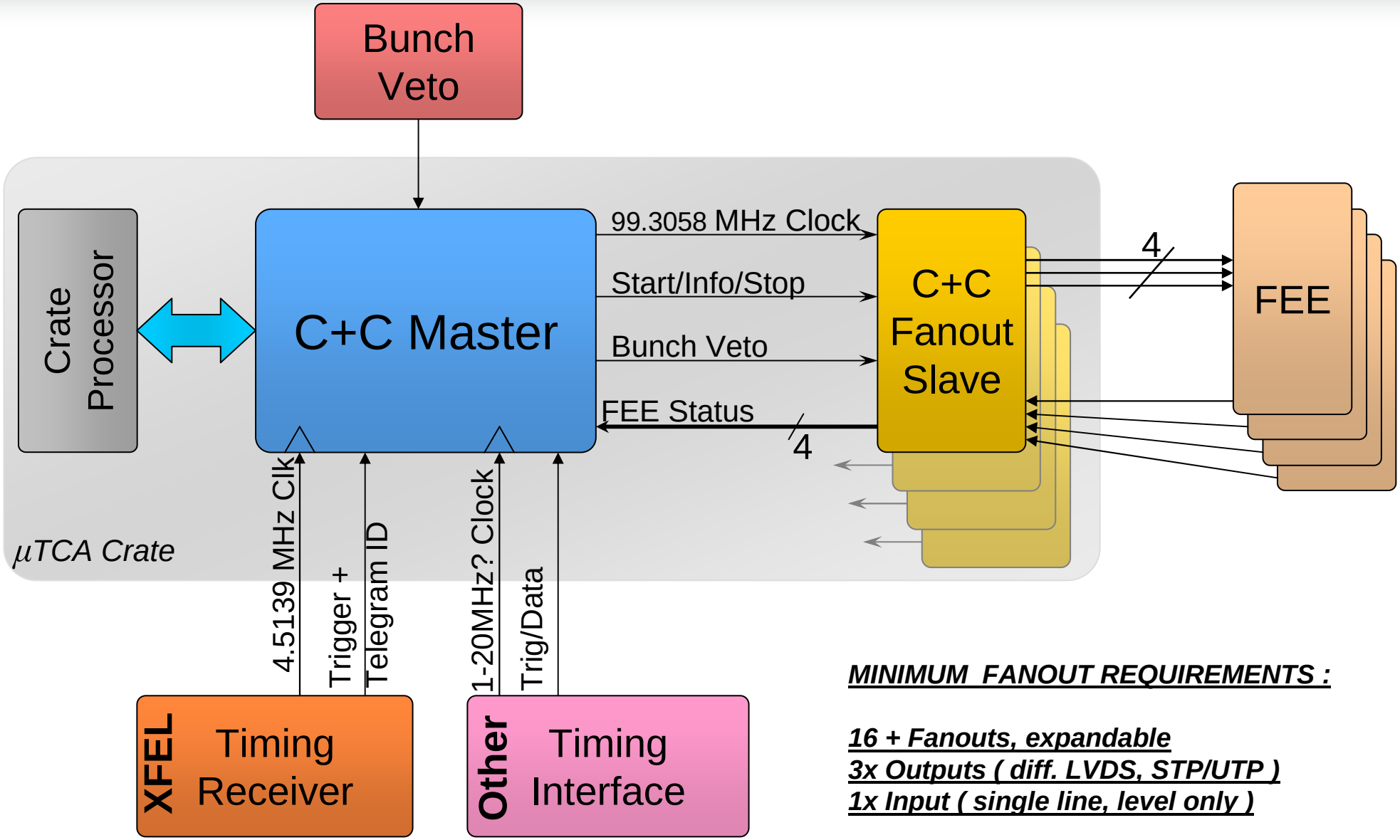
Overview



MINIMUM FANOUT REQUIREMENTS :

16 + Fanouts, expandable
3x Outputs (diff. LVDS, STP/UTP)
1x Input (single line, level only)

Clock

UCL

1) ~99 MHz CLOCK :

Integer multiple of the incoming 4.513889 MHz clock

from T.R. : 21x = 94.791669 MHz

22x = 99.305558 MHz

Fast Commands -1-

Three Fast Command Lines :

- Fanned out to all FEEs via C&C Fan-outs
- Same cable lengths
- Individual adjustable delays ???

We could propose to use the "ODELAY" functionality available on Virtex-5 (and Spartan-6) FPGAs, which allows for 0-63 bits of ~75ps delay on each I/O pin (when using 200MHz clock)

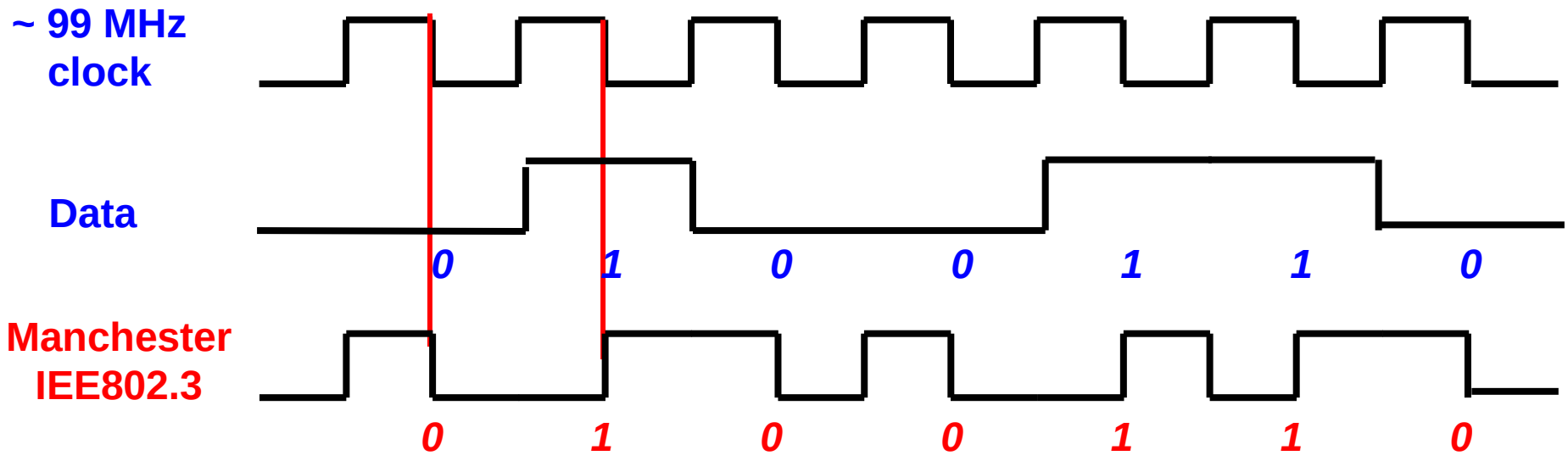
As we will have FPGA on each fan-out card, we could propose to use this delay facility on the 3x fast command lines sent out to all FEEs ???

AC Coupling : Manchester Coding

AC coupling on FEEs : ANALOG ADuM3441 : *skew too large*

=> use simple capacitive AC coupling

=> requires Manchester coding on both START / STOP and VETO command lines

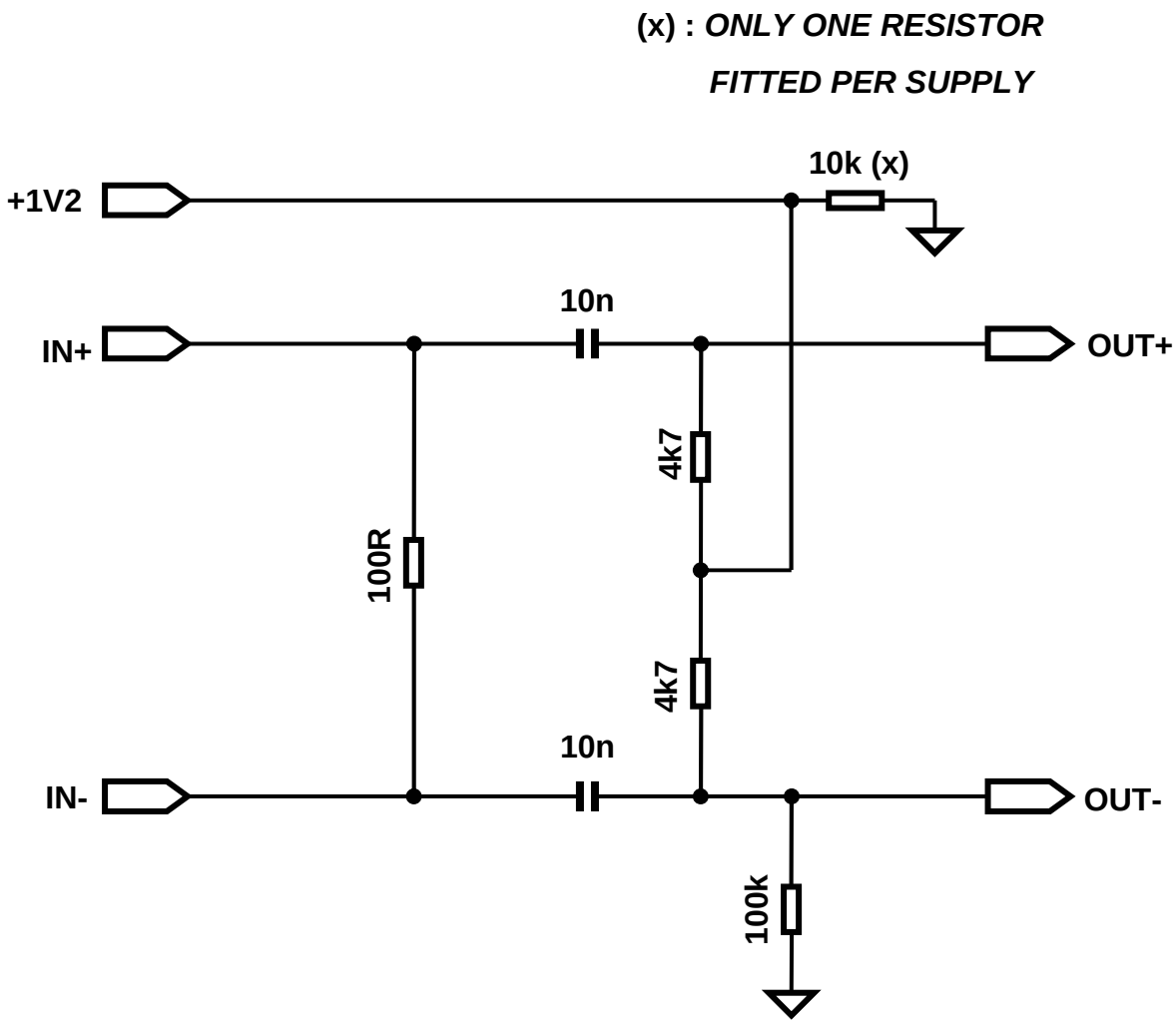


Data = Clock XOR Manchester Code

Simple AC – coupling

Simple capacitive AC-coupling

- Requires basic Manchester coding on each of the two fast command lines



Fast Commands -2-

2A) START-TRAIN / TRAIN-ID / BUNCH-STRUCTURE-ID / STOP

Synchronised to the ~99 MHz clock

Fixed phase relationship to the ~4.5 MHz clock

a) START : 1100 = 4 bits

Start pulse to start about ~ 15 msec (programmable in 200 nsec steps) before the train arrives

b) TRAIN-ID : = 32 bits

The train number is a unique number. From the DAQ point of view it should never repeat and should continuously count up

=> Generated on C&C (counter)

Fast Commands -3-

c) BUNCH-STRUCTURE-ID : = 8 bits MAX

probably only ~16 patterns for any given run/day

d) CheckSum of b) and c) = 8 bits MAX

- Assume maximum 3000 bunches per train

e) STOP : 1010 = 4 bits

Stop pulse at the END OF THE TRAIN

2B) RESET uC : 1001 = 4 bits

to reset the FE micro-controller via the FE FPGA

2C) Reserved : 1111 = 4 bits

Fast Commands -4-

UCL

3A) VETO BUNCH :

Synchronised to the ~99 MHz clock

Adjustable phase relationship to the ~4.5 MHz clock :

(up-to 10 clocks for LPD)

a) VETO FOLLOWS command : 110 = 3 bits

b) BUNCH-ID : = 12 bits

c) -reserved- : = 4 bits

3B) NO VETO

a) NO-VETO-FOLLOWS command : 101 = 3 bits

b) BUNCH-ID (???) : = 12 bits

c) -reserved- : = 4 bits

FEEs Status Feedback

- ***STATUS FEEDBACK from all FEEs :***

  Each FEE plugged-in & powered-up

  Status only : OK = ?? MHz clock

  ERROR = high / low / floating...

  Can change later to carry more information if required.

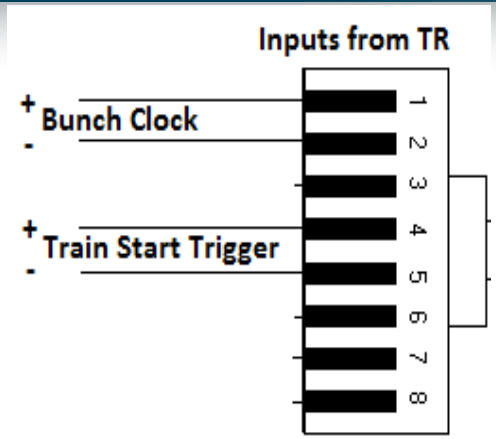
  (BUT this would need using Manchester coding as well)

Master Input Sockets A, B (& D, E)

UCL

Single RJ45 socket A

- Bunch Clock ~4.5 MHz
- Train Start Pulse

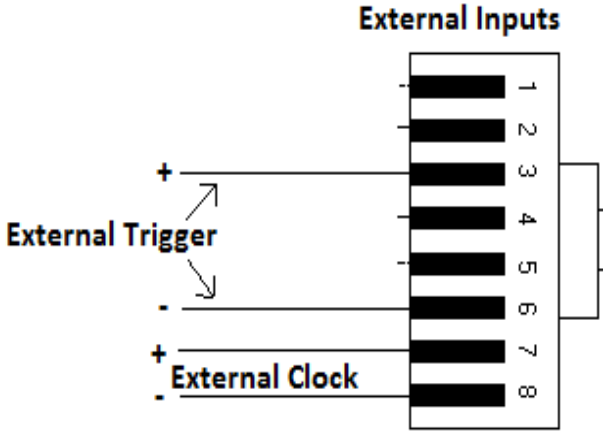


Single RJ45 socket B

-External Clock

(750 kHz – 6 MHz)

- External Trigger



Single Lemo 00 socket D

- External Clock (LVTTL / NIM)

(750 kHz – 6 MHz)

Single Lemo 00 socket E

- External Trigger (LVTTL / NIM)

Output Sockets C1, C2….C8

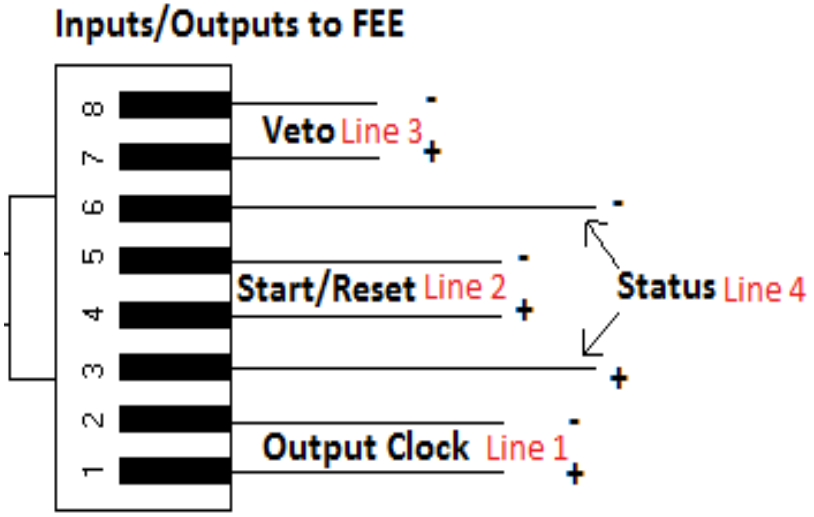
Block of 8x RJ45 connectors
(Tyco 1888507-3 : 2x4 bloc)

either :

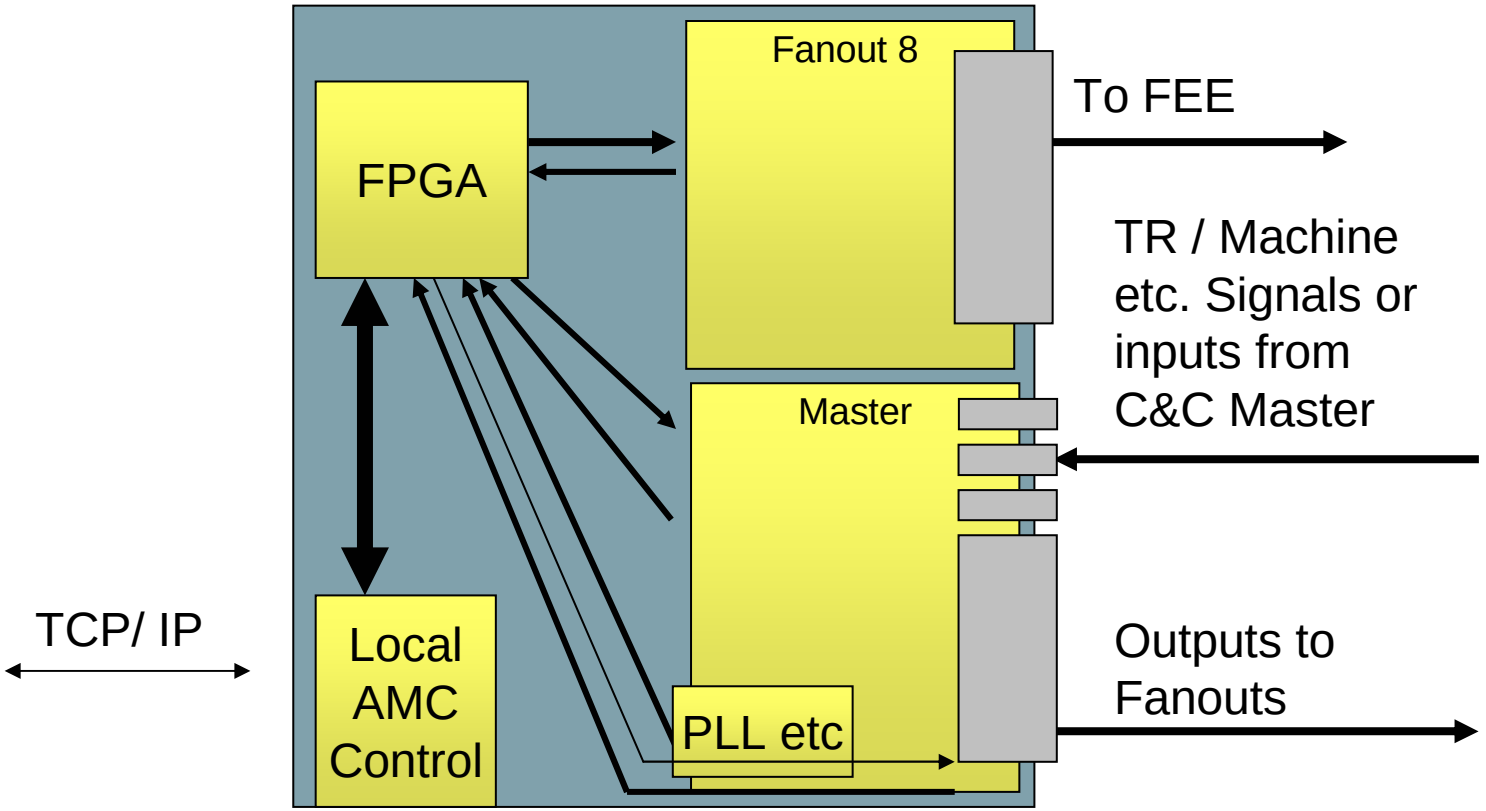
8 outputs to 8x Fan-Out cards

or :

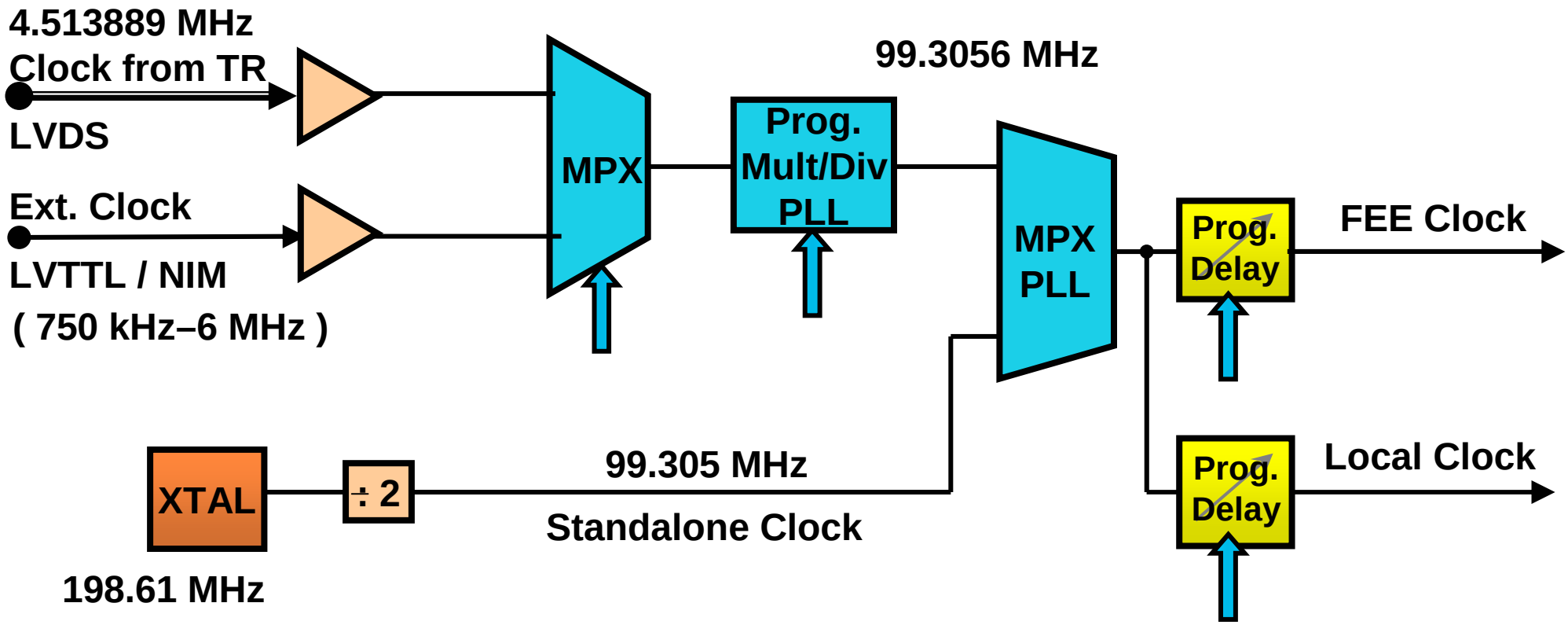
8 outputs from each Fan-Out card to FEEs



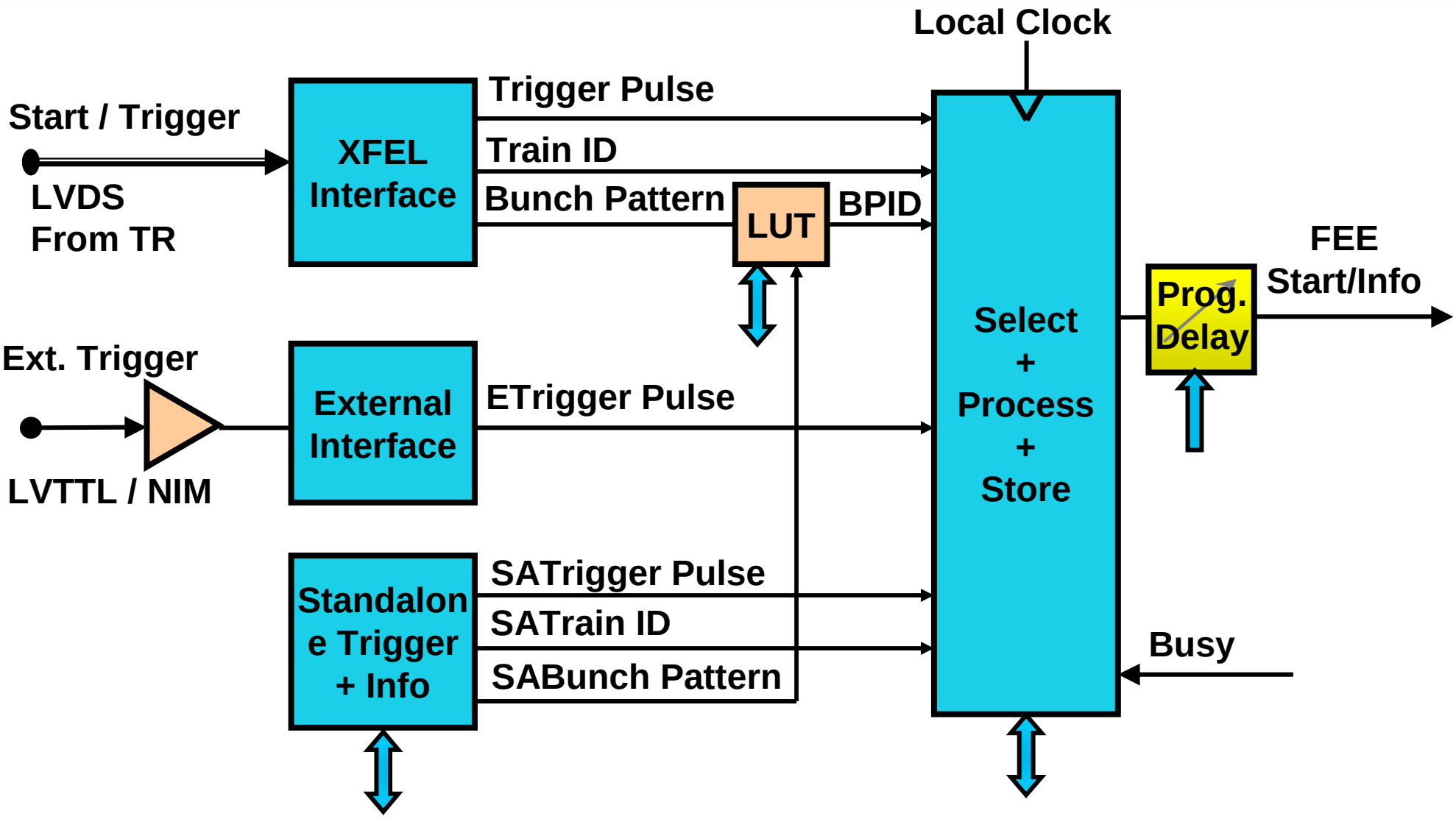
Single integrated prototype card



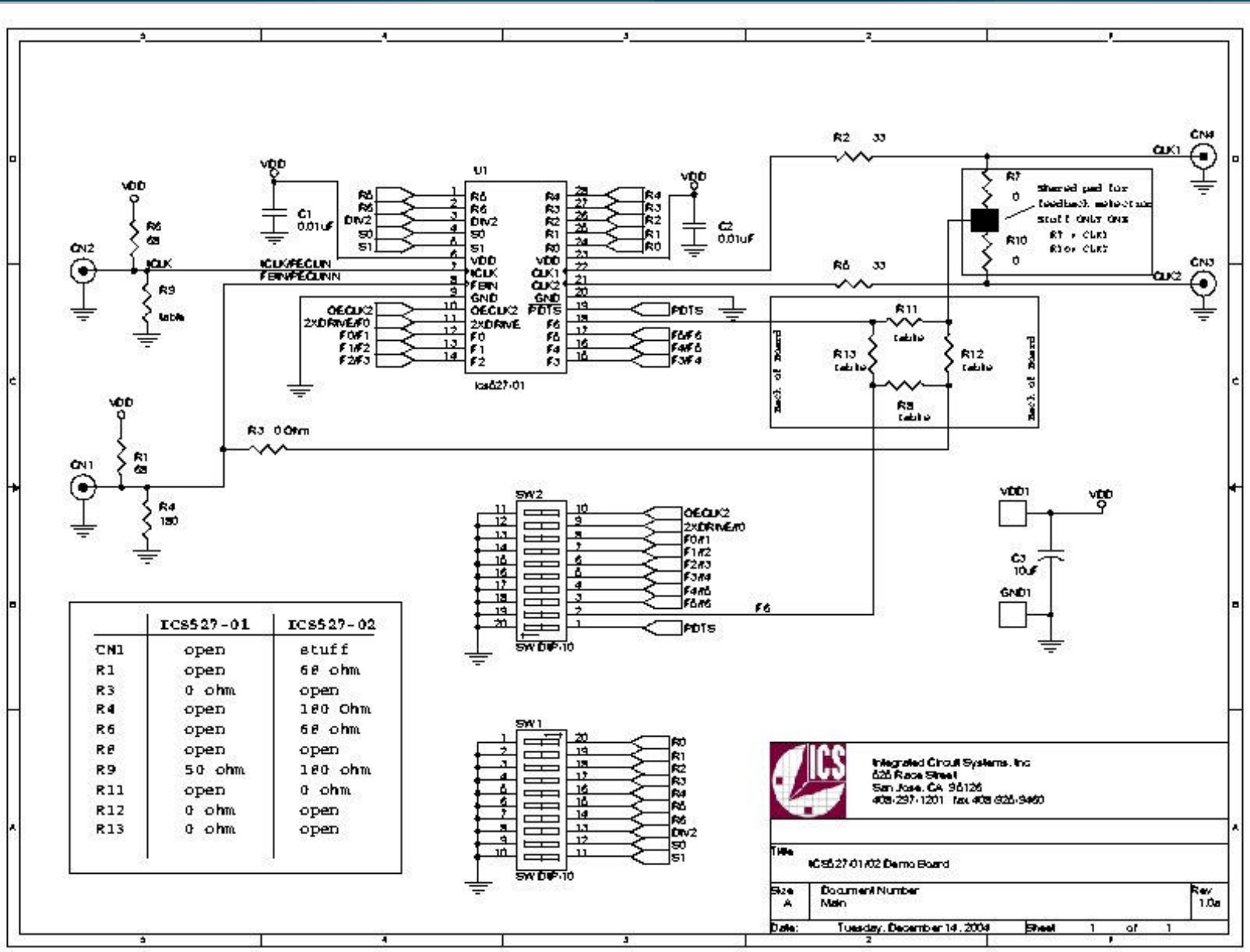
C+C Master Clock



C+C Master Trigger + Info



ICS570-01 PLL Demo Board



	ICS527-01	ICS527-02
CN1	open	stuff
R1	open	68 ohm
R3	0 ohm	open
R4	open	180 Ohm
R6	open	68 ohm
R8	open	open
R9	50 ohm	180 ohm
R11	open	0 ohm
R12	0 ohm	open
R13	0 ohm	open

End…..