AGIPD FEE status

- Reminder to concept, no real new items
- Argument for system clock n*clk_{XFEL}

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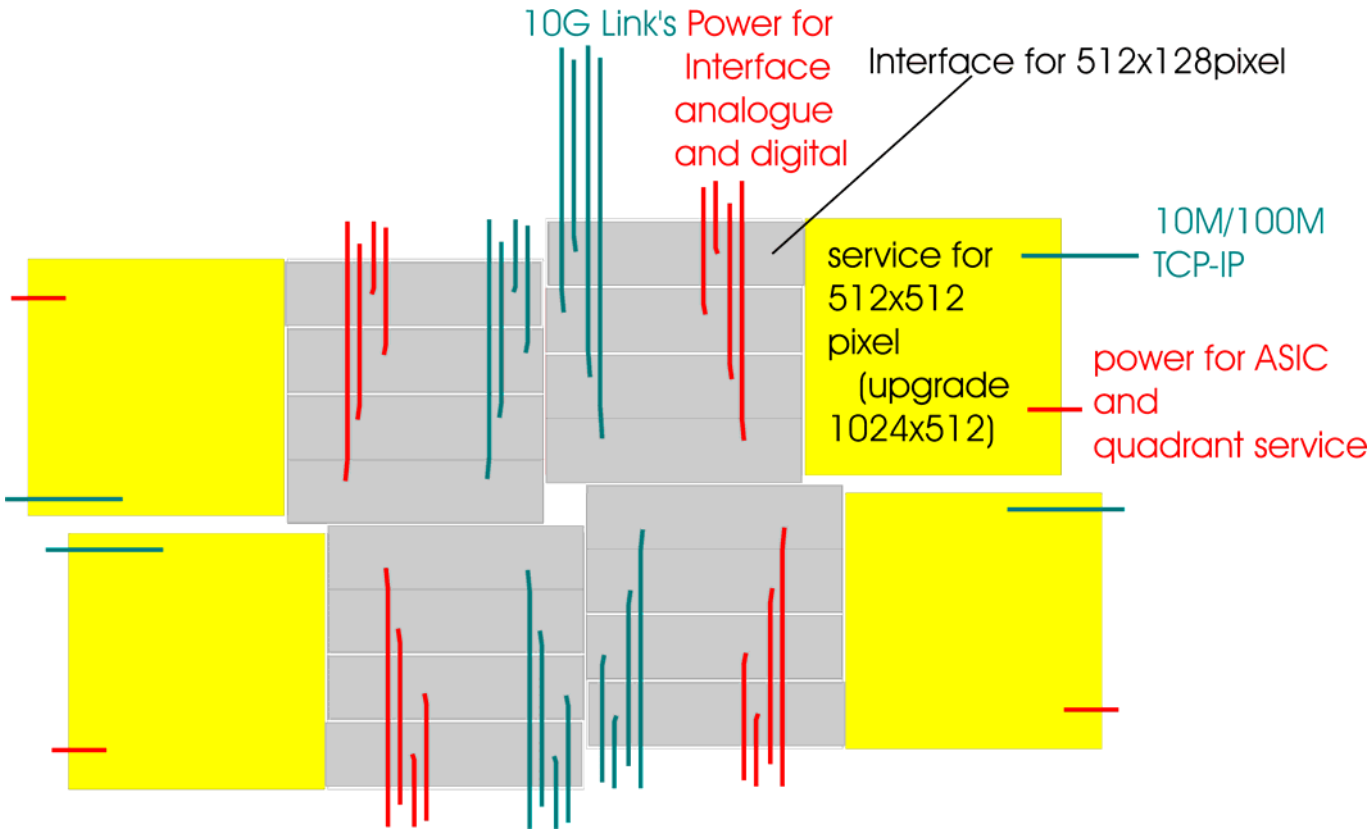
Reminder of concept: 4 quadrants



Arguments for system clock

Integer multiple of XFEL clk: $n*Clk_{XFEL}$

not option of PLL: $n/m\ CLK_{XFEL}$

Reason no jitter, different phase steps

- integrating pixel charge $Q=\int(t,t+\Delta t)Idt$
- defined storage time until digitization
- regerating the ADC time stable to bunch

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Wish

ADC handles only up to 50MS/s

multiple, serial ADC's : AD9252

clk near 100MHz and known factor

may be less than 100MHz (if 50MS/s)

to get back the ADC Clk, e.g. even factor

- System clock a multiple of XFEL-clk

n/m generated discrete steps of 2π k/m

harder to compensate for.

configurable factor n, to optimize storage …

To pay: system clock not exact 100MHz.