

## **FEE, TB and CC FPGA Meeting**

Wednesday, 18<sup>th</sup> January 2012  
Patrick Gessler

### **Present**

J. Coughlan, B. Fernandes, P. Gessler, E. Motuk, M. Postranecky, I. Sheviakov, P. Vetrov, M. Zimmer

### **Next Meeting**

**1<sup>st</sup> February 2012, 11:00 CET**

### **Open Points**

- **Collect final change request for DAMC2**
- **Collect feedback for VETO document**

### **Minutes**

#### **1. Update on Timing CDR development**

- Just received updated version of the document
- Will be distributed after the meeting
- Please check if reported issues now changed if needed

#### **2. Redesign of the DAMC2 board**

- The CC team requested a way to send the 99MHz from the RTM to other (slave) boards via TCLKA or TCLKB
- As it turned out in discussions with Manfred Zimmer's team, this is not easy to implement
- Therefore it was asked, if the requirement is still valid
- It was made clear by Martin and Erdem, that it is required to allow synchronization of the 99 MHz between different CC boards in one crate
- A proposal will be developed about how to implement this function in the DAMC2 by CC team and Patrick
- It will be discussed next week with Petr Vetrov and then presented in the DAMC2 redesign meeting next Thursday to be approved by all users of the DAMC2 board

#### **3. Upcoming cable measurements**

- Next week Erdem will come to XFEL to do measurements on possible cable length between the CC RTM and FEEs
- The measurements were already started at UCL based on bit error rate tests
- First results showed, that the maximum reliable length is 10m, but further clock-to-data phase optimizations are done to see, if it can be even improved
- The tests at XFEL will be measurements of clock jitter and data eye diagrams for the CC RTM outputs as well as Timing Receiver outputs

#### **4. Discussion on VETO document**

- The VETO document had been distributed before last meeting
- The comments are currently collected
- By now comments from Markus Kuster, Chris and Matthew had been received

- Erdem said, he currently don't see problems, the new part is to implement the Gigabit receiver in order to receive the information from the VETO unit
- John browsed through the document and the preliminary statement was that there is now problem seen. It will get clearer if the part for the implementation for the LPD is written. He will also look more deeply into the document and will send questions and comments
- Patrick will get in contact with Matthew about the questions sent
- On next meeting will be again time to discuss the VETO document

#### **5. Preparation for slice tests**

- Rob was not present, but John said, that Rob was working on the 10G adaptions and the pattern generator
- There is progress

#### **6. Status updates**

- LDP
  - o Train Builder:
  - o Signal routing completed yesterday
  - o LVDS balancing ongoing
  - o Final review will be done in two weeks
  - o One week later sending out for production
  - o FEMs:
  - o 6 new board passed the boundary scan check
  - o Further 14 boards are available for assembly
- AGIPD
  - o Hardware expected in two to three months
- DSSC
  - o Thomas was not able to join the meeting

#### **7. Upcoming Events**

- 25<sup>th</sup> – 27<sup>th</sup> January 2012 XFEL Users Meeting in Hamburg
  - o Erdem registered and will present the CC poster
  - o Patrick will present a DAQ electronics overview poster plus the TB poster

#### **8. AoB**

- Erdem and John will send the links to the papers to the mailing list

#### **Decisions and actions**

- Preparation for measurements at XFEL (Patrick)
- Erdem will bring cables and CC RTM for measurements (Erdem)
- Measurements of Cable length performance (Erdem, Patrick)
- Preparation and printing of posters (Patrick)

#### **Topics on Hold**

- Redesign/changes on CC RTM could wait till Summer 2012