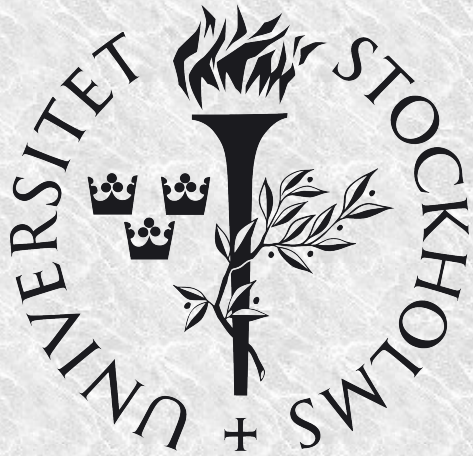
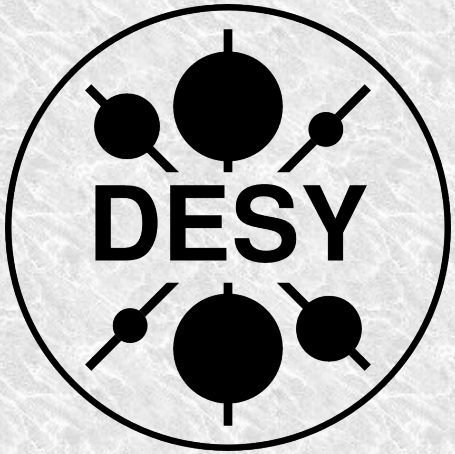
# Experiments timing receiver board description

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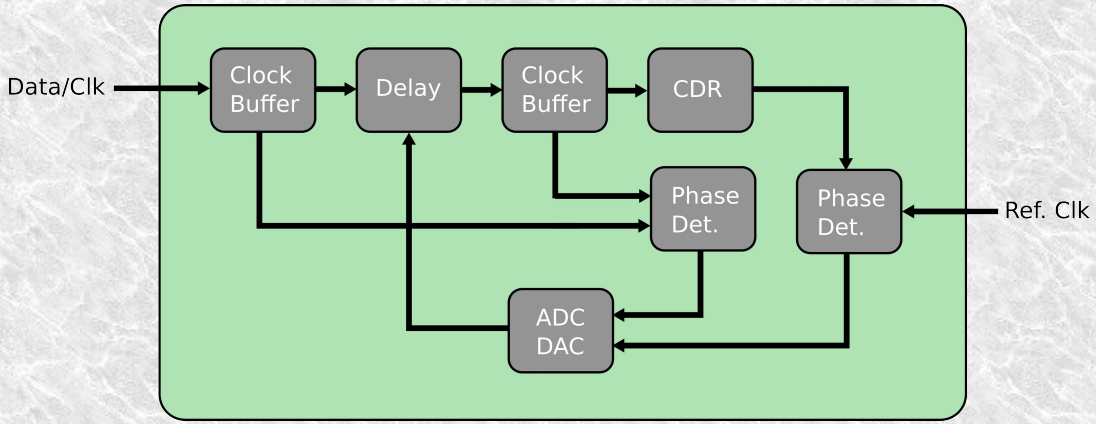
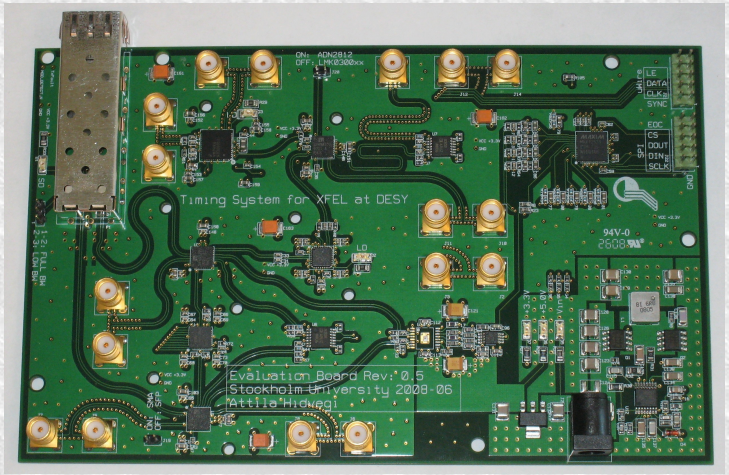
# Overview

- Test Board
  - Features
  - Measurements and results
- Next prototype
  - Features
  - Who is providing what
  - Status and time line

# Test Board - Features

- Contains:
  - clock distribution buffers
  - Delay chip
  - CDR
  - Phase detectors
  - SFP interface
  - ADCs and DACs
  - Monitoring and communication
  - 4-layer FR4 PCB
- Enables:
  - Testing of key functionality and concept
  - Characterization of key components
    - Performance
    - Temperature sensitivity

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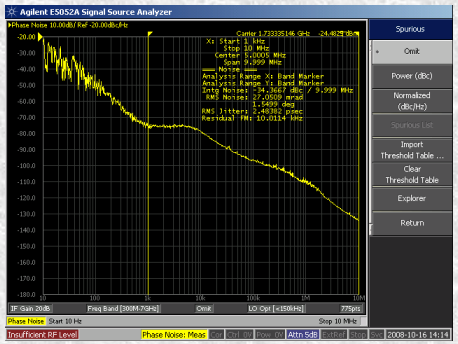
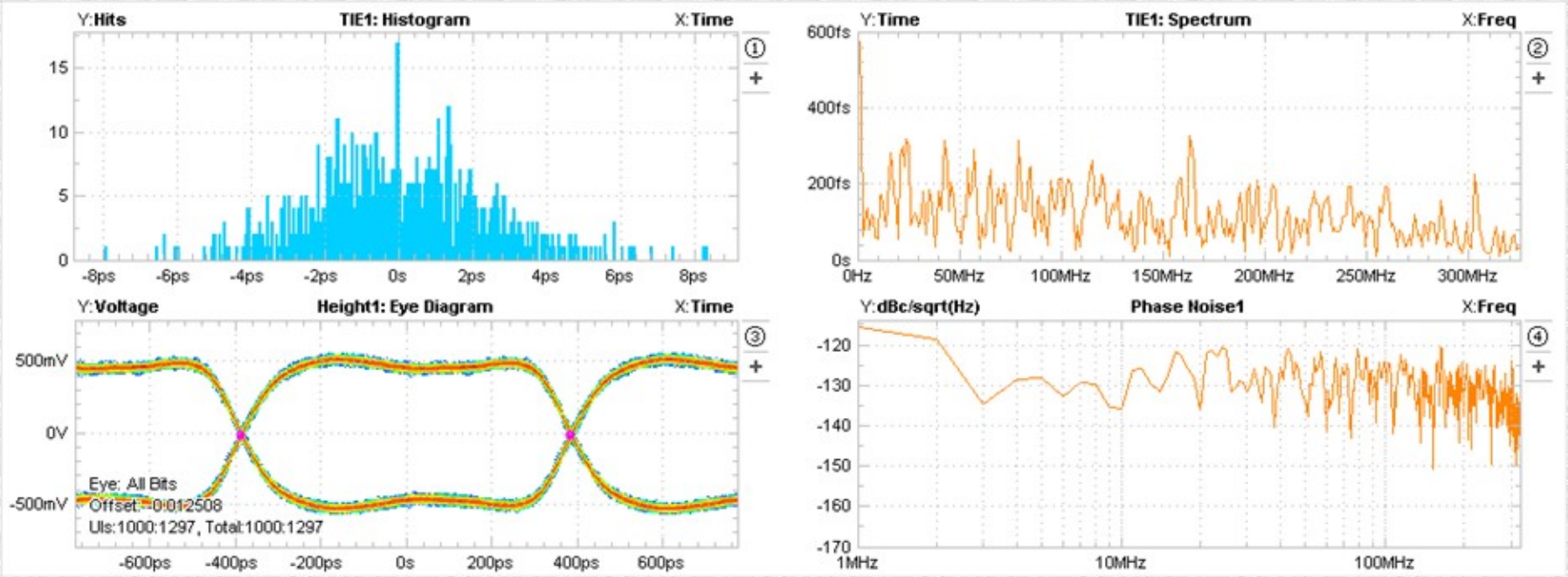
# Test Board – Measurements

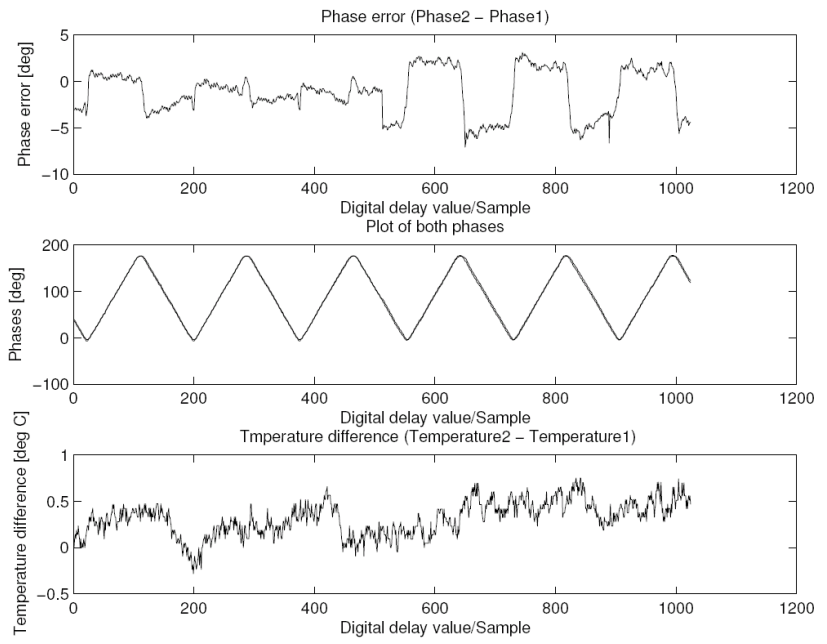


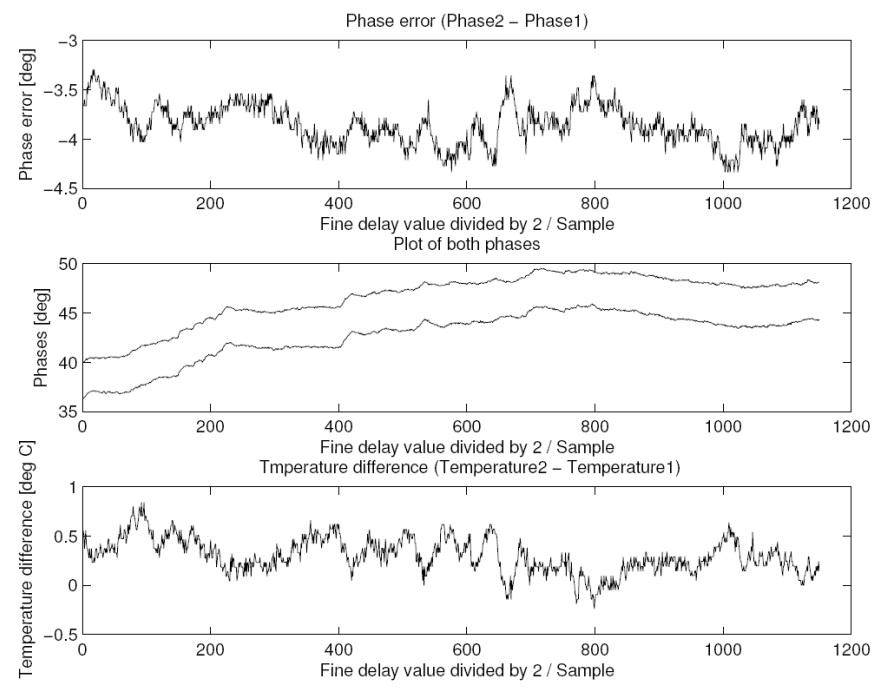

- Jitter measurements made at both DESY and Stockholm
- 2.5 ps RMS jitter, after CDR
- Signal Integrity look good
- Both signal integrity and jitter performance can improve even further with better PCB material



# Test Board - Measurements

- Extensive measurements have been made to characterize basic components
- Temperature dependency have been studied
- More measurements will be made in the future



# Next prototype - Features

- Outputs:
  - Individually adjustable phase and frequency divider on all clock outputs
    - FPGA solution:
      - Unlimited divider
      - Phase resolution: <100 ps
      - Random jitter: <100 ps RMS (*probably significantly exaggerated*)
      - Benefits: many FPGA I/Os are available and simple solution
      - Suitable for less demanding receivers
    - Discrete component solution:
      - Divider: up to 510
      - Phase resolution: <1 ps
      - Random jitter: <5 ps RMS
      - Suitable for demanding receivers
    - Both FPGA and Discrete solution will be tested on first prototype

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# Next prototype - Features

- Outputs:
  - Number of outputs
    - 4 clock and 4 trigger outputs in the front on the first prototype. Probably more on future prototypes.
    - Distribution through the backplane will be available...
  - DC coupled
  - LVPCEL and LVDS

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# Next prototype - Features

- Formfactor:
  - AMC for µTCA and ATCA
  - Other formfactors may be provided in future if there will be enough interest
- Virtex-V FPGA for control, but may be upgraded in future
- Separate microcontroller for MMC
- Radiation tolerance
  - Soft errors in firmware will be detected and corrected (from later firmware versions)

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# Clock, Trigger and Telegram distribution

- On first prototype signals on the frontpanel
  - 4 clocks and 4 trigger
- Clock and trigger distribution through backplane in future
  - In ATCA a custom backplane in Zone-3 would allow almost anything, but may require custom backplanes for different crates.
    - Who would provide that?
  - In some µTCA shelves there are direct connections between AMC cards for custom communications, which could be used for clock and trigger data.
    - Not available in all systems
    - Their number may be too few

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# Who is providing what

- Hardware: Stockholm University
  - AMC boards
- Firmware: DESY/Stockholm University
  - PCIe interface exist at DESY
  - Rest will be developed by Stockholm
- Software: DESY/Stockholm University
  - Linux and Solaris driver exist at DESY, but customizations will have to be made
  - DOOCS server and client application will be provided by DESY

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# Next Prototype – Status and Timeline

- Status
  - Under development
  - Some features still need to be determined
- TimeLine
  - Design ready 2008
    - PCB
    - Firmware and Software development may take longer
    - Only a few boards will be manufactured first for testing
  - Testing from January 2009
    - Timing performance
    - µTCA compatibility
  - May be available for users if needed in 2009 Q1-Q2

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