Large Pixel Detector Timing and Controls

John Coughlan.
XFEL Timing and Controls Meeting DESY Nov 12/13 2008

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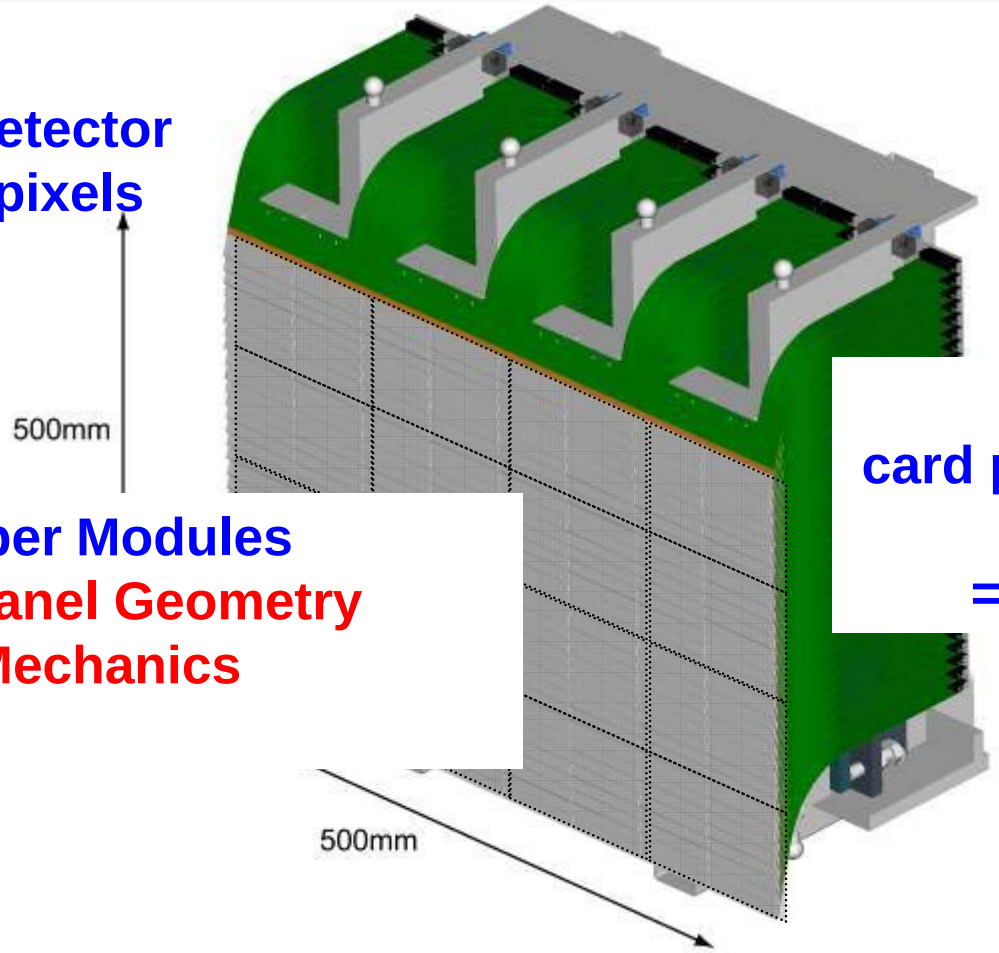
Phase 1 Prototype Detector
1M Pixel

Hybrid Pixel Detector
0.5 x 0.5 mm pixels



4 x 4 Super Modules
NEW Flat Panel Geometry
NEW Mechanics

1 FEI
card per Super Module
on rear
= 16 FEI cards

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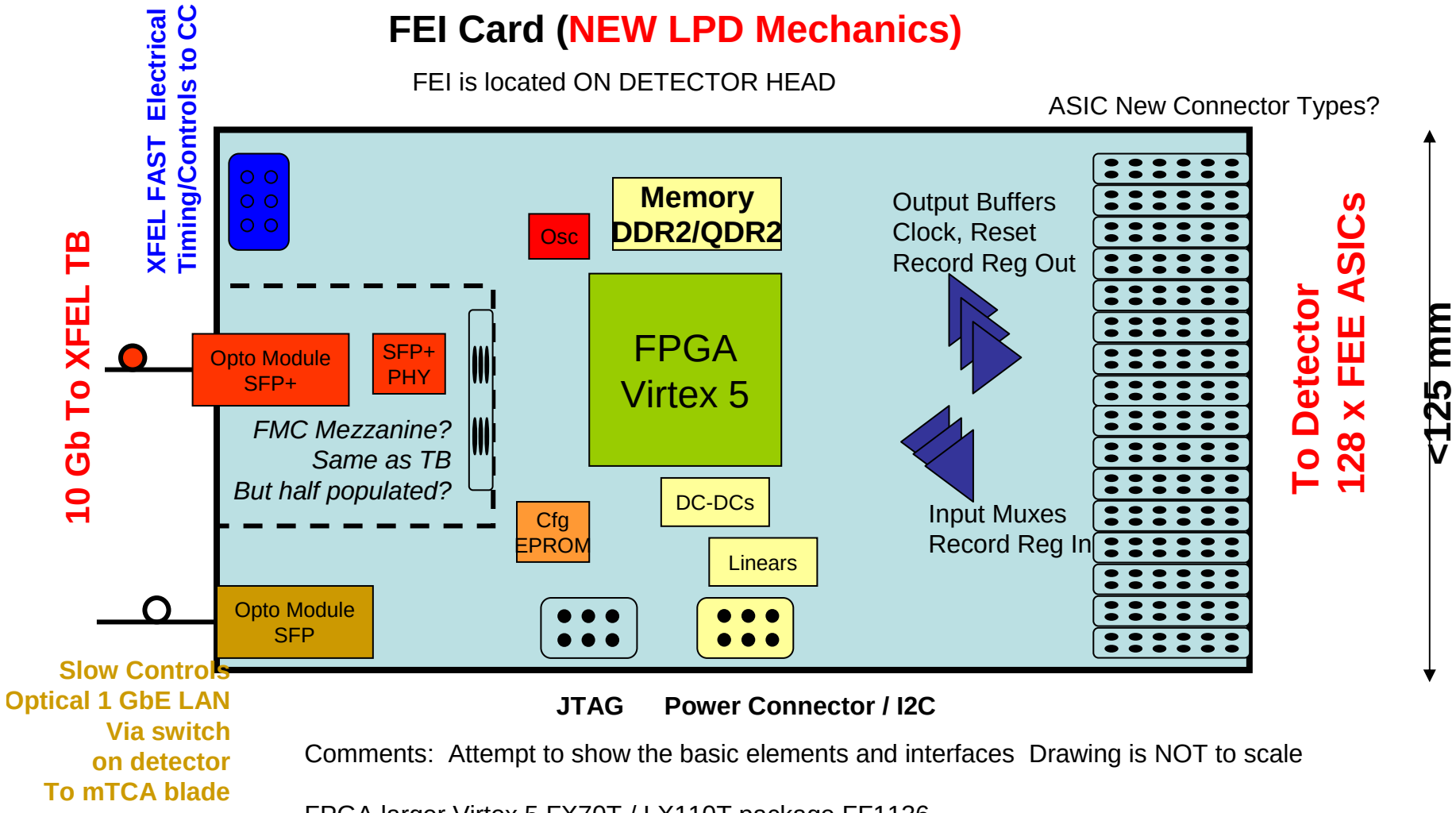
FEI Card (NEW LPD Mechanics)

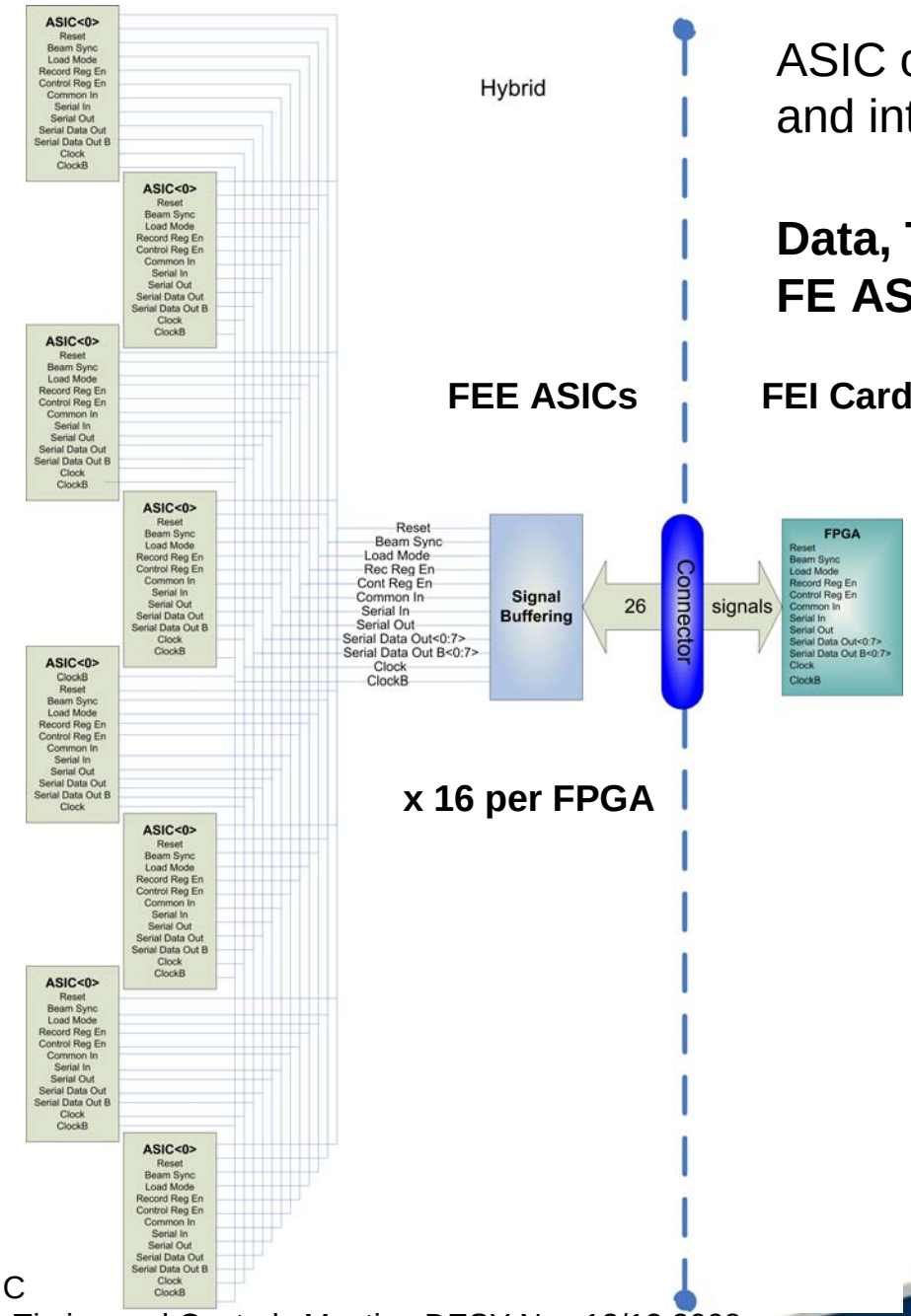
FEI is located ON DETECTOR HEAD



Comments: Attempt to show the basic elements and interfaces Drawing is NOT to scale

FPGA larger Virtex 5 FX70T / LX110T package FF1136
No more merging between cards.
RAM/FIFO to smooth data flow from asics to link

Readout – Opto SFP+ 10 Gbps Optical link direct to Train builder.
Fast controls link to CC card
LAN 1 GbE for Slow Controls interfaced to mTCA processor card



ASIC operation modes and interfaces defined

Data, Timing & Control Signals between FE ASICs and FEI card FPGA

Loading ASIC Parameters

Define Run as a new set of experimental conditions.

Before Run. SLOW Load each ASICs gains, biases +...

During Run before each Train. FAST load Bunch Select pattern* same to all ASICs. (But No trigger/veto during pulse train foreseen in ASIC)

*** one from a predefined pulse pattern set**
ASIC design max 3,000 pulses per Train

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Operating FE ASIC

Define Run as a new set of experimental conditions.
"Prepare" Run. SLOW Information Loaded per ASICs gains, biases…

During Run before each Train. **FAST** load Bunch Select info common to all ASICs. No bunch trigger/veto in ASIC design (yet).

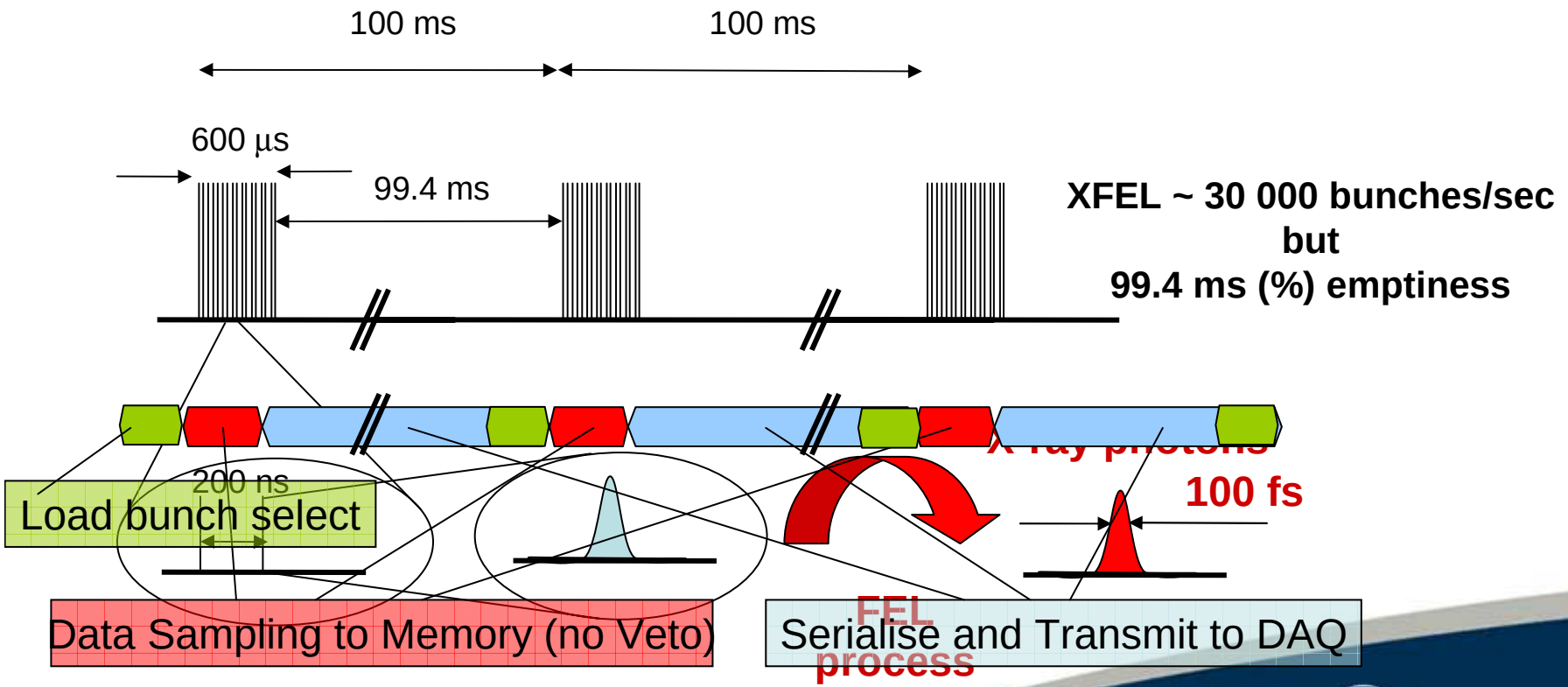
FAST events/signals to FEE ASICs

- Clock 100 MHz
- Start Train. Timing wrt bunches fixed Resolution < 0.7 nsec? Is this fixed for all machine conditions?
- Bunch Fill pattern info (could come together with Start Train event?) (> 10? msec before bunch train arrives).

- Adjust phase clock
- Adjust delay Start Train

XFEL Beam Structure

Electron bunch trains; up to 3000 bunches in 600 μsec, repeated 10 times per second.
Producing 100 fsec X-ray pulses (up to 30 000 bunches per second).



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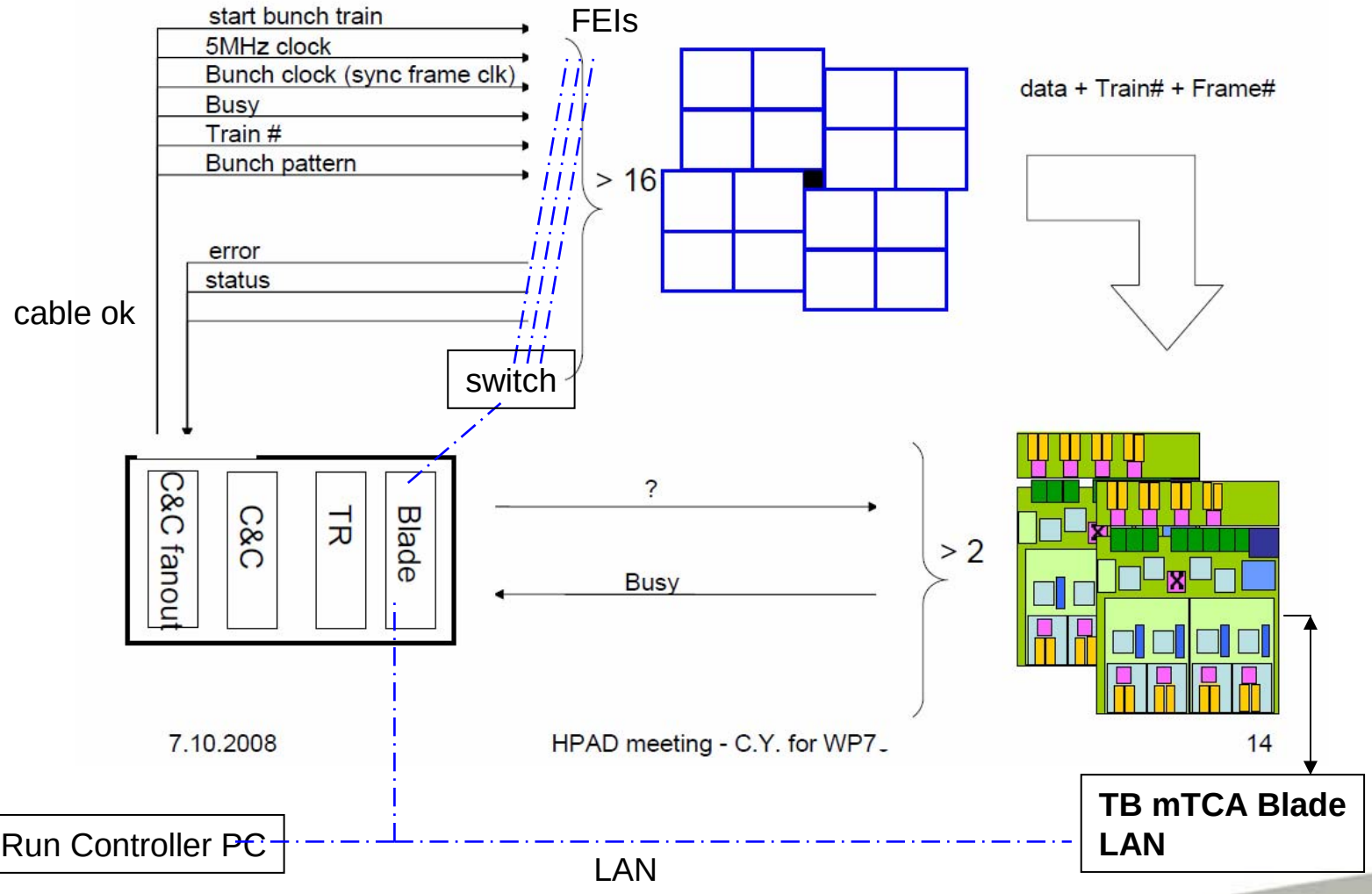
C&C signals and connections (complete?)



Train Builder
Clock and Controls

TB Boards in xTCA format. 20-30 m from detectors?
CC mTCA local to detectors.

Fast signals. Same electrical interface as FEI to CC?
Throttle (Busy) to associated FE mTCA.

Other comms via LAN?
Bunch train information from C&C to be appended to full Trains in Bunch Train header.
For redundancy checks against info in headers with detector data.

Indicate Ready/Error status.

Assume we do not need new hardware to interface TB

TB readout 10 Gb Asynchronous to FE clocks.

LAN interface via xTCA backplane to TB mTCA Blade. Slow Controls, DOOCs?
Receive Run status. Run parameters?
Feedback TB status.
Bunch train info via LAN?

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More questions

What, where and how do other data parameters get associated to FEE data?
In Data stream? At FEI, At Train Builder
Via CC Fast links or LAN
Or later associated via Dbase

What header data is needed with FEE data?

Per Run
Experimental conditions.

Per Train
Bunch fill pattern.
Bunch energies, currents?

Run States from Run Controller
Prepare Run : Setup samples?, Enable FEEs, Load calibration constants to FEI/FEEs , Load TB constants & logic
Start Run : Enable train start to FEEs
Stop Run : Disable FEEs

Spare Slides

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XFEL LPD ASIC

512 pixels

Analogue Pipelines
512 pulses deep **x 3 samples**

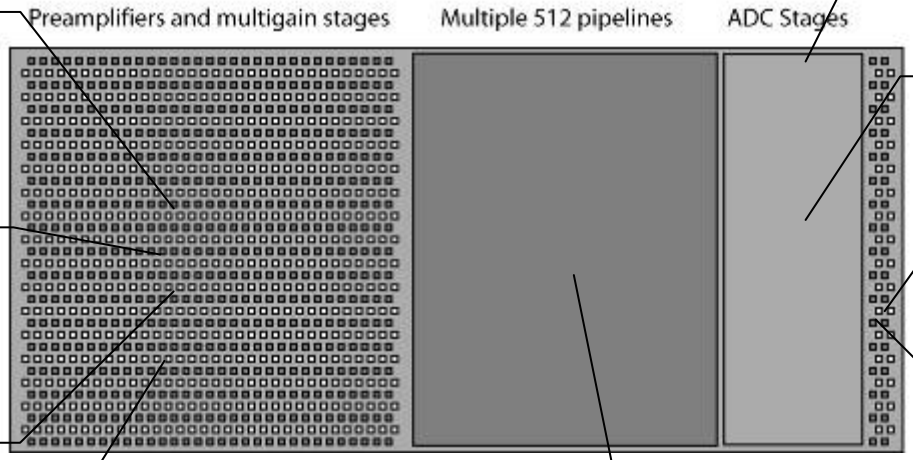
ADC
14 bits (12 eff) @ 8 MHz

Dynamic range stages

Overload Control

Pixel Resetting

Power supply Conditioning



Sequencing and control

ADC Stages

IO to DAQ

Power supplies

Store in Pipeline during bunch train
Readout during long gap

Deep pipeline memory (786,432 samples)

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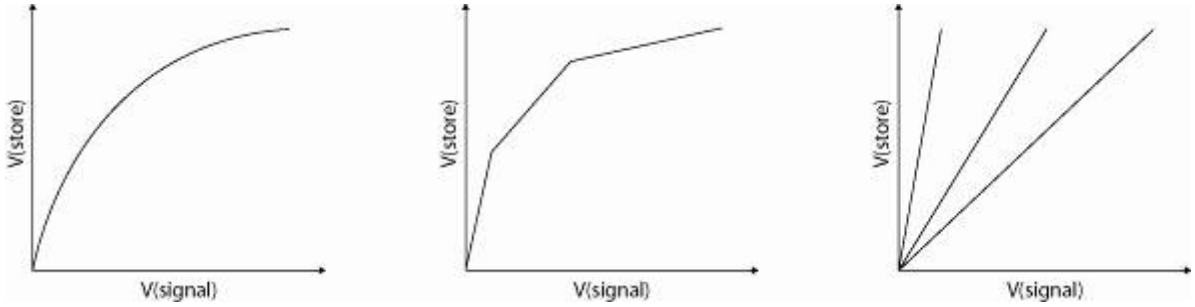
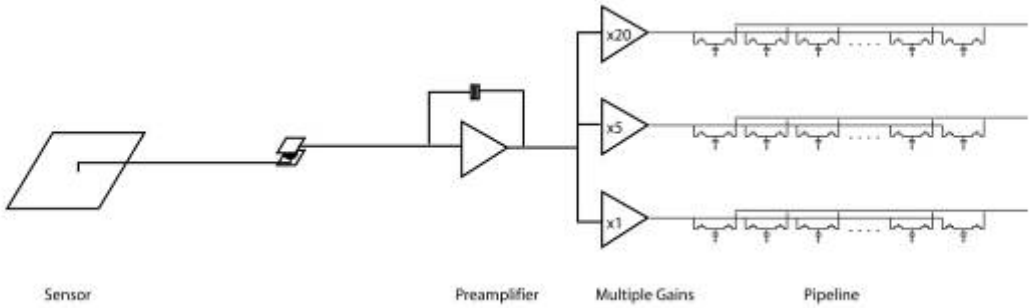
Multi-gain concept

Required dynamic range compression

- Experience with calorimetry at CERN
- Relaxes ADC requirements
- Fits with CMOS complexity





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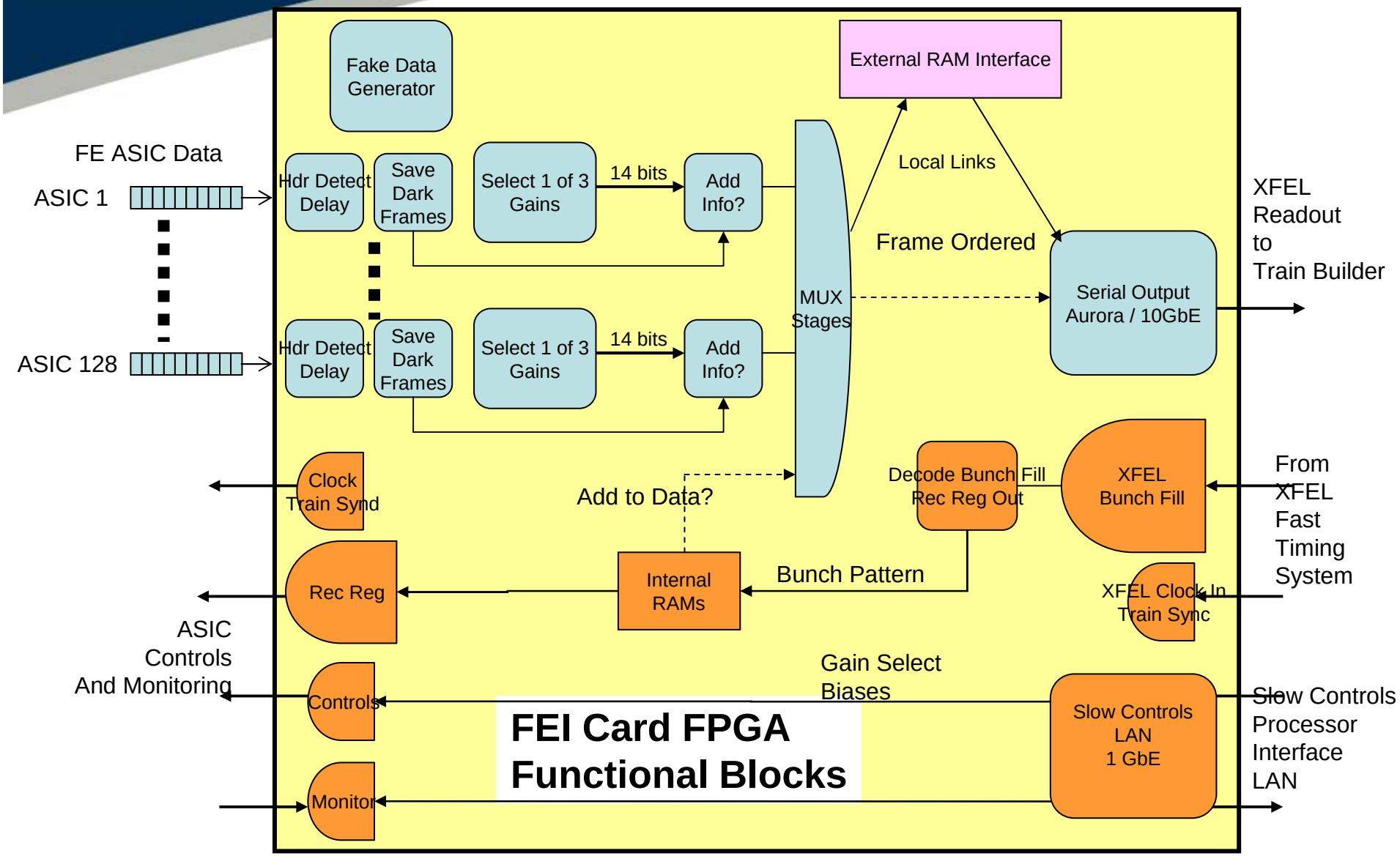

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