XFEL Timing System

Status 11.2008

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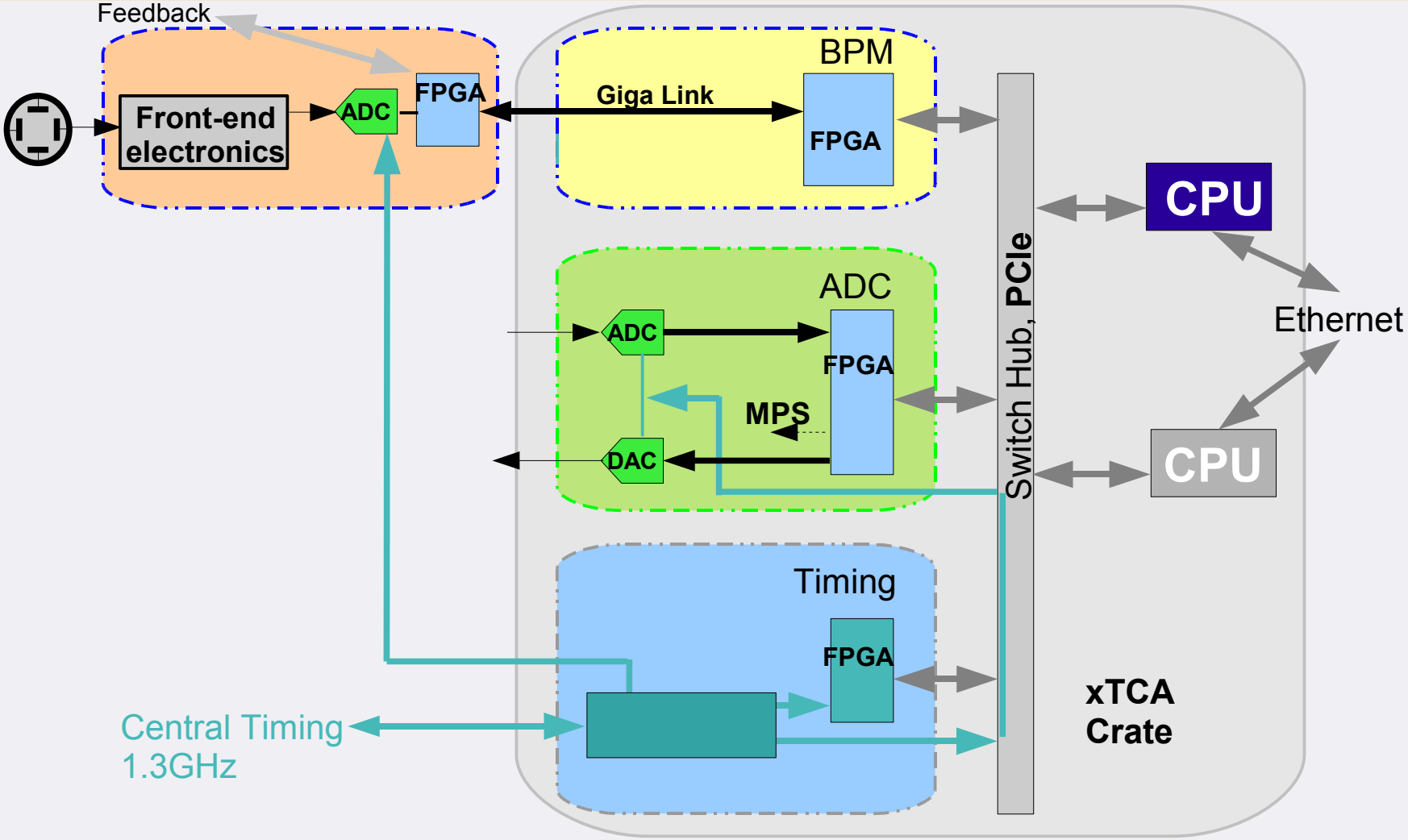
EDMS Nr.: D0000000001240941 Rev: A Ver: 1 Status: Released Dat.: 17.11.2008

The Front-end: XFEL Example



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Data Acquisition

Hardware:
receives clocks or patterns, triggers

to synchronize the bunches (ps stability)

RF/Diag
ADC
FPGA
clock
trigger
FPGA
Timing
PCIe
CPU
xTCA
Ethernet
Middle layer server
CPU
Tunnel

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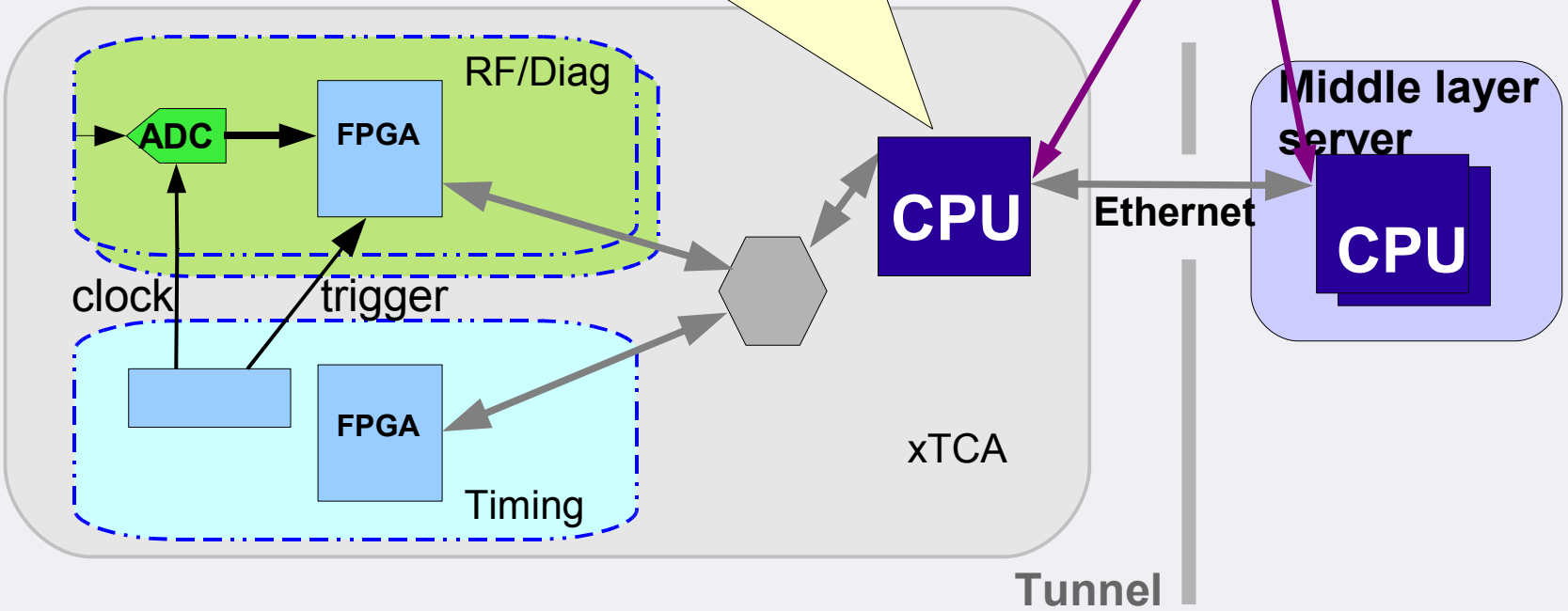
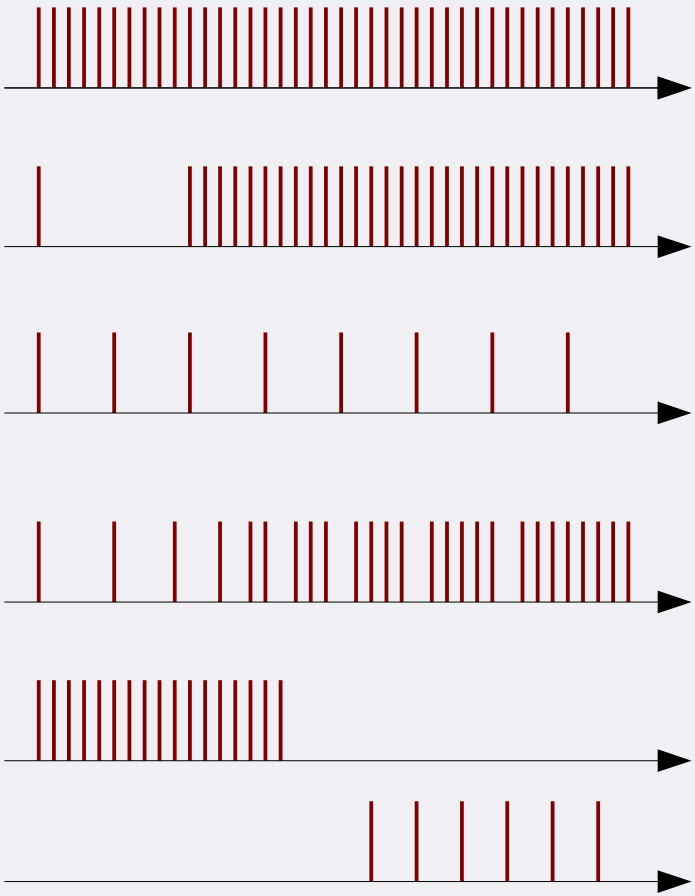
Data Acquisition

CPU:
receives event numbers, interrupts, modes

to synchronize the macro pulses for DAQ



Possible Bunch Patterns



Max: 5 Mhz, 3000 bunches

Pre bunch

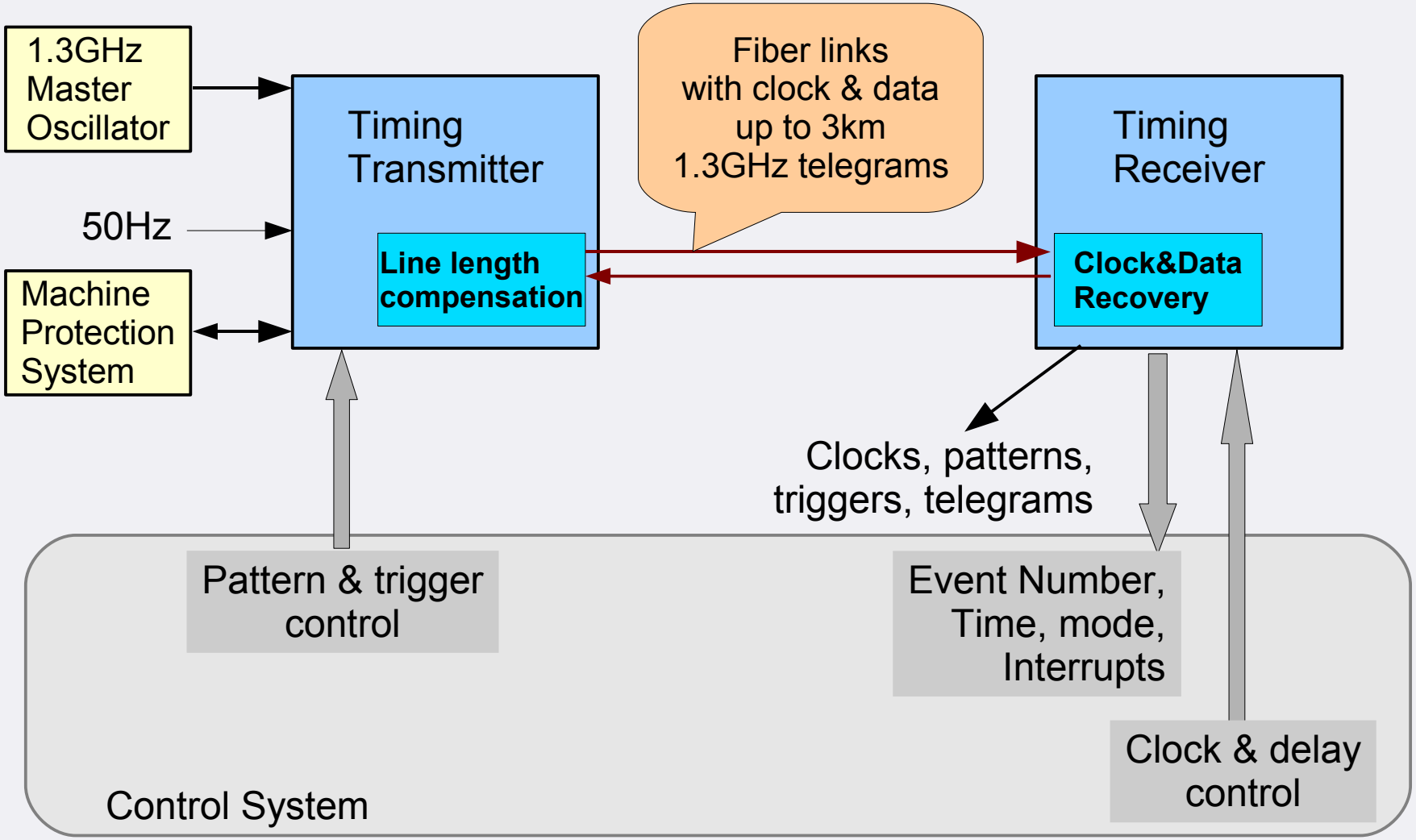
1 Mhz or lower frequencies

Arbitrary patterns

Different patterns @ different beamlines in one macro pulse

or varying patterns from shot to shot

Timing System Blocks



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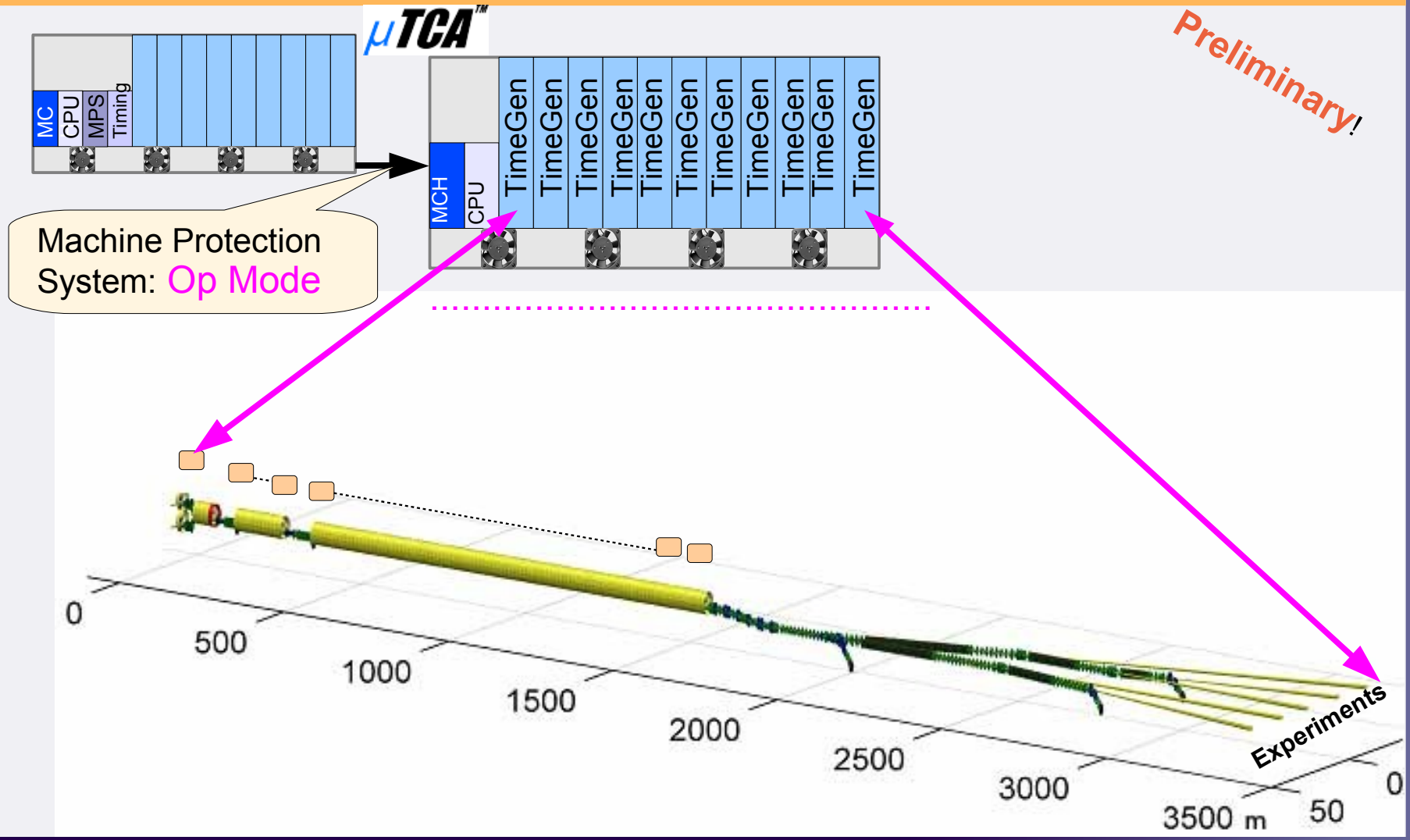
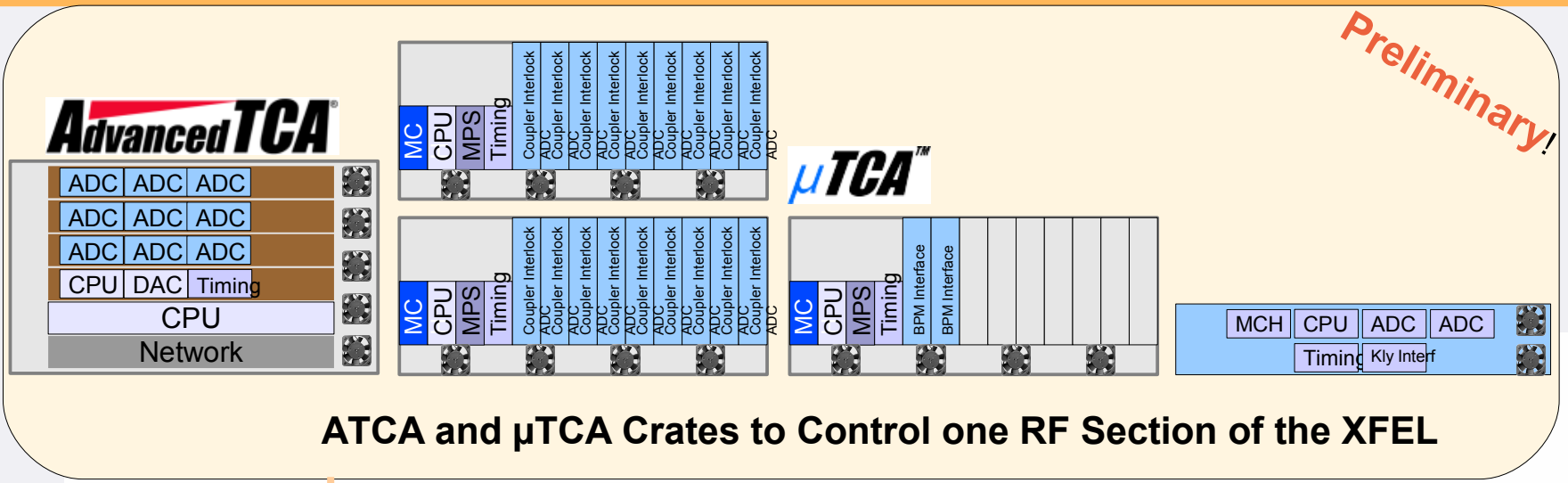
Timing System Requirements

- **1.3GHz telegrams**
  - With clock recovery, few ps jitter
  - Events and data for triggers, event number, modes, bunch pattern, (bunch charge?), ...
  - Sender compensates cable length, drifts and measures time delay from sender to receiver
- **Timing receiver outputs (hardware)**
  - Raw telegrams
  - Clock (and gated clocks) on front and backplane
  - triggers
  - Level (LVDS, LVPCL,..) to be defined
  - Connectors to be defined (e.g. infiniband)

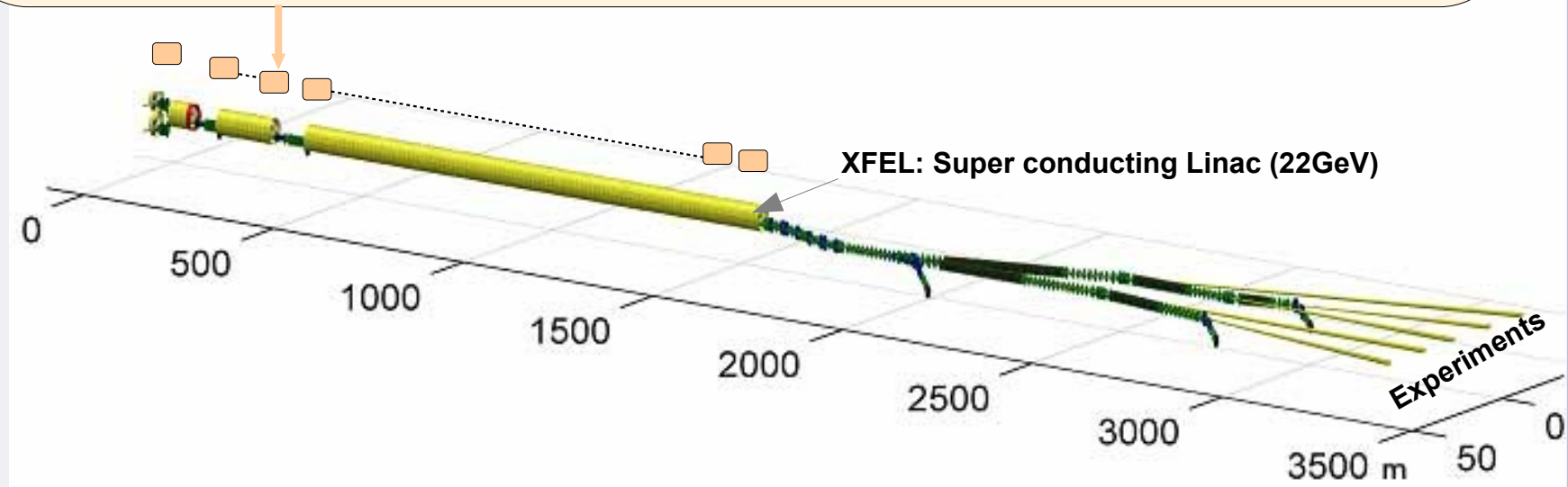
Star Topology to Distribute Timing



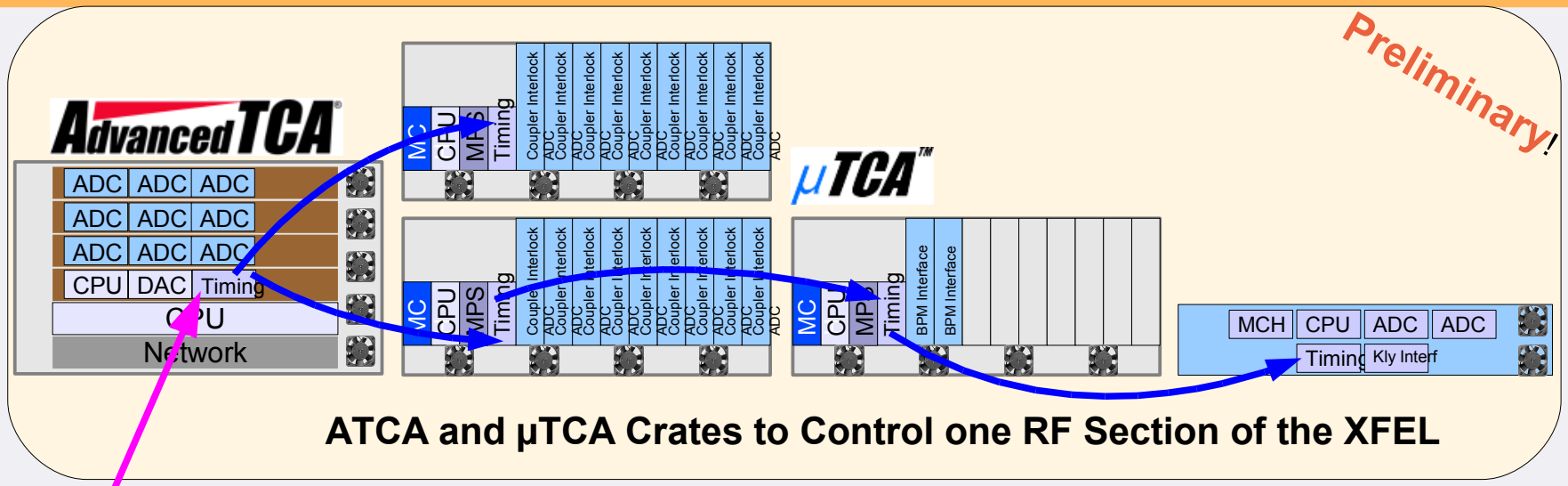
Geographical Layout of RF Stations



ATCA and µTCA Crates to Control one RF Section of the XFEL



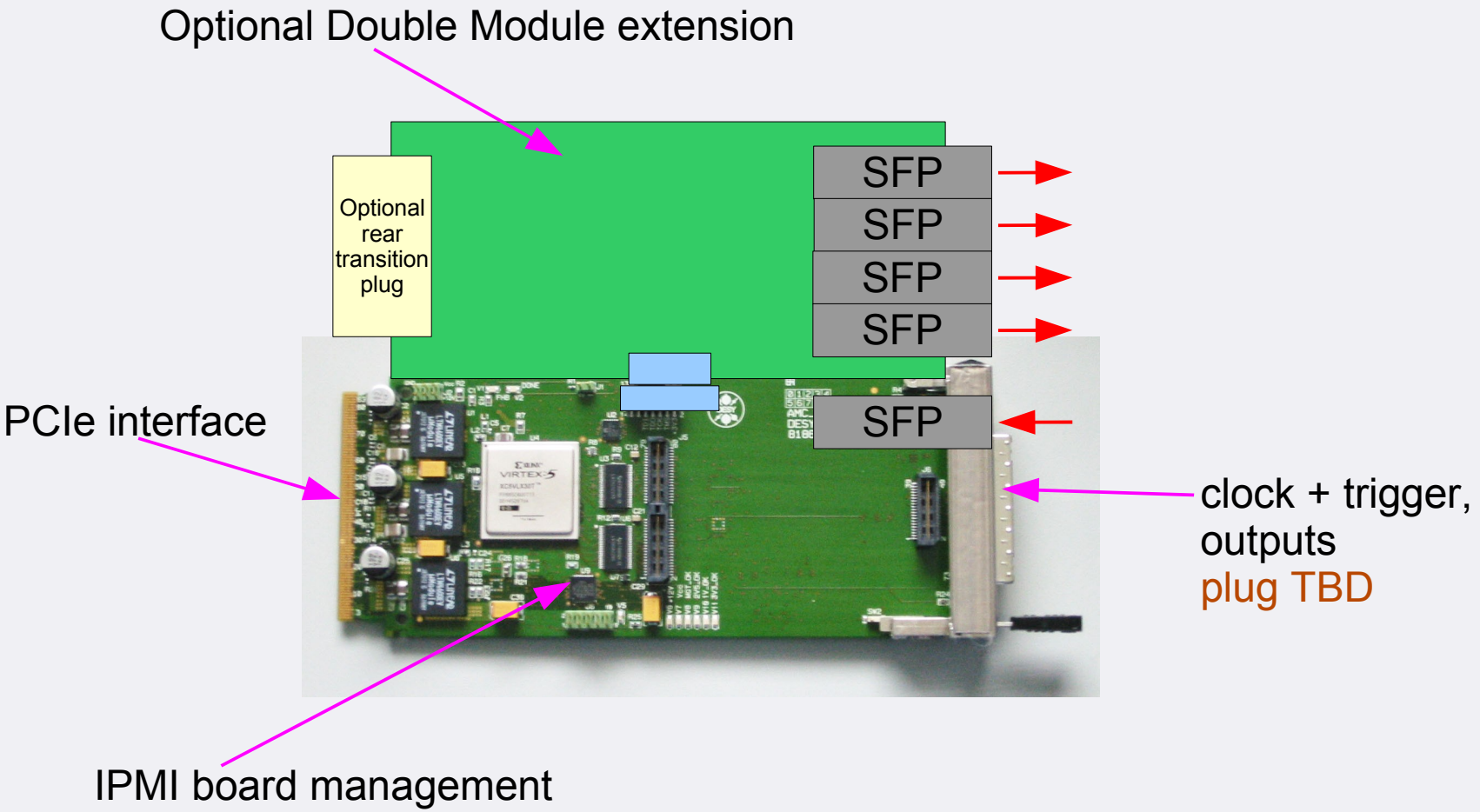
Possible Local Distribution



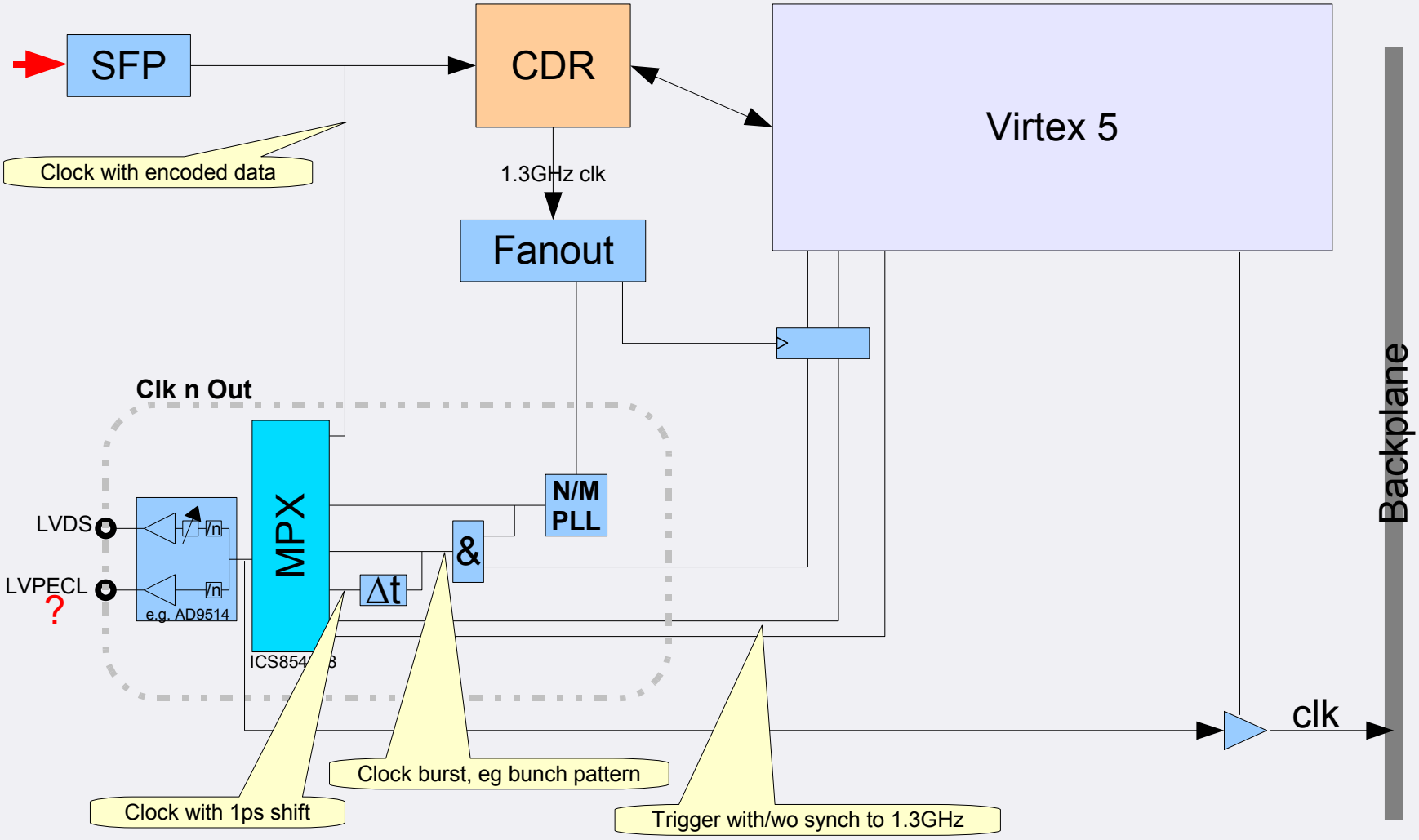
ATCA and µTCA Crates to Control one RF Section of the XFEL

Fiber optic
from central
timing generator

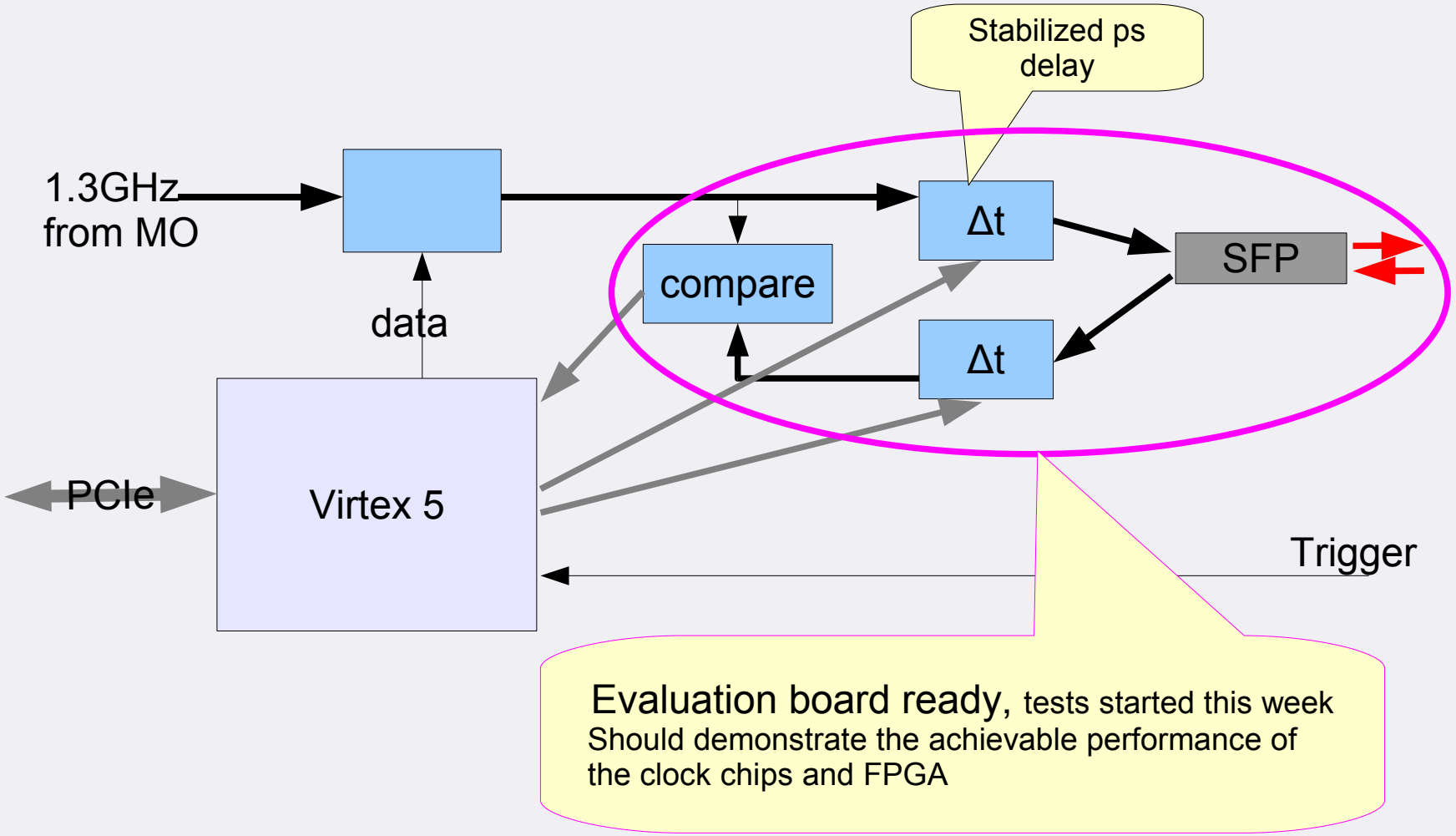
Possible AMC – Timing Receiver Module



Preliminary: output block



Preliminary: sender block



Evaluation board ready, tests started this week
Should demonstrate the achievable performance of
the clock chips and FPGA

Specs PRELIMINARY

- **Trigger:**
  - timing resolution: 1.54ns (0.769ns)
  - Programmable with 32 bits (up to 6s (3s))
- **Clocks:**
  - Jitter: < 5ps RMS (goal)
  - Constant or burst (e.g. bunch clock)
  - Automatic adaption of location/beam mode
- **Raw 1.3GHz telegrams with encoded data**
  - Data format is not yet fixed
    (number of filler words for the clock recovery to be defined)

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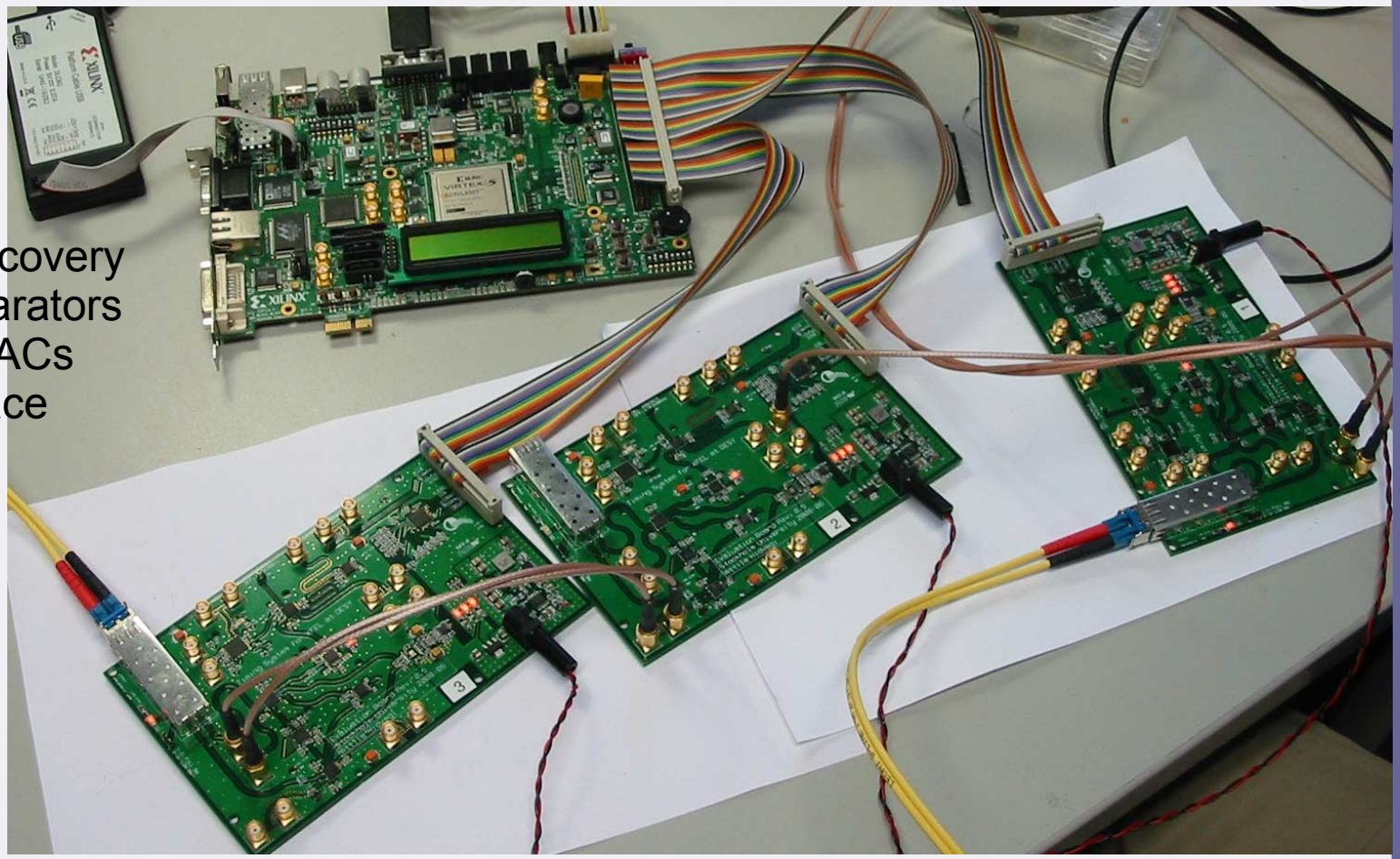
3 Test Boards connected to a Virtex 5

Contains:

fiber optic IO
delay chips
clock data recovery
phase comparators
ADCs and DACs
FPGA interface



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Outlook

- **First prototype**
  - Design ready 2008
  - Tests in January 2009