Minutes of 2D detector C&C and XFEL timing groups meeting (12.10.2008) and the C&C meeting (13.10.2008)

C.Youngman 14.11.2008 (last revised 16.11.2008)

1	Timing meeting attendance list	1
2	Note about the minutes	1
3	Terminology	1
4	XFEL timing system - K.Rehlich	2
5	Experiments timing receiver board description - A.Hidvegi	5
6	Requirements from the experiments - C.Youngman	5
7	Requirements from the Train Builder - J.Coughlan	6
8	Post Dresden decisions w.r.t. crate standards - K.Rehlich	6
9	C&C meeting attendance list	8
10	Pro's and con's of separate control and data handling - P.Goettlicher	8
11	Pro's and con's of combined control and data handling - A.Kugel	9
12	Clock&Control specification discussion	10

1 Timing meeting attendance list

UCL: M.Warren, M.Postranecky and M. Wing. DESY-FEA: M.Zimmer and I.Sheviakov. Stockholm/WP28: Ch.Bohm and A.Hidvegi. MCS4: A.Geissler and K.Rehlich. LPD detector and TB: J.Coughlan. AGIPD detector and DESY-FEB: P.Goettlicher. XFEL: J.Gruenert. DEPFET detector: A.Kugel (via EVO). WP76: S.Esenov and C.Youngman.

2 Note about the minutes

Rather than trying to write down every word that was said I've decided to keep the text to a minimum and summarize the talks by listing useful statements and definitions, open questions, etc. This is usually done from the 2D pixel detector point of view. **Bold** text indicates an important question, conclusion, etc.

The agenda, slides and these minutes are available at http://xfel.desy.de/project_group/work_packages/photon_beam_systems/wp_76_dag_control/timing/

3 Terminology

To avoid confusion 2D detector terminology is used throughout, what this translates to in timing terminology is as follows:

• Detector group = Timing group

- Train number = event number.
- Train (or bunch train) = macro-bunches.
- Delivery of a train = a shot.

4 XFEL timing system - K.Rehlich

Detectors interface to the timing system using a Timing Receiver (TR) board. A schematic of the proposed e-beam Beam Position Monitor (BPM) diagnostic system (4 beam pickup buttons or cavities) was shown, which shows how the TR board connects to the DAQ readout board and PC blade in a xTCA crate.

TR implementation:

- Currently the TR is planned to be a single height (height in the VME or CAMAC sense) AMC board, or possibly a double height board.
- There is a single height generic AMC carrier board developed by FEA which is a starting point for the TR design; its implementation:Virtex 5, PCIe backplane, IPMI board for crate management, etc.
- TR definitions are still required form many items: connectors types, etc.
- The proposed TR FPGA will have lots of space, but it should not be used for additional foreign firmware.
- The TR has no standalone timing generation capabilities, if needed a separate sender board can be used to drive the TR.

The TR is connected to the timing system's 1.3GHz clock via a front panel SFP fibre input. Data modulated onto the clock are:

- Triggers signals which identify a instance in time, and
- Telegrams additional information which accompany a trigger.

The timing distribution system ensures that the triggers are always delivered at the "correct" absolute time to any TR in the system (3km maximum TR to Master Timing Generator (MTG) separation, at $3ns/m = 0.3\mu s$)

Points associate with triggers:

- Examples of triggers are the "start train" trigger.
- Triggers are uniquely identified by an identifier number which is delivered to the TR user.
- Any number of triggers can be defined at the central trigger generator.
- All triggers are distributed to all TRs(?).
- Which triggers are passed on to the user (detector DAQ) are configured at the TR.
- Delivery of the trigger to the DAQ can be delayed by configuring the TR..
- Within a train all triggers are separated by known fixed periods. Inter train differences are not predictable. Difference between 2 trains can be 100µs due to synchronization of the linac with the mains frequency. There was a discussion about whether this was needed, if not then phase jumps would not be present the conclusion was that phase jumps could not be avoided.

• The "start train" trigger should be ~15ms before the train arrives. Maybe it should be called something else like "train configuration" trigger and define another trigger to be the real "start train" trigger later than the "train configuration" trigger, or may be the C&C should generate this second trigger internally.

Points associated with telegrams:

- Telegram information payload is always associated with a trigger (follows it).
- Example payloads: the train number, the absolute time, bunch occupation patterns, ...
- The bunch pattern format has to be defined, but it will be more than just an on/off bit per bunch as it must include beamline information (not all bunches go to all beamlines), etc.
- Do train number and absolute time always accompany triggers?
- There is essentially no limit to the payload length.

Obvious detector usage questions that arise:

- If an ID is used to index into a set of bunch patterns previously configured into the detector Front End Electronics (FEE), the index ID will have to be added to the telegram definitions where are these definitions made? The linac RF system uses a similar indexing scheme.
- If the bunch occupancy pattern is distributed by the timing system how do the experiments get the data on cold start or reset?
- Does the C&C have to check that the delivered bunch pattern is correct especially if an index is being used?
- The train number is a unique number. From the DAQ point of view it should never repeat and should continuously count (e.g. Event number = GPS time divided by something) even if it requires more that 32bits.

The BPM schematic shows a xTCA crate filled with TR, PC and readout (FEI) interface boards, where:

- the PC is used to configure the TR (enable triggers to be delivered, etc.).
- the TR can be configured to interrupt, via PCIe, a user process on the PC which gets the trigger number and can read any additional telegram data(?).
- the TR can deliver trigger and telegram information to the FEI directly via the crate backplane.
- The schematic is very similar to the ideas for 1D detector readout in the photon beam line systems, may be there is room for collaboration.

The preliminary TR timing performance specs were reviewed. Trigger:

- Timing resolution = 1.54ns, which can be synched to the bunch clock to get few hundred pico-sec accuracy.
- Programmable 32bit delay = 6s, which is meaningless for standard 10Hz train repetition rates.

Clocks:

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- Jitter \leq 5ps RMS.
- Constant (continuous) bunch clock or burst (the "or" is dangerous at least continuous is needed).

Raw 1.3GHz telegrams with encoded data:

• The data format is not yet fixed (the detectors need to be included in the definition process to define the trigger and payloads that they need).

Discussion of detector clock and timing requirements:

- The detectors would like the PLL, see slide 12 "output block", clock from the TR to be available, without phase shift. Can be distributed by the C&C system. Need a clock in the detector head. Kay says a 10MHz or 5MHz or 10GHz fixed w.r.t. to the bunches. Does the clock jump only in multiples of 200ns (the bunch frequency)? What was the answer?
- AGIPD needs: a known clock whose phase is fixed w.r.t. the bunches for storage pipe line control/operation and a continuously running without phase jumps arbitrary fixed phase w.r.t. pulses.
- LPD and DEPFET need: one continuously running clock with fixed phase w.r.t. bunches. Multiply up a 10MHz or 5MHz to 100MHz at the C&C would be OK.
- There is no way that the 200ns inter-bunch period can change, inter-pulse periods of 400, 600ns, etc. must be generated by setting the appropriate bunch occupancy pattern.
- Experiments require a few hundred ps to 1ns resolutions.
- AGIPD: if 100MHz clock available, can tolerate jitter no PLL then few nsecs; if PLL then need better jitter.
- From the detectors point of view an FPGA generated signal is OK.
- Preliminary specs. for DEPFET: assumes that generating the ADC clocks from the a continuous (reference) clock. Need to know what the allowed jitter is for DEPFET. Deriving from the 100MHz generated clock seems to be the easiest and cheapest solution.

The conclusion was that the TR would output a 5 or 10MHz clock whose phase is fixed w.r.t. the bunches and the C&C would multiply this up to 100MHz and distribute to the detector FEE. <u>There seems to be plenty of room for confusion here,</u> this issue must be watched to ensure that the correct clock output is produced.

The machine protection system (MPS) hardware is used to collect (?)(and distribute) error states in the machine. If the beam is off position at the detector the MPS has to be used to stop beam delivery. One could imagine monitoring the difference of BPM or intensity monitor signal on either side of the detector to determine whether the beam is hitting the detector (pixels hit by the beam are dead). The MPS hardware can/will be made available by Kay's group. **Does the interface hardware already exist? Is it AMC format? How does it interface to the blade PC. Is there a user manual or specification? Can we already test this module? How does the C&C and overall detector control handle the MPS system? Does a description of the MPS exits?**

5 Experiments timing receiver board description - A.Hidvegi

An overview of the status of the current test board: chipsets tested, test of key functionality, characteristics of key components like temperature stability, etc. was given. Test board measurements: 1.3GHz jitter RMS 2.5ps – but no control, was allowed to drift to see the drift size effects. The resolution might be better, but may also have a sine wave jitter component which is not seen.

Next prototype discussion:

- will allow adjustable phase and frequency divider on all clocks. Two solutions for clock generation are considered, FPGA and discrete chipsets. FPGA generation should be accurate enough for the detector requirements. Discrete chipsets will be needed for more demanding users like LLRF. Both will be tested in the next prototype. The phase resolution of the FPGA solution should be less 100ps. The divider is limited in the discrete component solution. A solution using logic in FPGA accompanied with re-synchronizing outside the FPGA is also possible, this could be as good as the discrete chipset solution and is expected to be cheaper. Form factor AMC for micro-TCA and ATCA. Separate micro-controller for MMC.
- Backplane issues. How to distribute the clock needs looking into due to the design and use of the backplanes. Currently the group has no experience of distributing fast clocks, which is why a prototype is being built. If double height were to be used then could define own backplane. Question of standard backplanes.
- Driver software will be provided for the boards users.
- Recommended hardware test environment see Kay's crate talk.
- Time line. Testing of next prototype starts Jan 2009.
- Self test standalone running functionality running without the fibre 1.3GHz signal is not foreseen. Needs thinking about. The conclusion was that detector side standalone functionality has to be provided by the C&C and nothing should be expected from the TR. The C&C also has to support operation at other light sources with their time structure.

6 Requirements from the experiments - C.Youngman

A brief overview of the 2D pixel detectors planned for XFEL was given (what the data the processing/flow looks like, what the XFEL readout architecture looks like, etc.) The train builder, which builds complete frames using input from the detector readout module interfaces (16/1Mpixel sensor), was also defined.

A proposed scheme for connecting detector FEE, clock and control (C&C) systems, and the train builder readout system was shown ("C&C signals and connections – basic idea" slide).

The definition requirements of fast signals, clocks and other information sent between: C&C to FEE and FEE to C&C were reviewed. As these and other C&C implementation details are more accurately recorded in the C&C meeting discussion, they are not written out here and the reader should look through Section 12.

7 Requirements from the Train Builder - J.Coughlan

A brief overview of the LPD front end was given. The ASIC requires a 100MHz clock from the C&C, start train, and bunch occupancy patterns from the C&C and timing systems. The LPD were thinking of receiving LVDS lines to receive: a pattern index ID, train number, etc.

TB signal interchange with the C&C system. As these and other C&C implementation details are more accurately recorded in the C&C meeting discussion, they are not written out here and the reader should look through Section 12.

The train number, bunch number, bunch patterns, etc., must be added to the data sent to the TB. A data format needs defining (pixel then rest).

Adding additional slow data (veto decision, timing, extra cameras, machine data, etc) should not be performed at the TB, instead the data should be sent to the PC layer for inclusion in the output data streams.

8 Post Dresden decisions w.r.t. crate standards -K.Rehlich

Many, 6-7, crates have been acquired and used over the last 18months. List of points reviewed during evaluation (see slides for details):

- Interchangeability of boards between different vendor crates.
- All crates had at least 1 problem: power management, fans too loud, etc., but vendor response to problem solving (new firmware, etc.) was good.
- Crate (+hub+cpu?) prices: 3.5 thru 5.5 kEurs, depending on number of slots, backplane, hub performance, etc.
- Most manufacturers support mid size (width) modules.
- Commercial IO modules are now becoming available, e.g. carriers for IP modules, ADC, etc. (ADLINK, Strueck, Tews...).
- Universal AMC board built by FEA at DESY is available.
- How to update FPGA firmware remotely is being addressed being addressed.
- IPMI crate monitoring and ability to reboot CPU.
- AMC cpu/disk systems evaluated.

• DOOCS protocol connections to crates talks IPMI to the shelf manager in the crates. This software (+GUI) could be bundled into a tarball for other users, if required.

Experience gained slides:

- Design of a module must follow specs precisely. Many starting problems.
- Advantage of micro-TCA is power switching (hot plugging) boards.
- Power management is useful.
- Fan speed control is important.
- Backplane configuration must be carefully chosen there is no Research Lab type standard as yet.
- Network boot feature of CPUs is required.
- Some PCIe configuration problems Solaris can hot swap on PCIe (since a few days), not possible on Linux.
- IPMI standard well defined this is not the case on PCs.
- Management of crate is well defined.
- Expected high backplane bandwidth performance of xTCA seen.
- Good analogue performance.

Wish list:

- Standard crates, standard backplanes, ...
- PCIe with multiple computers.
- Redundant power supplies tendency is to reduce this to simple solns.
- IPMI commands to switch off a crate or a module in it, is required.
- Software standards for interface between FPGA and CPU operating system.

Next developments w.r.t. detector and xTCA usage. Believe that xTCA is the correct way to go – number of vendors is increasing rapidly. ADlink, Struck, Tews producing IO and PC boards.

The long term aim is to define a standard crate and make a mass order for XFEL. Test to final system work: planning to make standard cooling airflow direction for front to back, bottom to top – one has to be careful what you put in the create. Other users at DESY LLRF – price issue is becoming important. ATCA blade with two 10Gb links. = 5k\$.

The DESY-FEA generic AMC board is freely available to collaborators, firms have to pay.

A starting point decision on which crates to buy for the TB and UCL is to buy the same crate as M.Zimmer i.e. Schroff which is a double AMC height crate with most of the required features and LOUD fans. This ______ is space for Manfred to insert the crate type.

9 C&C meeting attendance list

UCL: M.Warren, M.Postranecky and M. Wing. DESY-FEA: M.Zimmer. LPD detector and TB: J.Coughlan. AGIPD detector and DESY-FEB: P.Goettlicher. XFEL: J.Gruenert. DEPFET detector: A.Kugel (via EVO). WP76: C.Youngman.

10 Pro's and con's of separate control and data handling - P.Goettlicher

A brief review of the task of control, for AGIPD, was given. The slides should be look at for details. For the HEP people amongst us, control means slow control of elements like (setting and monitoring: power, vacuum, cooling, etc.) plus C&C of the detectors acquisition and readout electronics.

The requirement of keeping data together was discussed:

- The train builder is a conduit for event building module pixel data into frame ordered trains.
- Additional detector, train relevant, data exists, like: slow control monitoring values, bunch patterns used, XFEL machine parameters, etc.

How this data is handled is not yet defined:

- The XFEL architecture points towards keeping data from different sources in different files.
- Sources are: train builder, slow control, additional associated commercial cameras and machine parameters, etc.
- Sources other that the detector module links are slow and will not be acquired at the pulse rate at the detector, instead they arrive over the network which means that they could be late = should not be merged at the TB.

The conclusion is that we should assume that keeping the data in different files and allowing the PC layer to receive this data without trying to go through the TB is the best solution.

A data format for the pixel data pushed into and out of the TB will be required!

Listing of pro's:

- Control and high speed data handling are different task with different considerations of interactions to detector head, infrastructure...
- High speed optimized to data throughput: FPGA's and protocol in logic-cells Control easier in controller architectures and secure protocols: m-Controller, TCP/IP, 100MbE.
- Different expertise of programming and system build up.

- Different persons, different technologies.
- Control must be possible with priority at all time, would interrupt high speed data transfer.
- Control changes most likely quite often with user new sensors, discontinued infrastructure... Less debug time with expert only for "control like programming", if high speed is disentangled High speed data changes only consideration of laboratory.
- Other beam line: only control changes train builder only configuration, if considered well.
- Links of frontend-to-backend are not one-to-one as control: AGIPD plans for 16-Modules and/or 4 quadrants.
- Detector/beamline control is needed all the time, also when long preparation times without data taking and possibly.

Listing of con's:

- More cable (2 wire-pairs per link).
- Additional network switch.
- Additional communication channel: control to backend.

Both architectures are possible. eparate systems: control is master, favoured because both tasks looks well separated with only a few signals to interchange. Most user commands concern "control".

For discussion see Section 11.

11 Pro's and con's of combined control and data handling - A.Kugel

Control for DEPFET will consist of precision signals (clock, trigger, ...) needing separate copper connections and messages (configuration...) can be on a general purpose network. Keeping control and data paths apart is good design practice

Why consider to use combined path?

- DEPFET uses I/O modules with tight space constraints.
- Data and control paths (initially) assumed to be uni-directional only (and opposite directions).
- Data and control can use same protocol: UDP.
- Data and control ultimately be handled by same device (FPGA).

Common path for data and control messages pro's and con's. Pro's:

- Save space (fewer conectors), cables and components (PHY).
- Simple test setup PC with 10 GbE NIC for DAQ and control; big advantage is the prototyping phase.

Con's:

• Need to insert control messages into data path at higher level (train builder)Bidirectional protocols ("secured" UDP, monitoring, …) require more complex design of module FPGA logic and Train-Builder networking. Can we do it at the Train Builder?

Discussion concerning separate or combined data and control paths:

- Is the advantage during the prototyping phase real? If combined at the TB will it eventually require using a custom prototcol, i.e. not UDP?
- Combined data and control at the TB could probably be done, but gut feeling is that it makes things probably very complex and should not be done.
- People have separate abilities and going to combined data and control on a single link cuts many out, which is not good for partitioning the work especially at different sites.

The conclusion was to keep data and control links separate.

12 Clock&Control specification discussion

General requirements:

- For prototype testing and final running of the detectors the C&C must interface to other light source timing systems (LCLS, FLASH, Spring8...) and run standalone without external timing input.
- Flat field and other calibration run types require running the detector in stand alone mode and the C&C must support this.
- All information to the TB is sent via messages over an IP network (TCP assumed). A PC blade in the crate hosting the (>1) TB boards receives (train number, bunch pattern...) and distributes the messages over the backplane to the TB boards. The PC collects status information (periodically after each train and on request) from the TB boards and monitors and makes this information snapshot available over the network. The PC is responsible for board configuration and debug operation.
- Configuration information (messages) sent to the FEEs is sent from a PC in the C&C crate. The FEEs must provide status information (periodically after each train and on request) to the PC. The PC is responsible for FEE configuration and debug operation.
- The C&C must provide fan in and out for signals exchanged. For all 1Mpixels detectors 16 data links are used. The number of FEE connections may not be 16, it might be 4, 16, 20 depending on detector. Additionally the 2013 detector might scale to 2 or 4 Mpixels. The size increase must be foreseen in the C&C design.
- The presence of the XFEL timing receiver board is sensed via 50Hz heart-beat. The failure of a whole train or part of it is distributed by the machine protection system, which seems to be outside the scope of the TR – needs checking.
- There are no radiation and magnetic field issues, i.e. the detectors operate in a laboratory environment.

• Prototyping when C&C not available – detectors should use sequencers.

Links:

- Timing signals and clocks, **called collectively signals**, are distributed on dedicated cables (LVDS, differential).
- Configuration, debugging, and monitoring information, called collectively messages, are distributed on a network (100Mbit/s?)

C&C to FEE signals:

- Start bunch train arriving at the FEE say 15ms before the first pulse, the internal delay in the FEE actually times in the first pulse. Payload on this is the Train number, ID of pattern (always use an ID to define a pattern,). End buch train is also on this line so a protocol is needed.
- Bunch veto must be synchronized to the internal clock (see AGIPD for details)
- Bunch clock; a 100MHz clock, derived from the timing system, without phase jumps w.r.t. the bunches.

FEE to C&C signals:

• FEE module is plugged in and on – leave open the option of encoding additional data onto this line.

C&C to **TB** signals:

• None

TB to C&C signals:

• None, a busy throttle signal generated at the TB will probably be sent as a network message.

LEDs:

- On FEE board showing clock is running
- On C&C board showing that the cable is plugged at the FEE module and that the FEE is on.

Cables and grounding:

- LVDS is preferred on patch cables with RJ45 connect. The C&C to FEE lengths should be short (~5m) and not problematic for signal driving.
- All are shielded and isolated at the C&C side (using magnetic ac couplers).
- Grounding is defined at the FEE.
- Cables should be halogen free.
- The patch cable should include all signal links and the configuration network connection.

Handling FEE to C&C signals:

• Using a Virtex5 for collecting 8bits of data per module connection looks like overkill. Think about an internal bus or other solution.

Time line:

- Work that can be started using a C&C evaluation board design to test start bunch sending and other straight forward issues. Look at isolation issues.
- Non trivial prototype detectors will appear 4th Quarter 2009. Need feedback from LPD and other detectors.
- The UCL C&C group will present an update at the TB meeting on 4.12.2008.
- The group should start work on an in-kind contribution proposal.

The DAQ interconnectivity between the different 2D pixel detector sub-systems is shown below.



Figure 1 Conceptual layout of a 2D pixel detector's DAQ sub-systems

The HV and LV system are shown as external supplies. Serial powering could reduce the number of power lines, but the number of crates will stay approximately the same.