

xTCA TM

**PICMG® Specification MTCA.4
R 1.0 Draft 0.7gx**

AMC, μ RTM and μ TCA Shelf for Physics

10 September 2010



**Open Modular
Computing Specifications**

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1 Introduction

1.1 Objectives

The purpose of this document is to define an AMC and a corresponding μ RTM module set that can be used in an appropriate μ TCA shelf.

1.1.1 Reference documents

The publications cited in this section are relevant to this specification. Most of the specifications referred to are subject to periodic and independent updates, and are the responsibility of their respective organizations. The reader is advised to check carefully the version or revision of the referenced specification that is to be used in conjunction with this document.

1.1.2 Reference specifications

All documents may be obtained from their respective organizations.

Document	Organization	Contact information
PICMG 3.0 R3.0	PICMG	
PICMG AMC.0 R2.0		
PICMG IRTM.0 R1.0		
PICMG IRTM.1 R1.0		

1.1.3 Environment and regulatory documents

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In this specification the following key words (in **bold** text) will be used:

- may:** Indicates flexibility of choice with no implied preference.
- should:** Indicates flexibility of choice with a strongly preferred implementation. The use of **should not** (in **bold** text) indicates a flexibility of choice with a strong preference that the choice or implementation should be prohibited.
- shall:** Indicates a mandatory requirement. Designers **shall** implement such mandatory requirements to ensure interchangeability and to claim conformance with this specification. The use of **shall not** (in **bold** text) indicates an action or implementation that is prohibited.

Note: When not in bold text, the words “may,” “should,” and “shall” are being used in the traditional sense; that is, they do not adhere to the strict meanings described above.

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1.7 Acronyms and definitions

The following terms and acronyms are used in specific ways throughout this document.

1.8 Revision history

Date	Revision	Changes
13 Aug2009	D0.1	Introduction and major section headings
	D0.2	Outline complete at all header levels
	D0.3	
	D0.4	
	D0.5	
	D0.6	
	D0.7	
	D0.8	Ready for Final Subcommittee Review
	D0.9	Ready for Member Review
	RC1.0	Ready for Adoption Ballot
	R1.0	Adopted

2 Mechanical

2.1 AMC for Physics Module

2.1.1 Printed Circuit Board

The outline of the Physics AMC **shall** follow PICMG AMC.0 R2.0, Section 2.2.1.2 except as noted in Figure 2-1.

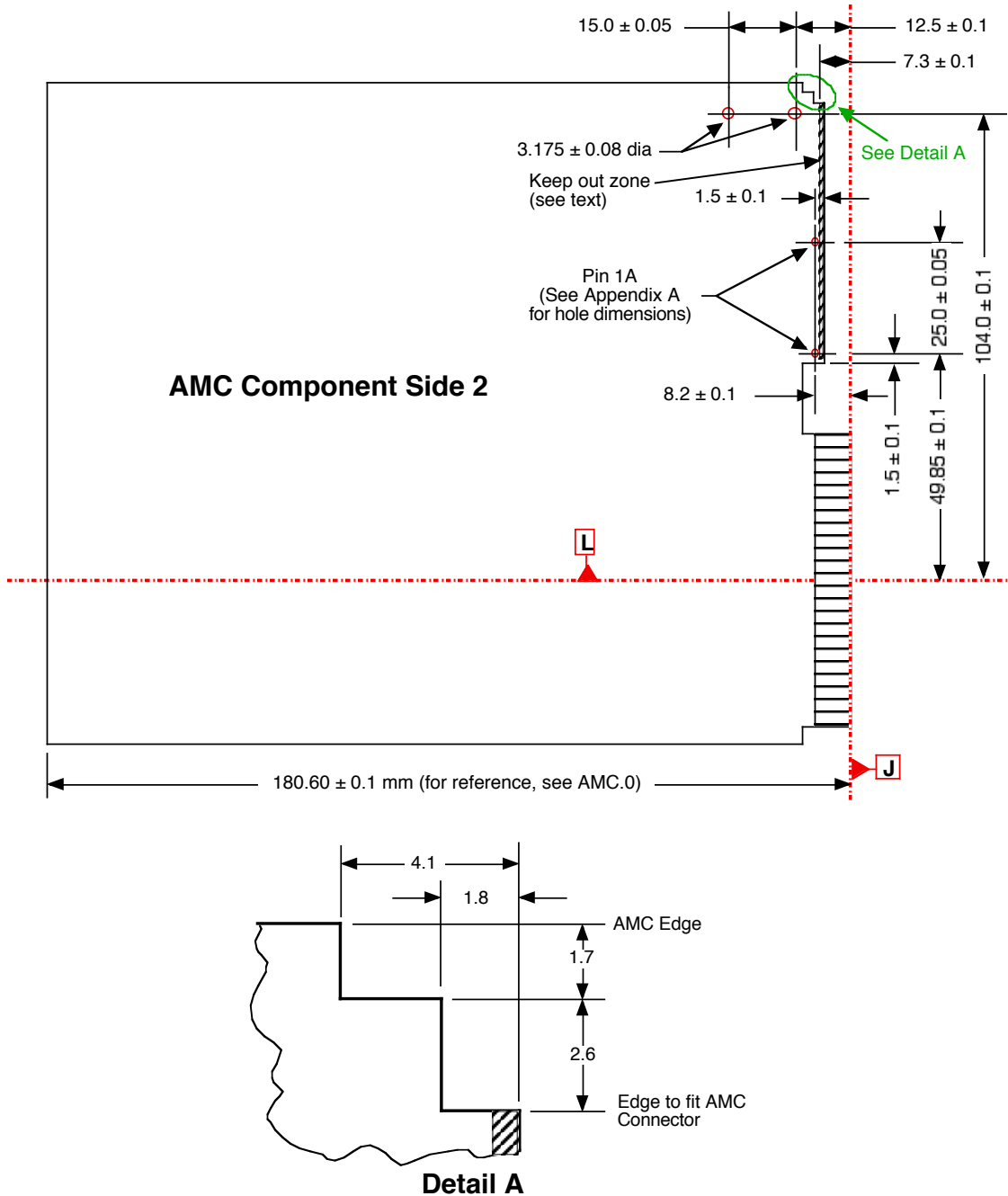


Figure 2-1: Physics AMC Dimensions

Unless otherwise noted all dimensions conform to AMC.0 R2.0. Note that although the AMC outline is similar to AMC.0, Figure 2-5 the profile in the Zone 3 area is different. The profile in that area was specified for the case when there were two backplanes in a doublewide shelf. The outline insured that the PCB missed the upper backplane AMC connector. Since that area is now specified for attachment to a μ RTM the old outline dimensions have been changed. The reference 42.5 is now 48.35, 107.5 is now 110.05 max., and the setback from Datum J that was 7.5 is now 8.2. The old outline was just the start of another edge card connector but with the fingers removed and cut short. The inside and outside PCB corners in the Zone 3 area **shall** follow AMC.0 R2.0, Section 2.2.2, Figure 2-12 (Inside edges to be R1 and outside edges to be R0.5).

Detail A allows AMC's without Zone 3 connectors and the Guide/Key block to be inserted in shelves or carriers that have an AMC connector in the Zone 3, Connector 1 area (see MTCA1, Figure 1). The removal of PCB material in the notch area (detail A) will result in the Guide/Key block overhanging the PCB by about 0.5 mm. One should be aware that some of the AMC's original functionality could be lost in such a configuration. In addition, to be compatible with shelves and carriers that have the AMC connector in the Zone 3, Connector 1 area, other components **shall not** be in the keep out zone shown in Figure 2-1.

The area under the Guide/Key **shall** be a conductive sheet that is connected to shelf ground. The mounting holes for the Guide/Key **shall** be plated thru. The area on Component Side 2 where the Guide/Key mounts **shall not** be solder masked.

The AMC board **shall** implement the ESD strip as detailed in AMC.0, Section 2.2.1.4.

2.1.2 Zone 3 Keying

The Physics AMC modules that mate with μ RTM modules **shall** implement a keying similar in function to the K2 keying in PICMG 3.0 R3.0, Section 2.3. The Female Key receptacle is on the Physics AMC Module. The mechanical specification for the Key is in Appendix B.

2.1.2.1 Voltage keys

Physics AMC modules **shall** have the keying as N is described in Table 2-1.

Table 2-1 : Data Connector Voltage Level Keying

N	Data Signal in Volts
1	LVDS
2	0 – ± 1
3	$>\pm 1$ – ± 3.3
4	$>\pm 3.3$ – ± 10
5	$>\pm 10$
6	Reserved
7	Reserved
8	Reserved

2.1.2.2 Key Orientation

Table 2-2: Key Orientation

Value of “N”	A = Orientation in Degrees
1	0
2	45
3	90
4	135
5	180
6	225
7	270
8	315

The Orientation details can be found in Appendix B.

2.1.3 Connectors

2.1.3.1 Zone 1

The front board **should** use the add-on plug connector instead of edge card fingers. This construction technique is similar to that specified for the MCH in MTCA.0 R1.0, Section 2.11.4. The versions of these connectors that have only Tongue 1 would be used here. These connectors have tighter tolerances and better overall mechanical properties than that obtainable with edge fingers. In addition the tight constraint on the PCB thickness is relaxed.

2.1.3.2 Zone 3 ADF Connectors

Front Board ADF connectors J30 and J31 **shall** be as defined in Appendix A. This 30 pair plug **can** be used on midsize and full size modules. A 20 pair plug of the same ADF family **may** be used for applications on either compact, mid-size or full size modules. Columns E and F are not available in the 20 pair version and therefore JTAG cannot be implemented. Both the 20 and 30 pair ADF connectors are detailed in Appendix A.

The ADF J30 connector **shall** have both data, power and system management assigned to pins as shown in Table 2-3. Implementation of JTAG is optional. The corresponding pins **shall** be left unconnected if JTAG is not used. ADF connector J31 **may** be populated to afford extra data connectivity

Table 2-3: Power/Management Pin Assignments for P/J30

Row 1			Row 2		
Col	Name	Description	Col	Name	Description
A	RTM_PWR	+12 Volts	A	RTM_PWR	+12 Volts
B	RTM_PWR	+12 Volts	B	RTM_PWR	+12 Volts
Gnd	RTM_GND	Ground	Gnd	RTM_GND	Ground
C	RTM_PS#	RTM Present	C	RTM_MP	+3.3 Volts
D	RTM_SDA	I ² C Data	D	RTM_SCL	I ² C Clock
Gnd	RTM_GND	Ground	Gnd	RTM_GND	Ground
E	RTM_TCK	Optional JTAG TCK	E	JTAG_TDI	Optional JTAG TDI
F	RTM_TDO	Optional JTAG TDO	F	JTAG_TMS	Optional JTAG TMS
Gnd	RTM_GND	Ground	Gnd	RTM_GND	Ground

Table 2-4 has the pin assignments for the J30/P30 connectors. Functions in columns that are not used as shown **shall** be left unconnected. J31/P31 are entirely user-defined usage.

Table 2-4: J30/P30 Pin Assignments

Col→ Row↓	Gnd	F	E	Gnd	D	C	Gnd	B	A
10	GND[7]	F[7]	E[7]	GND[7]	D[7]	C[7]	GND[7]	B[7]	A[7]
9	GND[6]	F[6]	E[6]	GND[6]	D[6]	C[6]	GND[6]	B[6]	A[6]
8	GND[5]	F[5]	E[5]	GND[5]	D[5]	C[5]	GND[5]	B[5]	A[5]
7	GND[4]	F[4]	E[4]	GND[4]	D[4]	C[4]	GND[4]	B[4]	A[4]
6	GND[3]	F[3]	E[3]	GND[3]	D[3]	C[3]	GND[3]	B[3]	A[3]
5	GND[2]	F[2]	E[2]	GND[2]	D[2]	C[2]	GND[2]	B[2]	A[2]
4	GND[1]	F[1]	E[1]	GND[1]	D[1]	C[1]	GND[1]	B[1]	A[1]
3	GND[0]	F[0]	E[0]	GND[0]	D[0]	C[0]	GND[0]	B[0]	A[0]
2	GND	JTAG TMS	JTAG TDI	GND	SCL	MP	GND	PWR	PWR
1	GND	JTAG TDO	JTAG TCK	GND	SDA	PS#	GND	PWR	PWR

The user-defined pins are named by Row 0 to 17 (row numbers continue across J30 and J31) and Column name A to F. Each pair A/B, C/D and E/F **may** be used as a differential pair or as two individual single-ended signals. If used as a differential signal pair A, C and E **should** be used as positive/+ and B, D and F as negative/- signals. The three ground pins of a row are connected together within the ADF-plug and have the same name. All pins named 'GND' **shall not** be used for signals. Ground pins are internally connected by row.

Table 2-5: J31/P31 Pin Assignments

Col→ Row↓	Gnd	F	E	Gnd	D	C	Gnd	B	A
10	GND[17]	F[17]	E[17]	GND[17]	D[17]	C[17]	GND[17]	B[17]	A[17]
9	GND[16]	F[16]	E[16]	GND[16]	D[16]	C[16]	GND[16]	B[16]	A[16]
8	GND[15]	F[15]	E[15]	GND[15]	D[15]	C[15]	GND[15]	B[15]	A[15]
7	GND[14]	F[14]	E[14]	GND[14]	D[14]	C[14]	GND[14]	B[14]	A[14]
6	GND[13]	F[13]	E[13]	GND[13]	D[13]	C[13]	GND[13]	B[13]	A[13]
5	GND[12]	F[12]	E[12]	GND[12]	D[12]	C[12]	GND[12]	B[12]	A[12]
4	GND[11]	F[11]	E[11]	GND[11]	D[11]	C[11]	GND[11]	B[11]	A[11]
3	GND[10]	F[10]	E[10]	GND[10]	D[10]	C[10]	GND[10]	B[10]	A[10]
2	GND[9]	F[9]	E[9]	GND[9]	D[9]	C[9]	GND[9]	B[9]	A[9]
1	GND[8]	F[8]	E[8]	GND[8]	D[8]	C[8]	GND[8]	B[8]	A[8]

2.1.3.3 Zone 3 Non ADF Connectors

Sections **shall** be added under Section 2.1.3 in this position and other (if necessary) level 4 subsections. Appendix C (or following) **shall** contain all necessary mechanical details for the connector defined in these sections. A Drawing shall be inserted in this section showing the upper right hand portion of Figure 2-1 with pin 1 positions designated. Also, appropriate test dimensions shall be indicated in a drawing that is similar to Figure 2-2.

If another connector style is specified in this (or equivalent) sections it is the users responsibility that it is mechanically compatible with the shelf defined herein. The mechanical specifications should be defined so that others can manufacture AMC's and μ RTM's that will function reliably when mated.

This section may also have pin out information as required.

2.1.4 AMC Face Plate

Physics AMC Modules **shall** have a faceplate as specified in MicroTCA.1 R1.0. The Front Module Face Plate **shall** have a latch and retention device as defined in PICMG Rugged MicroTCA.1 R1.0, Section 2.5. See also PICMG Rugged MicroTCA.1 R1.0, Appendix B for implementations of the retention device.

2.1.5 AMC Test Dimensions

The test dimension for the depth of the assembly is the same as that in PICMG Rugged MicroTCA.1 R1.0. The projection of the Zone 3 connector mating face beyond Datum J is an added dimension. The test dimensions from Datum L are to the edge of the connector housing.

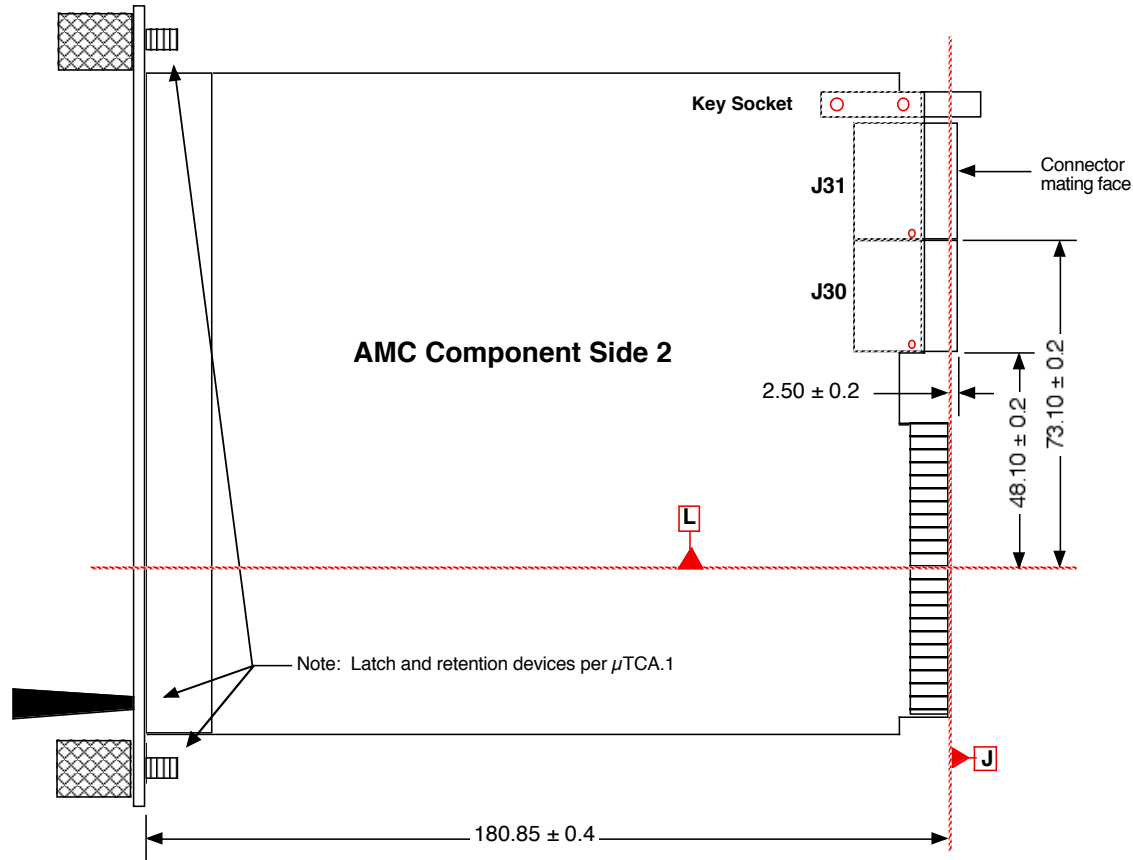


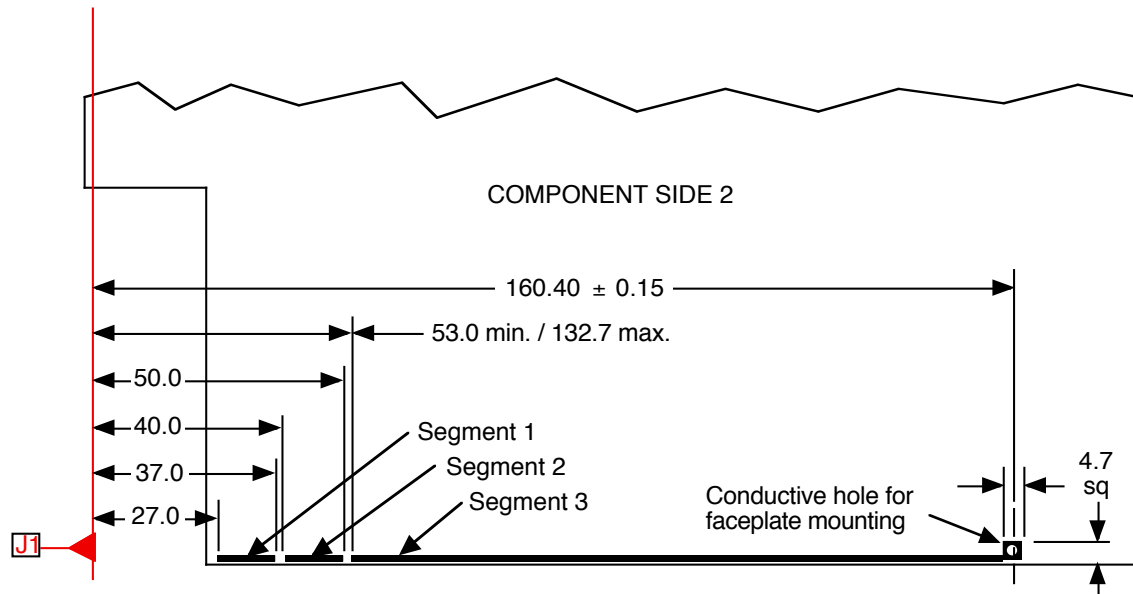
Figure 2-2: Physics AMC Module Test Dimensions

2.2 Physics μ RTM

The construction of the μ RTM is similar to the AMC in AMC.0 R2.0. The panel and other hardware **shall** be rotated 180° about an axis perpendicular to the PCB so as to be compatible with existing hardware. This rotation places the latch in the upper left of the μ RTM module. Other hardware is similarly repositioned. All positions are viewed from side two of the PCB.

2.2.1 Printed Circuit Board

The μ RTM is similar to the AMC front board in size. Figure 2-3 shows the board outline and the location of the Zone 3 connectors and the male alignment/key pin. As in the AMC specification there are reserved areas for hot swap switch, faceplate mounting hardware, and ESD zone along the top and bottom edge.



2.2.2 Zone 3 Keying

The area under the Guide/Key **shall** be a sheet that is connected to shelf ground. The mounting holes for the Guide/Key **shall** be plated thru. The area on Component Side 2 where the Guide/Key mounts **shall not** be solder masked.

See this document [Section 2.1.2](#) and Appendix B for other Key Information.

2.2.3 Zone 3 Connectors

2.2.3.1 ADF Connectors

The μ RTMs **shall** position the Zone 3 ADF connector(s) according to the pin 1 location for each connector as shown in Figure 2-3. The mounting hole pattern on the μ RTM **shall** be as shown in Appendix A.

2.2.3.2 Non ADF Connectors

Sections **shall** be added under Section 2.2.3 in this position and other (if necessary) level 4 subsections. Appendix C (or following) **shall** contain all necessary mechanical details for the connector defined in these sections. A Drawing shall be inserted in this section showing the upper left hand portion of Figure 2-3 with pin 1 positions designated. Also, appropriate test dimensions shall be indicated in a drawing that is similar to Figure 2-4.

2.2.4 μ RTM Face Plate

Physics μ RTM Modules **shall** have a faceplate as specified in MicroTCA.1 R1.0. The μ RTM Face Plate **shall** have a latch and retention device as defined in PICMG Rugged MicroTCA.1 R1.0, Section 2.5. See also PICMG Rugged MicroTCA.1 R1.0, Appendix B for implementations of the retention device. The hardware is the same as for the AMC, however, the mounting is reversed top to bottom.

2.2.5 μ RTM Test Dimensions

Modules that conform to this specification **shall** meet the test dimensions in Figure 2-4. The test dimensions from Datum L1 are to the edge of the connector housing.

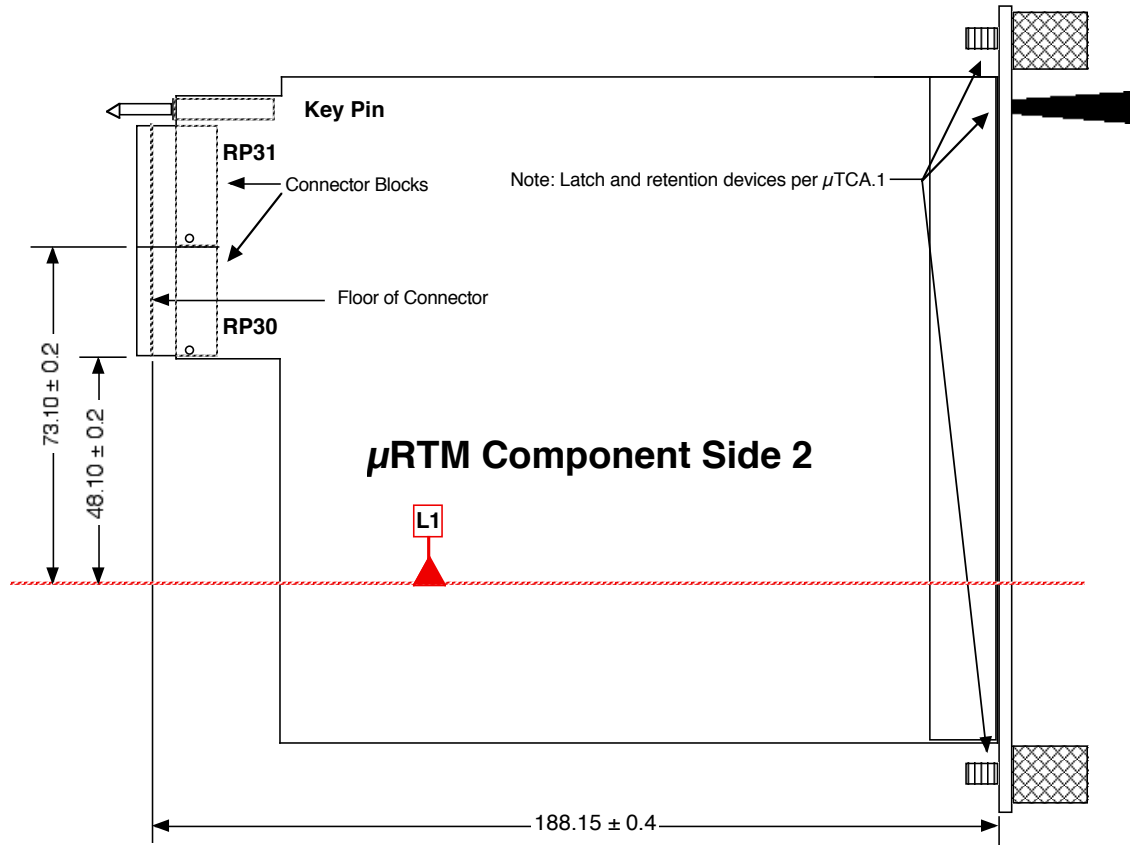


Figure 2-4: Physics μ RTM Module Test Dimensions

2.3 Physics μ TCA Shelf

In the broadest sense one can think of the Physics μ TCA shelf as two shelves mated back-to-back. Obviously there is more to the shelf but this gives the user a way of viewing this section of the document.

2.3.1 Shelf Dimensions

The shelf specification follows the MTCA.0 R1.0 specification. The AMC modules and the front part of the shelf are fully compatible with the Double-Width modules of this specification. The rear of the shelf accommodates μ RTM modules specified in this document.

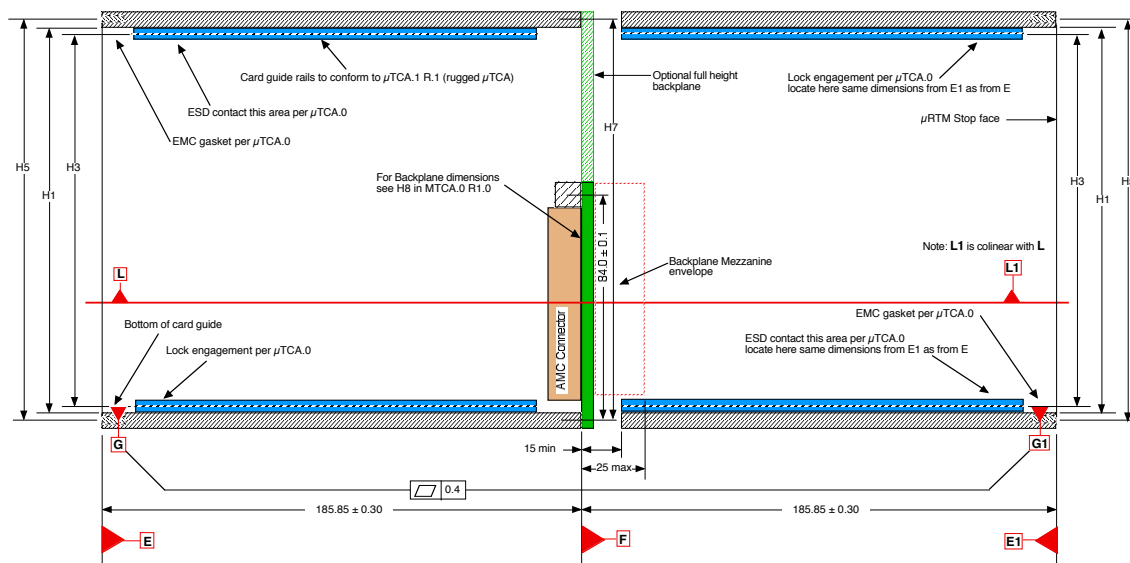


Figure 2-5 : Side view of Shelf

For missing dimensions see MTCA.0, Section 2. This side view drawing **shall** serve as the bases for designing the Physics μ TCA shelf. Other manifestations of the shelf such as Pico, half width rack mounted, *etc* **shall** conform to these dimensions. Shelves that have the modules mounted horizontally rather than vertically have certain constraints imposed by the module retention requirements. Such shelves are not described in this document and may prove difficult to manufacture. The backplane printed circuit board thickness **should** be 5 mm

2.3.2 Insertion of Front and Rear Boards

When initially configuring modules in the μ TCA shelf the following sequence **shall** be followed.

1. Insert the Front AMC Module of the AMC/ μ RTM pair
2. Fasten the retention device on the AMC panel to the shelf
3. Insert μ RTM
4. Fasten the retention device on the μ RTM panel to the shelf

After the initial placement of the front and rear boards one or the other may be removed as necessary. If both boards are removed then the initial insertion sequence **shall** be repeated.

2.3.3 Shelf Test Dimensions

Shelves that conform to this specification **shall** meet the test dimensions in Figure 2-6.

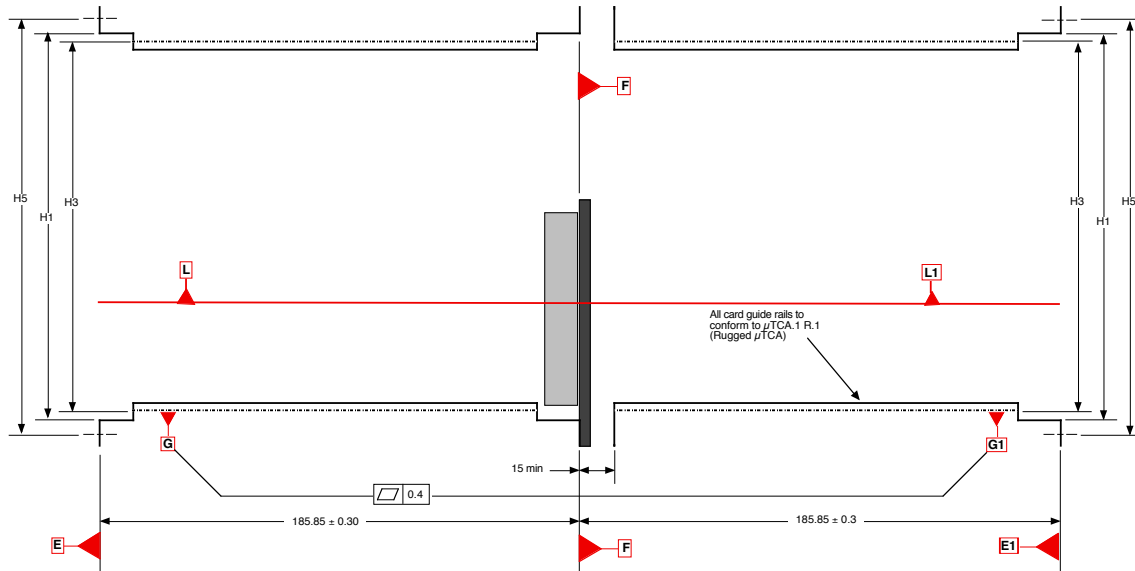


Figure 2-6: Test Dimensions for Shelf

Datum's L and L1 are collinear. For location of Datum L see MTCA.0, R1.0, Figure 2-29. The dimensions H1, H3 and H5 are defined in MTCA.0, R1.0, Section 2.7.1.

2.3.4 Shelf Cooling

2.3.4.1 Airflow Balancing

Empty slots in the front and rear of the shelf **shall** have airflow balancing plates on the filler modules to distribute the cooling more evenly that if they were left open. AMC and μ RTM modules that do not block at least 80% of the Zone 3 area **shall** implement a mechanism that meets this requirement.

2.3.4.1.1 AMC Modules

AMC Modules **shall** have either connectors and keys or an airflow blocking mechanism in the Zone 3 area to control the flow of cooling air through the front of the shelf to meet the requirement in [Section 2.3.4.1](#).

2.3.4.1.2 AMC Filler Modules

AMC filler modules **shall** conform to PICMG Rugged MicroTCA.1 R1.0, Section 5.4.

2.3.4.1.3 μ RTM Modules

μ RTM Modules **shall** have either connectors and keys or an air-flow blocking mechanism in the Zone 3 area to control the flow of cooling air through the rear of the shelf to meet the requirement in [Section 2.3.4.1](#) above.

2.3.4.1.4 μ RTM Filler Modules

These modules **shall** be similar to the AMC filler modules described in MicroTCA.1 R1.0. The preferred solution is to have a movable horizontal vane. The Zone 3 area **shall** have an airflow blocking mechanism that fills a minimum of 80% of the area between the front and rear. The size of connectors used and guide/key can fulfill this requirement.

2.3.4.1.5 Shelf

The cooling requirements are similar to PICMG Rugged MicroTCA.1 R1.0. In the Physics μ TCA shelf there is also the rear μ RTM area to cool. The cooling air supply **shall** meet the specifications in the MicroTCA.0 and MicroTCA.1.

The monitoring of cooling for the shelf **shall** be integrated into the system management system.

2.3.5 Module heights for shelves

Shelves can be constructed for any module height or mixture of various heights. Compact modules can only have the 2-row ADF connector in Zone 3. Midsize modules can have either the 2 or 3 row ADF connector in Zone 3. Full size modules can either 2, 3 or 4 row ADF connectors. Modules without Zone 3 connectors, if used, **shall** have a μ RTM filler module inserted in the rear of these units to block air flowing between the front and rear of the shelf.

It should be noted that there could be a slight interference between the adjacent modules gasket and the connector when inserting either the AMC or the μ RTM. This interference only occurs as the inserted module passes the adjacent front panel and does not impact the other hardware on either board. This has not been deemed to be a problem and should not prevent the use as stated.

2.3.6 Zone 3 Backplane

The shelf and Physics AMC module is defined such that a backplane could be placed in Zone 3 without modifying the AMC module. If a μ RTM were also used with the Zone 3 backplane it would have to be modified.

This specification does not detail either the backplane or the μ RTM that would be compatible with such a backplane.

3 Management

3.1 Overview

MicroTCA.4 systems extend the functionality of the MicroTCA.0 specification. This section defines the hardware platform management extensions required by MicroTCA.4 systems. The requirements from AMC.0 and MicroTCA.0 apply to MicroTCA.4 systems unless explicitly superseded by this specification.

3.2 μ RTM Management Hardware

AMCs designed for MicroTCA.4 systems support a μ RTM via Zone 3 connectors (see [Section 2.2.3](#)). The μ RTM is managed by the MMC of the front AMC board. In order to manage a mismatched μ RTM, a standardized management interface between the AMC and the μ RTM is required.

The management interface between the AMC and the μ RTM includes the following:

- Ground
- PS#
- Management Power (MP)
- I²C bus
- Payload Power (PWR)

In addition to the signals through the Zone 3 Interface, there are additional hardware requirements for the AMC and the μ RTM.

Figure 3-1 shows a block diagram of the basic AMC and μ RTM management hardware.

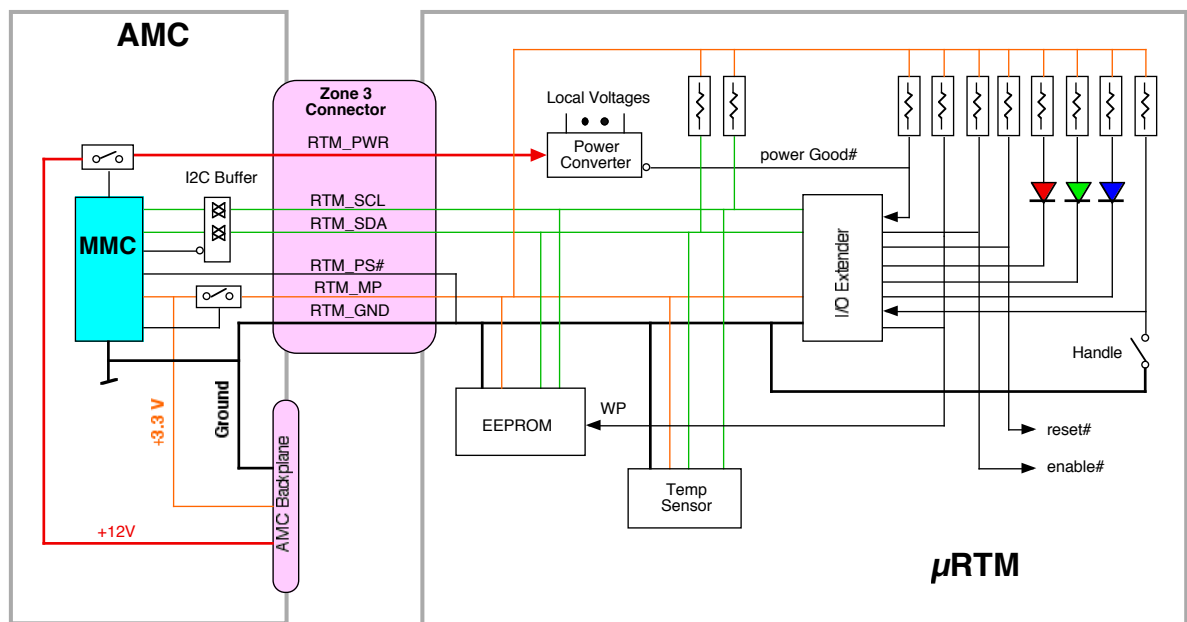


Figure 3-1: AMC/ μ RTM Management Block Diagram

3.2.1 PS#

The PS# signal is used to detect the presence of a μ RTM.

The Front AMC **shall** pull-up PS# to management power.

The μ RTM **shall** connect PS# to ground.

The Front AMC's MMC **shall** monitor the PS# signal. If the Zone 3 connectors do not guarantee PS# to be a last mate contact, the MMC design **should** take precautions to ensure the μ RTM is fully mated before considering the μ RTM as present. These precautions are design specific and are beyond the scope of this specification.

3.2.2 Management Power

Management Power (MP) is delivered to the μ RTM through the Front AMC. The Front AMC's MMC **should** gate MP to the μ RTM.

3.2.3 I²C Bus

The MMC **shall** provide an I²C bus for connection to devices on the μ RTM. The AMC **should** provide a bi-directional buffer such as an LTC4307 or equivalent be used to isolate the μ RTM I²C bus from the AMC's I²C bus.

The μ RTM **shall** provide an AT24C32A-compatible serial EEPROM that contains the Platform Management FRU information of the RTM. This EEPROM **shall** be connected to the Front AMC MMC's I²C port. The address of the EEPROM **shall** be 50h. If a larger EEPROM is needed, devices up to 24C512 may be used, as they are software compatible with the 24C32.

The μ RTM **shall** provide a PCF8574A-compatible I/O extender as an interface to the hot swap handle and LED's on the faceplate of μ RTM. The I/O extender **shall** be connected to the Front AMC MMC's I²C port. The address of the I/O extender **shall** be 3Eh.

The I/O extender is used to detect the hot swap handle position and to drive three LED's. Further, one I/O line is used to enable the writing of updates into the EEPROM by the MMC. The remaining I/O lines **may** be used for signaling a "power ok" state of the μ RTM, generating a reset and an enable signal to the μ RTM. The latter three signals are application specific. Table 3-1 lists the allocation of I/O pins.

Table 3-1: I/O pin assignment of the I/O extender

Pin	Description
P0	Hot Swap Handle 0 = Handle Closed 1 = Handle Open
P1	Blue LED 0 = On 1 = Off
P2	LED1 Red 0 = On 1 = Off
P3	LED2 Green 0 = On 1 = Off
P4	μ RTM Power Good# (Optional) 0 = Power Good 1 = Not Power Good
P5	μ RTM Reset# (Optional) 0 = Reset# Asserted 1 = Reset# Not Asserted
P6	μ RTM Enable# (Optional) 0 = Enabled 1 = Disabled
P7	EEPROM Write Protect (Optional / Reserved) 0 = Write Enabled 1 = Write Protected

P0 to P3 **shall** be used for the indicated purpose defined in Table 3-1. P0 “Hot Swap Handle” allows the MMC to determine if the hot swap handle is opened or closed. P1 “Blue LED” allows the MMC to control the state of the Blue LED on the μ RTM’s faceplate. P2 “LED1 Red” allows the MMC to control the state of the red element for the μ RTM’s LED1. P3 “LED2 Green” allows the MMC to control the state of the green element for the μ RTM’s LED2.

P4 to P6 **should** be used as indicated in the Table 3-1. The implementations of P4 to P6 are μ RTM specific and are not applicable to all μ RTM designs. P4 “ μ RTM power good” is an indication to the MMC that the power on the μ RTM is in a good condition. P5 “ μ RTM Reset” allows the MMC to reset circuitry on the μ RTM. P6 “ μ RTM Enable” is used to control any necessary isolators and/or output enables on the μ RTM.

P7 **should** be used as indicated in Table 3-1, and **shall not** be used for any other purpose. P7 “EEPROM Write Enable” allows write protection control for the μ RTM’s EEPROM.

The AMC and μ RTM **may** implement additional devices on the I²C bus, however, the AMC and μ RTM designer needs to be cautious about the I²C bus specification. Although SMBus is very similar to I²C, there are minor differences. Some SMBus devices might appear to work, but might occasionally cause errors. I²C compatibility is required.

3.2.4 Payload Power

Payload power is delivered to the μ RTM through the Front AMC. The Front AMC’s MMC **shall** gate Payload Power to the μ RTM. The MMC **shall** only enable Payload Power to the μ RTM as defined in [Section 3.5](#).

Payload Power is delivered to the μ RTM as 12V. If a μ RTM requires other voltages, the μ RTM **shall** provide any necessary voltage conversion circuitry.

3.2.5 μ RTM Temperature Sensor

The μ RTM **shall** provide at least one temperature sensor readable by the Front AMC’s MMC. The temperature sensor **should** monitor the most temperature critical component on the μ RTM. The temperature sensor **may** be connected to the I²C bus or **may** be connected using user I/O.

3.3 FRU Device IDs

The AMC.0 specification requires AMCs to implement a single FRU device ID of 0. Because the μ RTM needs to be managed as an independent FRU, this specification requires the MMC to implement two specific FRU device IDs. The MMC **shall** implement FRU Device ID 0 to represent the Front AMC. In MicroTCA.4 environments, the MMC **shall** implement FRU Device ID 1 to represent its μ RTM. In response to a Get PICMG Properties command, the MMC **shall** report a *Max FRU Device ID* of 1.

The MMC **shall** provide a FRU Device Locator record in its SDRs for the μ RTM. This FRU Device Locator record **shall** report the μ RTM as having an Entity ID of PICMG Rear Transition Module (COh). The MMC **shall** implement the Get Device Locator Record ID command as defined in the AMC.0 specification.

The Carrier Manager **shall** map each AMC’s FRU Device ID 0 (Front AMC) to Carrier Manager relative FRU Device IDs 5-39 as defined in MicroTCA.0. The Carrier Manager **shall** map each AMC’s FRU Device ID 1 (μ RTM) to Carrier Manager relative FRU Device IDs 90-124.

3.4 MicroTCA Carrier Information

The MicroTCA Carrier Information record includes a list of Slot Entries for each FRU in the MicroTCA Carrier. Each Slot entry specifies the Site Type and Site Number as well as physical location coordinates.

Slot Entries corresponding to μ RTMs **shall** have their *Site Type* field set to a value of 09h

(Rear Transition Module as defined in the PICMG 3.0 specification). Slot Entries corresponding to μ RTMs **shall** have their *Site Number*, *Origin X*, and *Origin Y* fields set to the same values as the respective fields in the associated Front AMC's Slot Entry.

3.5 Operational State Management

Hot swap of μ RTMs is handled very similarly to hot swap of AMCs. The Front AMC's MMC implements two Module Hot Swap sensors, one for the Front AMC and one for the μ RTM. The Carrier Manager implements FRU Hot Swap sensors for each Front AMC and each μ RTM. Additionally, the Carrier Manager maps a FRU ID to the μ RTMs, maps sensors to μ RTM sensors, *etc.*

The following sections provide more details about operational state management for μ RTMs.

3.5.1 Typical μ RTM Insertion Process

- 1) The μ RTM is inserted and PS# is asserted.
- 2) When the MMC detects PS# asserted by the μ RTM, it enables MP to the μ RTM and the μ RTM's management circuitry is powered.
- 3) The MMC sets the μ RTM's Blue LED to On
- 4) The MMC enables the Module Hot Swap sensor associated with the μ RTM, and generates a Module Hot Swap sensor (RTM Present) event.
- 5) The Carrier Manager changes the Hot Swap state for the μ RTM from M0 to M1.
- 6) The MMC performs a compatibility check as described in [Section 3.5.3 Compatibility Check](#).
- 7) If the μ RTM was determined to be compatible with the Front AMC, the MMC enables the remaining sensors associated with the μ RTM.
- 8) The MMC generates a Module Hot Swap sensor (μ RTM Compatible or μ RTM Incompatible) event.
- 9) The Carrier Manager creates local sensors that map to each sensor associated with the μ RTM.
- 10) The user closes the μ RTM hot swap handle.
- 11) When the MMC detects the μ RTM's hot swap handle is closed, by polling the Hot Swap Handle bit in the μ RTM's I²C I/O extender, it generates a Module Hot Swap sensor (Handle Closed) event from the Module Hot Swap sensor associated with the μ RTM.
- 12) The Carrier Manager changes the Hot Swap state for the μ RTM from M1 to M2 and sends a Set FRU LED (Blue LED Long Blink) command to the MMC for FRU ID 1.
- 13) The MMC starts blinking the μ RTM's Blue LED accordingly by periodically changing the state of the Blue LED bit in the μ RTM's I²C I/O extender.

- 14) The Carrier Manager, Shelf Manager or System Manager sends a Set FRU Activation (Activate) command to the Carrier Manager.
- 15) The Carrier Manager changes the Hot Swap state for the μ RTM from M2 to M3.
- 16) The Carrier Manager sends a Set Power Level (Level=1) command to the MMC for FRU ID 1.
- 17) If the μ RTM was determined to be compatible, the MMC enables payload power to the μ RTM.
- 18) The Carrier Manager changes the Hot Swap state for the μ RTM from M3 to M4.
- 19) If the μ RTM was determined to be compatible, the MMC enables the μ RTM and AMC Zone 3 Interfaces by clearing the μ RTM Enable# bit in the μ RTM's I²C I/O extender.
- 20) The Carrier Manager sends a Set FRU LED (Blue LED Off) command to the MMC for FRU ID 1.
- 21) The MMC turns off the μ RTM's Blue LED by setting the Blue LED bit in the μ RTM's I²C I/O extender.

3.5.2 Typical μ RTM Extraction Process

- 1) The user opens the μ RTM hot swap handle
- 2) When the MMC detects the μ RTM's hot swap handle is open by polling the Hot Swap Handle bit in the μ RTM's I²C I/O extender, it generates a Module Hot Swap sensor (Handle Open) event from the Module Hot Swap sensor associated with the μ RTM.
- 3) The Carrier Manager changes the Hot Swap state for the μ RTM from M4 to M5 and sends a Set FRU LED (Blue LED Short Blink) command to the MMC for FRU ID 1.
- 4) The MMC starts blinking the Blue LED accordingly by periodically changing the state of the Blue LED bit in the μ RTM's I²C I/O extender.
- 5) The System Manager, Shelf Manager or Carrier Manager sends a Set FRU Activation (Deactivate) command to the Carrier Manager
- 6) The Carrier Manager changes the Hot Swap state for the μ RTM from M5 to M6 and sends the FRU Control (Quiesce) command to the MMC for FRU ID 1.
- 7) The MMC takes any design specific action to quiesce the Zone 3 Interface. Refer to [Section 3.5.7 Quiesce Actions](#) for more details.
- 8) The MMC disables the μ RTM and AMC Zone 3 Interfaces by setting the μ RTM Enable# bit in the μ RTM's I²C I/O extender, and generates a Module Hot Swap sensor (Quiesced) event from the Module Hot Swap sensor associated with the μ RTM.

- 9) The Carrier Manager sends a Set Power Level (Level=0) command to the MMC for FRU ID 1.
- 10) The MMC disables payload power to the μ RTM.
- 11) The Carrier Manager changes the Hot Swap state from M6 to M1, and sends a Set FRU LED (Blue LED On) command to the MMC for FRU ID 1.
- 12) The MMC turns on the μ RTM's Blue LED by clearing the Blue LED bit in the μ RTM's I²C I/O extender.
- 13) The user extracts the μ RTM.
- 14) When the MMC detects PS# is de-asserted, the MMC disables all the sensors associated with the μ RTM except the Module Hot Swap sensor, disables the μ RTM's MP, generates a Module Hot Swap sensor (RTM Absent) event, and then disables the Module Hot Swap sensor associated with the μ RTM.
- 15) The Carrier Manager changes the Hot Swap state for the μ RTM from M1 to M0 and deletes all local sensors associated with the μ RTM.

3.5.3 FRU Hot Swap and Module Hot Swap Sensors

The Carrier Manager manages the hot swap state for μ RTMs similarly to how it manages the hot swap state for AMCs. The Carrier Manager **shall** implement a FRU Hot Swap sensor as defined in the PICMG 3.0 specification for each μ RTM.

μ RTMs are hosted by the MMC on the Front AMC. The MMC **shall** implement a Module Hot Swap sensor for the μ RTM in addition to the Module Hot Swap sensor for the AMC. The Module Hot Swap sensor associated with the μ RTM **shall** generate events as defined in Table 3-2. The Module Hot Swap sensor associated with the μ RTM **shall** respond to Get Sensor Reading commands as defined in Table 3-3.

Table 3-2: Module Hot Swap Event Message

Data Type	Byte	Data Field
Request Data	1	<i>Event Message Rev</i> = 04h (IPMI specification)
	2	<i>Sensor Type</i> – F2h (Module Hot Swap)
	3	<i>Sensor Number</i> = xxh (Implementation specific)
	4	<i>Event Direction (bit 7)</i> = 0b (Assertion) Event Type [6:0] = 6Fh (Generic Availability)
	5	Event Data 1 [7:4] = 00h (unspecified Event Data 2 and 3) [3:0] = Current Event 0 = Module Handle Closed 1 = Module Handle Opened 2 = Quiesced 3 = Backend Power Failure 4 = Backend Power Shut Down 5 = μ RTM Present ¹ 6 = μ RTM Absent ¹ 7 = μ RTM Compatible ¹ 8 = μ RTM Incompatible ¹ 9-Fh = Reserved
	6	<i>Event Data 2</i> = FFh or not present
	7	<i>Event Data 3</i> = FFh or not present
Response Data	1	<i>Completion Code</i>

¹ Only applicable to Module Hot Swap sensors associated with μ RTMs. For Module Hot Swap sensors associated with other Module types, write as 0b and ignore on read.

Table 3-3: Get Sensor Reading (Module Hot Swap sensor)

Data Type	Byte	Data Field
Request Data	1	<i>Sensor Number</i> (FFh = reserved)
Response Data	1	<i>Completion Code</i>
	2	<i>Sensor Reading</i> [7:0] Not Used. Write as 00h.
	3	<i>Standard IPMI byte</i> (See “Get Sensor Reading” in the IPMI specification): [7] – 0b = All Event Messages disabled from this sensor [6] – 0b = Sensor scanning disabled [5] – 1b = Initial update in progress. This bit is set to indicate that a “Re-Arm Sensor Events” or “Set Event Receiver” command has been used to request an update of the sensor status, and that update has not occurred yet. Software should use this bit to avoid getting an incorrect status while the first sensor update is in progress. This bit is only required if it is possible for the MMC to receive and process a “Get Sensor Reading” or “Get Sensor Event Status” command for the sensor before the update has completed. This is most likely to be the case for sensors, such as fan RPM sensors, that may require seconds to accumulate the first reading after a re-arm. [4:0] Reserved. Ignore on read.
	4	<i>Current State Mask</i> [7] – 1b = μ RTM Compatible ¹ [6] – 1b = μ RTM Absent ¹ [5] – 1b = μ RTM Present ¹ [4] – 1b = Backend Power Shut Down [3] – 1b = Backend Power Failure [2] – 1b = Quiesced [1] – 1b = Module Handle Opened [0] – 1b = Module Handle Closed
	(5) ²	[7] – Reserved. Write as 1b. Ignore on read. [6:1] – Reserved. Write as 0b. Ignore on read. [0] – 1b = μ RTM Incompatible ¹

¹ Only applicable to Module Hot Swap sensors associated with μ RTMs. For Module Hot Swap sensors associated with other Module types, write as 0b and ignore on read.

² Required for Module Hot Swap sensors associated with μ RTMs. This is optional for all other Module types.

The Front AMC's MMC **shall** enable and disable the Module Hot Swap sensor associated with the μ RTM as defined in [Section 3.5.6](#) Sensor Management. When the MMC detects that the μ RTM is present, after enabling the Module Hot Swap sensor associated with the μ RTM, the MMC **shall** generate a Module Hot Swap (μ RTM Present) event from the Module Hot Swap sensor associated with the μ RTM. When the MMC detects that the μ RTM is no longer present, before disabling the Module Hot Swap sensor associated with the μ RTM, the MMC **shall** generate a Module Hot Swap (μ RTM Absent) event from the Module Hot Swap sensor associated with the μ RTM.

The MMC **shall** support μ RTM Compatible and μ RTM Incompatible states and events as defined in [Section 3.5.5](#) Compatibility Check.

The MMC **shall** support other Module Hot Swap sensor states and events as defined in the AMC.0 specification.

3.5.4 FRU Activation and Deactivation

The MicroTCA Carrier Activation and Current Descriptor record includes a MicroTCA Carrier Activation and Current Descriptor for each FRU connected to a Power Channel. The MicroTCA Carrier Activation and Current Descriptor specifies the current limitations of the Power Channel and whether the System Manager, Shelf Manager or Carrier Manager is responsible for activating and deactivation the corresponding FRU.

μ RTMs **shall** be listed in the MicroTCA Carrier Activation and Current Descriptor record. MicroTCA Carrier Activation and Current Descriptors corresponding to μ RTMs **shall** have their *Site Type* field set to a value of 09h (Rear Transition Module as defined in the PICMG 3.0 specification). Because μ RTMs do not directly connect to Power Channels, MicroTCA Carrier Activation and Current Descriptors corresponding to μ RTMs **shall** have their *Power Channel* and *Maximum Channel Current* fields set to 0. Each MicroTCA Carrier Activation and Current Descriptor corresponding to a μ RTM **shall** be listed after the associated Front AMC's MicroTCA Carrier Activation and Current Descriptor in the MicroTCA Carrier Activation and Current Descriptor record.

It should be noted that μ RTMs receive their power via the Front AMC. If a Front AMC is deactivated, its Payload Power will be disabled; in this case, the μ RTM connected to that AMC will also have its Payload Power disabled. A System Manager, Shelf Manager, or Carrier Manager **may** implement an activation/deactivation policy that activates Front AMCs prior to μ RTMs and deactivates μ RTMs prior to Front AMCs.

3.5.5 Compatibility Check

The Zone 3 Interface connecting the Front AMC and the μ RTM has a few standardized pins for basic management, but most of the pins are user defined. In order to help prevent damage if an AMC is connected to an incompatible μ RTM, a compatibility check is performed to determine if the AMC and μ RTM are compatible with each other.

The result of the compatibility check is reported via the μ RTM Compatible and μ RTM Incompatible state bits in the Module Hot Swap sensor. Additionally, the Front AMC's

MMC will only enable Payload Power and clear the μ RTM Enable# bit in the μ RTM's I²C I/O extender if the AMC and μ RTM are determined to be compatible.

The MMC performs the compatibility check by reading Zone 3 Interface Compatibility records from the AMC's FRU information and from the μ RTM's FRU information. If matching records are found, the AMC and μ RTM are considered as compatible. If matching records are not found, then the AMC and μ RTM are considered incompatible.

The Zone 3 Interface Compatibility record is defined in the PICMG IRTM.0 specification.

[Note: Because the IRTM.0 specification is currently not ratified, and therefore not generally available, the Zone 3 Interface Compatibility record is duplicated here. Once the IRTM.0 specification is ratified, this record should be removed from this specification to avoid inconsistencies. Also, because the IRTM.0 specification is not ratified, this record is subject to change.]

Table 3-4: Zone 3 Interface Compatibility record

Offset	Length	Field description
0	1	<i>Record Type ID</i> . Value C0h (OEM).
1	1	[7:7] End of list. Set to one for the last record. [6:4] Reserved, write as 0h. [3:0] Record format version (=2h for this definition).
2	1	<i>Record Length</i> .
3	1	<i>Record Checksum</i> . Holds the zero checksum of the record.
4	1	<i>Header Checksum</i> . Holds the zero checksum of the header.
5	3	<i>Manufacturer ID</i> . For this specification 12634 (0x00315A, LSB first) shall be used
8	1	<i>PICMG Record ID</i> . The value XXh (should be same as in IRTM spec) shall be used for this definition.
9	1	<i>Record Format Version</i> . For this specification, 0h shall be used.
10	1	<i>Type of Interface Identifier</i> : 0h = PICMG IRTM.0 REP Number 1h = Other PICMG specification-defined interface identifier 2h = Interface Identifier GUID 3h = OEM interface identifier 4h-FFh = Reserved
11	N	<i>Interface Identifier Body</i> (format depends on the type), terminated by the end of record.

An Interface identifier body of type 0 (PICMG IRTM.0 REP Number) is not applicable for an AMC/ μ RTM because μ RTMs are explicitly not IRTM.0 compliant. The PICMG IRTM.0 REP Number format is listed here only for completeness.

Table 3-5: PICMG IRTM.0 REP Number

Offset	Length	Field description
11	4	The IRTM.0 REP number, 32 bits, LS byte first

An Interface identifier body of type 1 (Other PICMG specification-defined interface identifier) has the following format:

Table 3-6: Other PICMG Specification-defined Interface Identifier

Offset	Length	Field description
11	4	The PICMG specification unique identifier, LS byte first (format TBD)
15	1	The PICMG specification major revision number
16	1	The PICMG specification minor revision number
17	M	The opaque interface identifier body

The interface Identifier Body of type 2 (Interface identifier GUID) has the following format:

Table 3-7: Interface identifier GUID

Offset	Length	Field description
11	16	Interface identifier GUID, LS byte first. Globally Unique Identifier generated in accordance with AMC.0.

An Interface Identifier Body of type 3 (OEM interface identifier) has the following format:

Table 3-8: Interface identifier OEM

Offset	Length	Field description
11	3	Manufacturer ID (IANA) of the OEM that owns the definition of this interface. LS Byte first.
14	4	OEM-defined interface designator, 32 bits, LS byte first

AMCs and μ RTMs **shall** provide at least one Zone 3 Interface Compatibility record in their FRU information.

When the MMC detects a μ RTM is present, the MMC **shall** perform a compatibility check. If any Zone 3 Interface Compatibility record in the μ RTM's FRU information matches any Zone 3 Interface Compatibility record in the AMC's FRU information, the AMC and μ RTM **shall** be considered compatible, otherwise the AMC and μ RTM **shall** be considered incompatible. Zone 3 Interface compatibility records **shall** be considered as matching if the records are the same length and are identical from Offset 9 through the end of the records, otherwise, the records **shall** be considered as not matching.

After performing the compatibility check, the MMC **shall** generate a Module Hot Swap sensor event indicating the result of the compatibility check.

3.5.6 Sensor Management

μ RTM sensors are dynamically populated or depopulated on the MMC when the μ RTM is detected as present or absent. Similarly, the Carrier Manager dynamically populates and depopulates local sensor mapped to the μ RTM sensors are μ RTM presence or absence is reported via the Module Hot Swap sensor events.

When the Front AMC's MMC detects that a μ RTM is present, the MMC **shall** enable the Module Hot Swap sensor for the μ RTM. When the MMC determines that the μ RTM is compatible with the Front AMC, the MMC **shall** enable any additional μ RTM sensors. When the MMC detects that the μ RTM is no longer present it **shall** disable all μ RTM sensors except for the Module Hot Swap sensor associated with the μ RTM. The MMC **shall** disable the Module Hot Swap sensor associated with the μ RTM after generating the Module Hot Swap (μ RTM Absent) event.

The MMC **shall** provide an SDR for the Module Hot Swap sensor associated with the μ RTM. This allows the MMC to provide a Module Hot Swap sensor the μ RTM regardless of the result of the compatibility check. Although it is likely that the MMC also provides the SDRs for other μ RTM sensors, the exact implementation of μ RTM sensor SDRs is design-specific and is beyond the scope of this specification.

The SDRs for sensors associated with the μ RTM **shall** use the PICMG Rear Transition Module entity ID COh and the AMC's site number + 60h as a device-relative entity instance number.

3.5.7 Quiesce Actions

When the Front AMC's MMC receives a FRU Control (Quiesce) command with FRU Device ID set to 1, the MMC **shall** take appropriate action (implementation specific) to bring the Zone 3 interface to a quiesced state and generate a Module Hot Swap (Quiesced) event from the Module Hot Swap sensor associated with the μ RTM.

If the μ RTM is determined to be compatible and the μ RTM supports the μ RTM Enable# bit in the μ RTM's I2C I/O extender, the MMC **shall** set the μ RTM Enable# bit after the Zone 3 Interface is quiesced, but before generating the Module Hot Swap sensor (Quiesced) event.

Because the Zone 3 Interface is mostly user defined pins, the actions needed to quiesce the Zone 3 Interface can vary greatly from one design to another. In the simplest cases, there might not be any action required. In other cases some or all of the user defined pins may need to be isolated, and in some cases, all or part of the Front AMC might even need to be powered off under MMC control. The specific actions needed are design specific and are beyond the scope of this specification.

3.6 Power Management

The Front AMC's Module Current Requirements record **shall** include the power required for any compatible μ RTM.

If a μ RTM is determined to be incompatible, the MMC **shall not** enable Payload Power to the μ RTM.

If a μ RTM is determined to be compatible, upon receipt of a Set Power Level (Level = 1) command, the MMC **shall** enable Payload Power to the μ RTM. If the μ RTM supports the μ RTM Enable# bit in the I²C I/O extender, the MMC **shall** clear the μ RTM Enable# bit after enabling Payload Power to the μ RTM.

Upon receipt of a Set Power Level (Level = 0) command, the MMC **shall** disable Payload Power to the μ RTM. The μ RTM Enable# bit is set as part of the quiesce actions as defined in [Section 3.5.7](#).

3.7 Cooling Management

Because μ RTMs have Carrier Manager FRU Device IDs, they **may** be listed as cooled FRUs in MicroTCA Fan Geography records.

3.8 E-Keying

Physics applications require special clock, trigger, and interlock connections between modules. For this reason, they use special backplanes with specific connections on AMC ports 12 through 15 and 17 through 20.

Ports 12 through 15 are routed using point-to-point links and **shall** be E-Keyed using the standard E-Keying mechanisms defined in the AMC.0 specification. However, physics applications are likely to use custom protocols on ports 12 through 15. When using custom protocols, the corresponding Link Descriptors **shall** specify *Link Type* values of F0h – FEh (E-Keying OEM GUID definition as defined in the PICMG AMC.0 specification).

Ports 17 through 20 are routed in a multidrop bus topology. This is incompatible with point-to-point E-Keying. A Carrier Based Connectivity record in the Carrier FRU information describes the bused connections.

Table 3-9: Carrier Based Connectivity Record

Offset	Length	Field description
0	1	<i>Record Type ID</i> . Value C0h (OEM).
1	1	[7:7] End of list. Set to one for the last record. [6:4] Reserved, write as 0h. [3:0] Record format version (=2h for this definition).
2	1	<i>Record Length</i> .
3	1	<i>Record Checksum</i> . Holds the zero checksum of the record.
4	1	<i>Header Checksum</i> . Holds the zero checksum of the header.
5	3	<i>Manufacturer ID</i> . For this specification 12634 (0x00315A, LSB first) shall be used
8	1	<i>PICMG Record ID</i> . The value TBD shall be used for this definition.
9	1	<i>Record Format Version</i> . For this specification, the value 0h shall be used.
10	1	<i>Bused Connection Count</i> . Number of Bused Connection Descriptors (N) that follow.
11	Variable	<i>Bused Connection Descriptors</i> . This is a list of Bused Connection Descriptors. Each entry shall be formatted as defined in Table 3-6.

The Carrier Based Connectivity record includes a list of Bused Connection Descriptors. Each Bused Connection Descriptor describes a bused connection.

Table 3-10: Bused Connection Descriptor

Offset	Length	Field description
0	1	<i>Bused Device Count</i> . The number of devices (D) connected to the corresponding bus.
1	2 * D	<i>Bused Device Descriptors</i> . This is an array of D Bused Device Descriptors. Each entry shall be formatted as defined in Table 3-7.

Each Bused Connection Descriptors includes an array of Bused Device Descriptors. Each Bused Device Descriptor specifies a single port on a specific AMC or on-Carrier device that is connected to the bus.

Table 3-11: Bused Device Descriptor

Offset	Length	Field description
0	1	<i>Resource ID</i> . Indicates the AMC Slot ID or on-Carrier device. [7] Resource Type. 1 AMC, 0 indicates on-Carrier device ID [5:4] Reserved; write 0h [3:0] On-Carrier device ID or AMC Site Number
1	1	<i>Port</i> . Indicates the Port number within the AMC Slot or on-Carrier device.

MicroTCA Carriers implementing bused connections **shall** include a Carrier Based Connectivity record in the Carrier FRU Information.

A Bused Connection Descriptor **shall** be provided for each bus.

A Bused Device Descriptor **shall** be provided for each port of each AMC Slot or on-Carrier Device that is connected to a bus.

During the E-Keying process, the Carrier Manager **shall** explicitly disable all Ports listed in both an AMC's AdvancedMC Point-to-Point Connectivity record and a Carrier Bused Connectivity record.

Use of an AMC that implement Point-to-Point Connectivity on Ports that are bused by the Carrier could result in damage to devices connected to the bus. Disabling the Port via E-Keying does not guarantee electrical compatibility in this case. It is the system integrator's responsibility to ensure that all AMCs to be used in a bused Carrier are electrically compatible with the bused implementation.

If an AMC provides an AdvancedMC Point-to-Point Connectivity record for a Channel that uses a Port listed in the Carrier Bused Connectivity record, the Carrier Manager **should** issue a warning to an appropriate user interface. This warning is intended to alert a system integrator during development and testing that an electrical incompatibility might exist. Specifics of the warning and the user interface are design specific and are outside the scope of this specification.

Compatibility checking, enabling and disabling of bused ports, and arbitration of transmitters and receivers is application specific and is outside the scope of this specification.

3.9 FRU LEDs

Because the μ RTM's LEDs are controlled using an I²C I/O extender, rapid blink rates and short on or off times can cause excessive bandwidth consumption on the I2C bus and of the MMC's microcontroller. For this reason, the Front AMC's MMC **may** round the *On-Duration* and *Off-Duration* times of a Set FRU LED State command with FRU Device ID set to 1 up to the next multiple of 100ms.

3.10 Zone 3 Interface Documentation

FRU information can contain a variety of information about a FRU. It might be desirable to include information describing where to get documentation for the Zone 3 interface. Table 3-12 defines the Zone 3 Interface Documentation record. This record provides a Uniform Resource Locator (URL) that can be used to locate documentation for the Zone 3 Interface of the corresponding FRU.

Table 3-12: Zone 3 Interface Documentation record

Offset	Length	Field description
0	1	<i>Record Type ID</i> . Value C0h (OEM).
1	1	[7:7] End of list. Set to one for the last record. [6:4] Reserved, write as 0h. [3:0] Record format version (=2h for this definition).
2	1	<i>Record Length</i> . = N+4
3	1	<i>Record Checksum</i> . Holds the zero checksum of the record.
4	1	<i>Header Checksum</i> . Holds the zero checksum of the header.
5	3	<i>Manufacturer ID</i> . For this specification 12634 (0x00315A, LSB first) shall be used
8	1	<i>PICMG Record ID</i> . The value TBD shall be used for this definition.
9	1	<i>Record Format Version</i> . For this specification, the value 0h shall be used.
10	N	<i>URL</i> . The Internet Uniform Resource Locator string that can be used through a World Wide Web browser to obtain documentation information about this Zone 3 interface. (e.g. “http://www.my_vendor.com:280?docu=my_board”)

AMCs and μ RTMs **may** provide a Zone 3 Interface Documentation record in their FRU information.

4 Electrical

4.1 General

This document uses the electrical specifications for AMC's and μ TCA shelves. This specification adds a connector in Zone 3 of a doublewide AMC and an associated μ RTM module. Other than defining the Zone 3 connector, the μ RTM module and the μ TCA shelf this specification relies on previous documents for most details.

4.2 Power

4.2.1 AMC and RTM Power

Total power used by AMC front board and its associated μ RTM **shall** conform to PICMG AMC.0 R2.0 except that the maximum Management Power current **shall** be increased from 150 mA to 180 mA. Of this 180 mA the μ RTM is limited to 30 mA. The current limit for the AMC remains at 150 mA.

The Payload Power **shall** not be enabled to the μ RTM until system management has performed a compatibility check. This check should include the μ RTM temperature if it can be obtained prior to asserting the Payload Power.

4.2.2 μ RTM Power

Two voltages are fed from the front board to the μ RTM. One is Payload Power (PWR) and the other is Management Power (MP). The MP current **shall** conform to AMC.0 R2.0, Section 4.2.2. The front board MMC **shall** control the switching of the PWR to the μ RTM. The designer **shall** consider the voltage drop that will be introduced if these voltages are switched by the AMC.

For AMC's and associated μ RTM's following the specifications in [Sections 2.1.3.2](#) and [2.2.3.1](#) the four power pins (A1, B1, A2, B2) on the J30/P30 ADF connectors **shall** be connected together on both modules with impedances that do not differ by more than 20% to insure current flow is the same to 20%. For other connectors the power pins assigned **shall** conform to the specifications in this and other sections.

The MP current drawn by the μ RTM **shall not** exceed 30 mA.

MP surge current **shall** be limited to 270 mA for a maximum of 200 ms.

The PWR current drawn by the μ RTM **shall not** exceed 3 amperes. The voltages for the μ RTM's PWR and MP pins are the same as those defined in AMC.0 R2.0, Section 4.2 with the drop of the PWR switch taken into account by the module designer.

The Module **shall** be designed so that sudden power loss **shall not** cause permanent damage to the module.

The average power calculation in AMC.0, REQ 4.4b **shall** include the μ RTM in the calculation.

The μ RTM module **should** provide an input capacitance of at least 0.5 μ F on Payload Power per W of its maximum Payload Power requirement.

The voltage tolerances in AMC.0, Section 4.2.1.2 **shall** be applied to the μ RTM.

The power and grounding in AMC.0, Section 4.2.2 and 4.2.3 **shall** be applied to the μ RTM.

4.3 Data

The Zone 3 data connectors **shall** conform to PICMG 3.0 R3.0, Section A.4. The backplane connectors **shall** conform to PICMG MTCA.0 R1.0, Section 7.

4.4 Clocks

Clocks on the Zone 3 plug are not defined by this specification. User defined pins can be used for this purpose. Other clocks in the AMC connector follow MTCA.0 and Section 6 below.

4.5 Isolation

Input isolation is defined as in PICMG MTCA.0 R1.0, Section 4.8.1.11. AC isolation is defined in PICMG MTCA.0 R1.0, Section 4.8.2.2.

4.6 ESD

See PICMG AMC.0 R2.0, Section 2.2.6.

4.7 Signal Levels

User specified signal levels in Zone 3 at the AMC/ μ RTM interface **shall not** exceed the levels specified by the mechanical keying in Table 2-1 .

5 Thermal

5.1 Thermal Requirements

The following document **should** be used as a guide for thermal requirements for both the Front Board and the μ RTM.

PICMG AMC.0 R2.0: Advanced Mezzanine Module specification, Section 5

PICMG MTCA.0 R1.0: μ TCA base specification, Section 5

PICMG MTCA.1 R1.0: Air Cooled Rugged μ TCA specification, Section 5

5.2 Air Flow Balancing

See this document [Section 2.3.4](#).

5.3 μ RTM power

The average power on the μ RTM **shall not** exceed 30 watts. This power limit is calculated from the 3 A limit on the pins and the minimum of 10 V as given in AMC.0 R2.0, Section 4.2. Since all power is supplies by the front AMC module, the power used buy the μ RTM **shall** be subtracted from that available to the AMC front board. The maximum power available to the AMC is 80 W.

6 Interconnect

6.1 Introduction

Needs to be written

6.2 Fabric interface

Fabrics are as specified in PIGMC AMC.1 thru AMC.4. No specification in this document.

6.3 MCH Specifications

The hardware platform management is specified in MTCA.0, Section 3. No specification in this document.

6.4 Clocking

6.4.1 General clocking topology

Figure 6-1 shows the general concept of the clock, trigger and interlock signal connections. Two radial clocks as defined in AMC.0 are used to distribute low jitter, high quality clocks by radial links from all AMC slots to the MCH. FCLKA is reserved and provided for PCIe usage. Ports 17 to 20 (Rx17/Tx17 to Rx20/Tx20) are used as a bus for trigger, clock and interlock signal distribution.

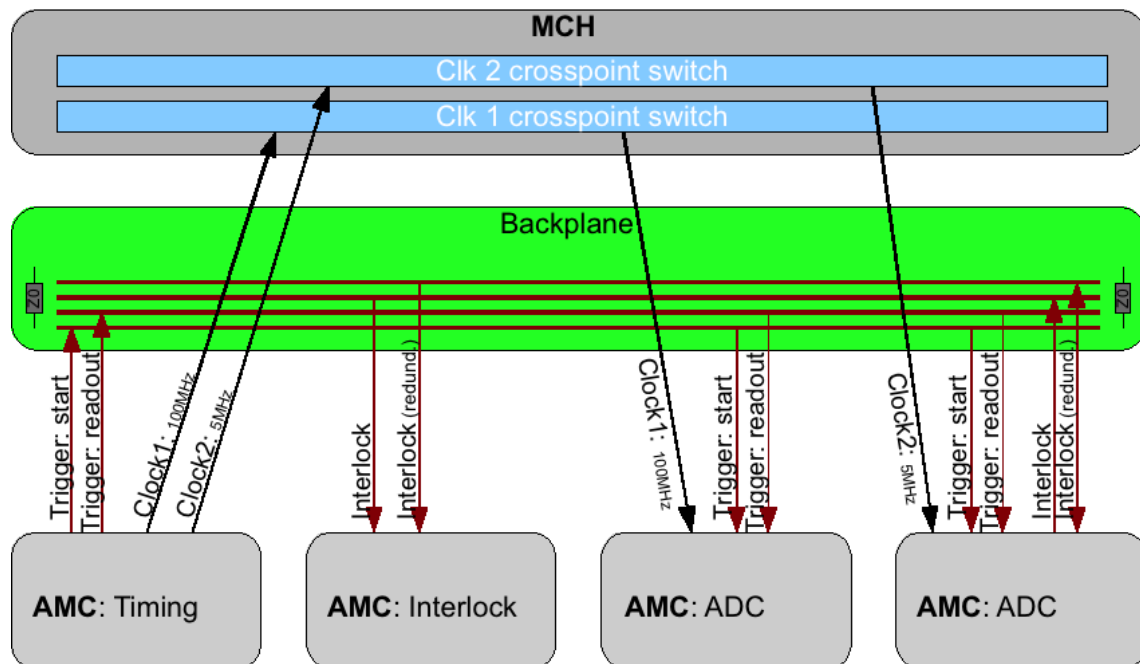


Figure 6-1: Example using radial clocks and bused triggers

6.4.2 Radial clock circuitry

Two point-to-point lines from all AMC modules to the MCH implement the clocks as differential pairs (M-LVDS) as defined in AMC.0, Section 6.3.1. The lines are bidirectional. Any AMC can be the source or the receiver of clock TCLKA or TCLKB. A 100 Ω line-termination is required on both ends of the transmission line. These terminations are in both the MCH and the AMC module as shown in Figure 6-2. Any stubs in the PCB layout have to be avoided (see AMC.0, Section 6.3.1).

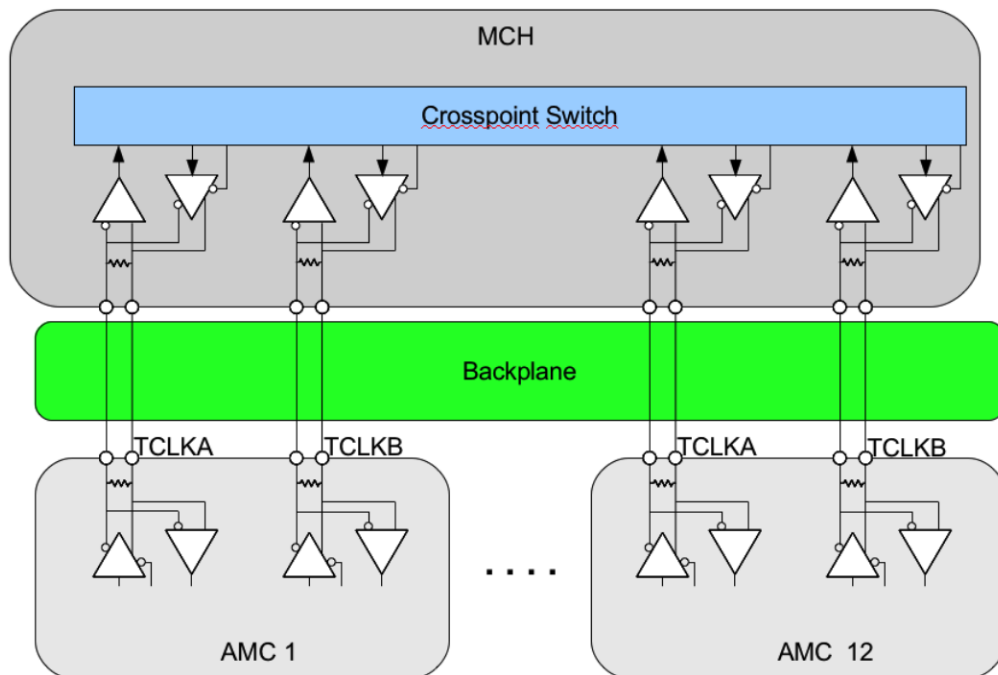


Figure 6-2: TCLKA and TCLKB are bidirectional example.

TCLKC and TCLKD are implemented in a similar manner to TCLKA and TCLKB except they are connected to the redundant MCH.

6.5 Bus lines general topology

In Figure 6-3 an example usage of the bus lines is given. The differential Receiver and Transmitter lines of the ports 17 to 20 of all AMC's are connected together on the backplane. At both ends of the backplane these lines **shall** be terminated by 100 Ω .

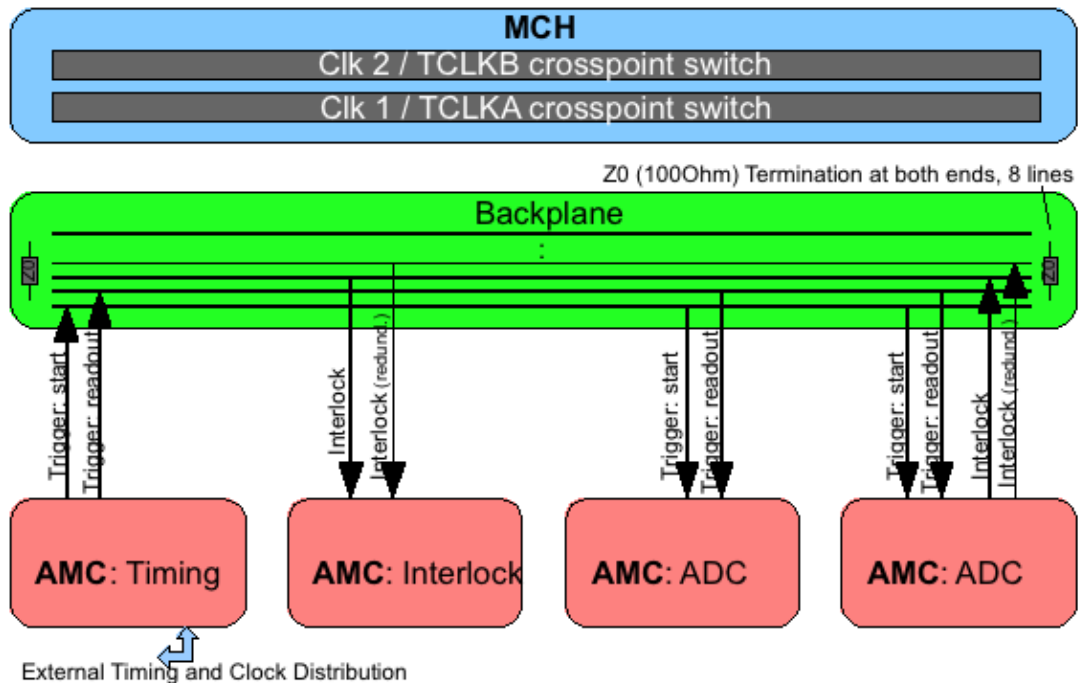


Figure 6-3: Example using the 8 bus lines

6.5.1 Ports 17 to 20 usage

The differential lines **shall** be driven by M-LVDS, according to EIA/TIA-899. The AMC modules may implement a receiver or a transmitter or both on every Rx and Tx pair of the ports 17 to 20. The differential lines on AMC modules (stubs) should be short as possible but no longer than 30 mm.

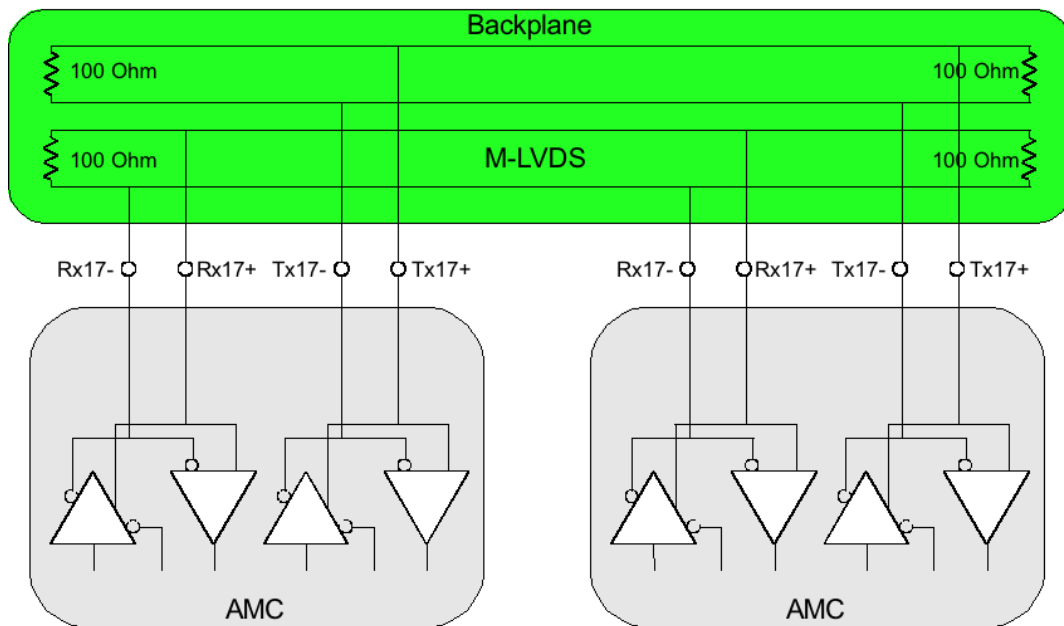


Figure 6-4: M-LVDS transceiver shown for port 17

The usages of the bus lines are application dependent. Table 6-1 indicates a possible usage.

Table 6-1: Example usage of the 8 bus lines for triggers, interlocks and clocks

AMC Port	Name	Description	Usage
Rx17	TrigStart	Start sampling data	Triggers
Tx17	TrigEnd	Stop sampling data	
Rx18	TrigReadOut	Start data transfer to CPU	
Tx18	ClkAux	Low performance clock	
Rx19	Reset	Reset of counter, dividers	
Tx19	Interlock 0	Interlock line 0	3 interlocks to provide 2 out of 3 redundancy
Rx20	Interlock 1	Interlock line 1	
Tx20	Interlock 2	Interlock line 2	

6.6 JTAG interface

See PICMG MTCA.0 R1.

6.7 μ TCA interface topologies

6.7.1 Backplane

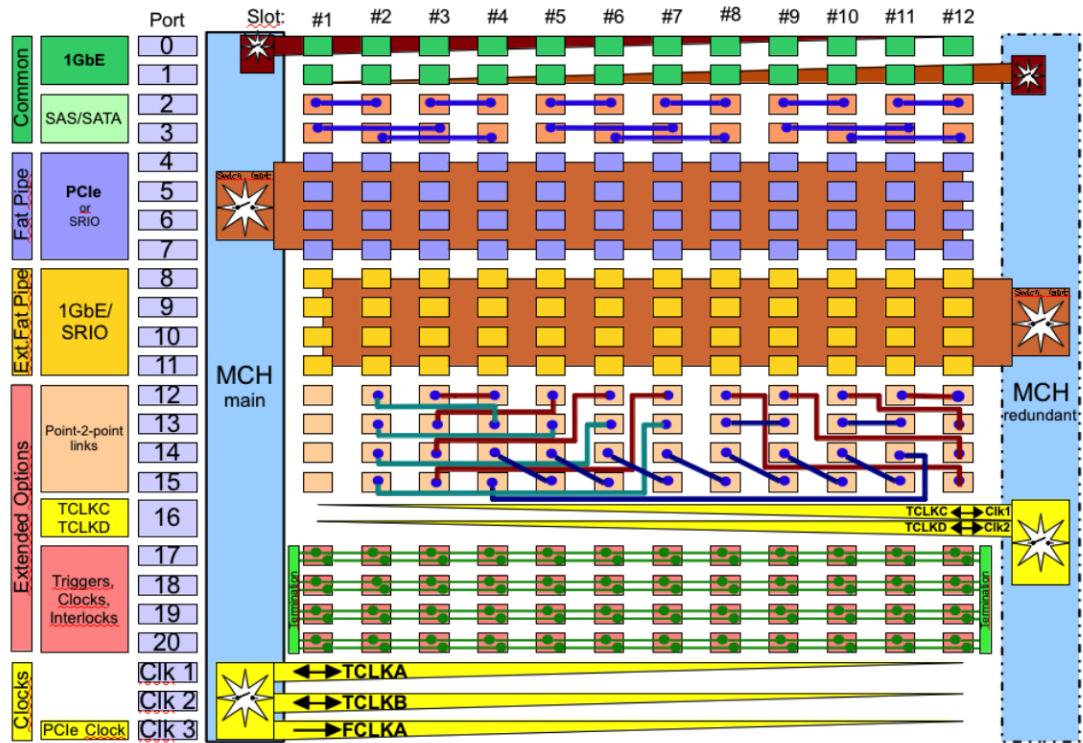


Figure 6-4: Example of a μ TCA Physics backplane

The following are the uses of the various Ports and Clocks in this example.

- Port 0 **should** be used for base Ethernet interface. Port 1 is connected to the optional (redundant) MCH.
- Port 4 to 7 **should** be used for PCIe.
- Port 12 to 15 **may** be used for application specific wire-ring.
- Ports 17 – 20 **should** be wired as a bus according Section 6.4.
- FCLKA (Clk3) **should** be used for PCIe clock distribution as defined in MTCA.0 R1.0
- TCLKA and TCLKB **should** be wired from the main MCH to all AMC slots.
- TCLKC and TCLKD **should** be wired from the redundant MCH to all AMC slots.

6.8 MCH Connector pin allocations

The MCH is connected according to MTCA.0.

6.9 System examples

Add Physics example(s)

7 Regulatory

The following are regulatory documents that may be required:

PICMG AMC.0 R2.0: Advanced Mezzanine Module specification, Section 7

PICMG MTCA.0 R1.0: μ TCA base specification, Section 7

Radiation tolerance?

Water cooling?

Materials?

Etc.

Add Others

8 A. Twenty and Thirty Pair Advanced Differential Fabric connector definitions

The information in this Appendix is similar to that in PICMG 3.0 except that it delineates 20 and 30 pair versions of the Advanced Differential Fabric (ADF) connector.

A.1 General data

A.1.1 Objective of this document

See PICMG 3.0 R3.0

A.1.2 Scope

See PICMG 3.0 R3.0

A.1.3 Intended method of mounting

See PICMG 3.0 R3.0

A.1.4 Ratings and characteristics.

See PICMG 3.0 R3.0

A.1.5 Normative references

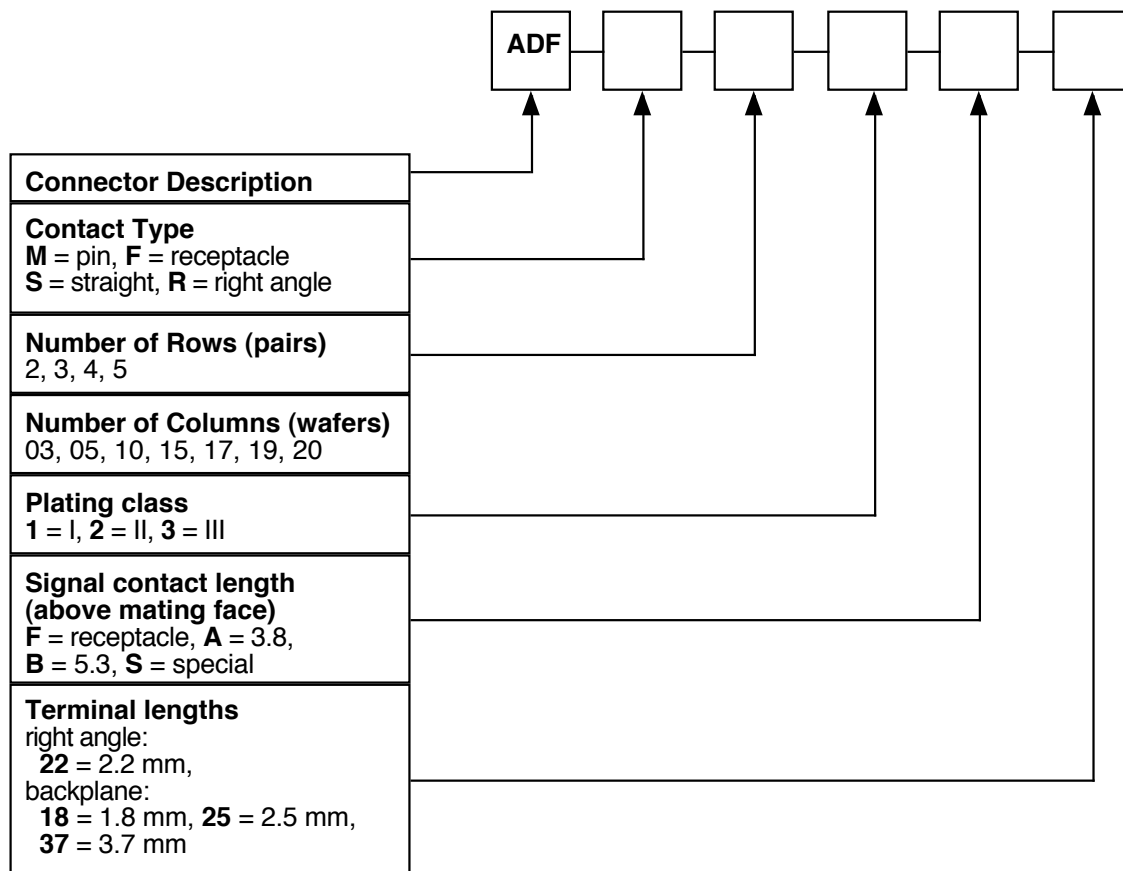
See PICMG 3.0 R3.0

A.1.6 Markings

See PICMG 3.0 R3.0

A.1.7 Type designation

Table A-1: ADF part number designator



Using this nomenclature a receptacle 30 pair ADF receptacle connector in Zone 3 of the AMC would be designated:

ADF-FR-3-10-2-F-22

The mating connector on the μ RTM would be designated:

ADF-MR-3-10-2-B-22

Note that for the male right angle only the B signal contact length is available.

A.2 Technical information

A.2.1 Definitions

A.2.1.1 Contacts and terminations

See PICMG 3.0 R3.0 except on line 37 and change “Front Board” to “Front Board and μ RTM”.

A.3 30 Pair ADF Connectors

A.3.1 General isometric view and common features

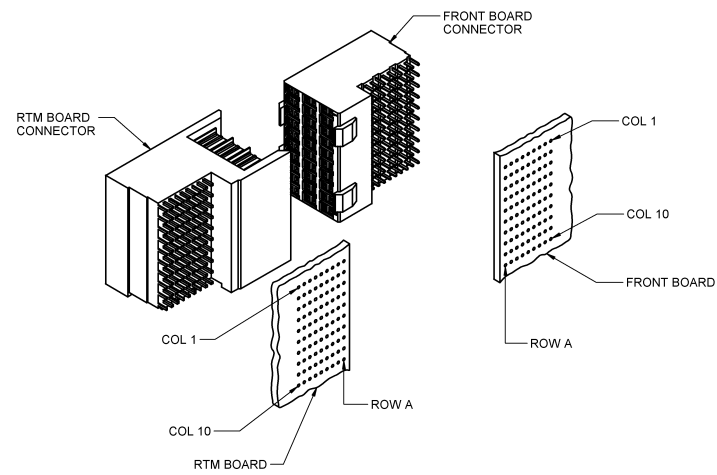


Figure A-1 Zone 3 front board and μ RTM mating diagram

Note: Reverse RTM and AMC in drawing.

A.3.2.2 Right Angle Pin Connector

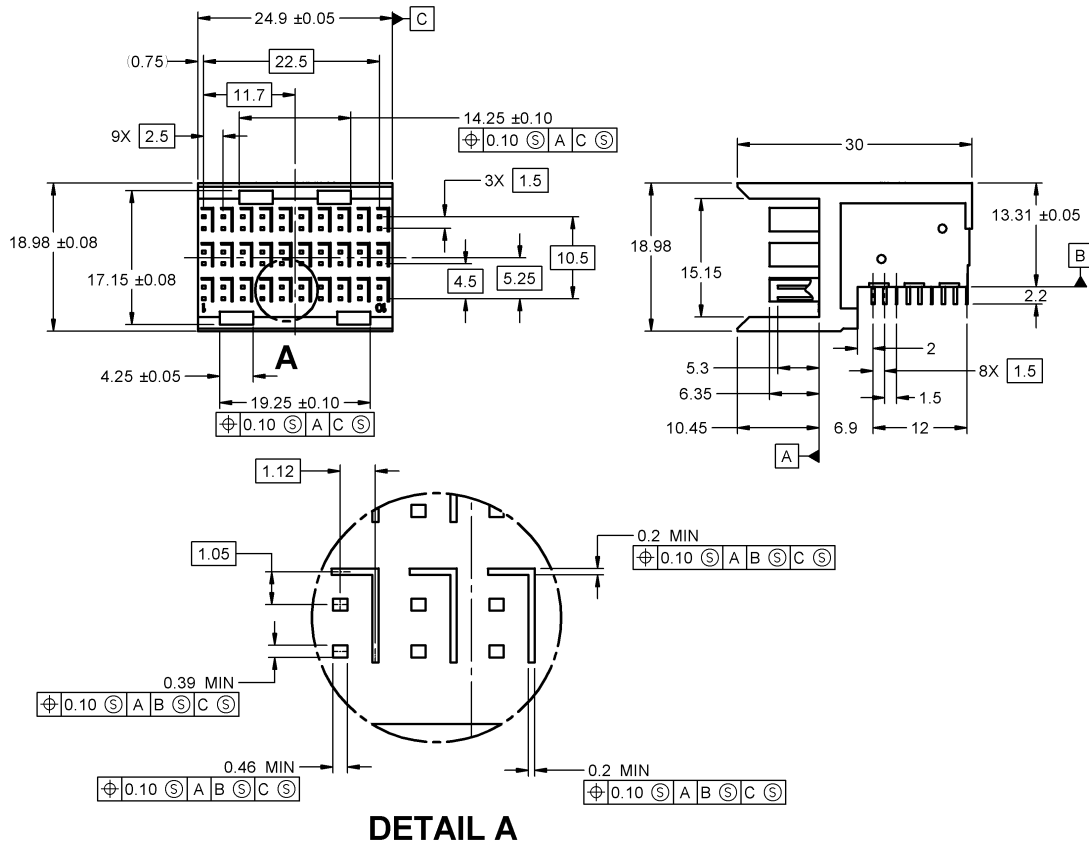


Figure A-3: Three row μ RTM connector dimensions

A.3.2.2.1 Contacts

See PICMG 3.0, Section A.3.3.2

A.3.2.2.2 Contacts tip geometry

See PICMG 3.0, Section A.3.3.3

A.3.2.2.3 Terminations

See PICMG 3.0, Section A.3.3.4

A.4 Dimensional information for 20 Pair Connectors

A.4.1 General isometric view and common features

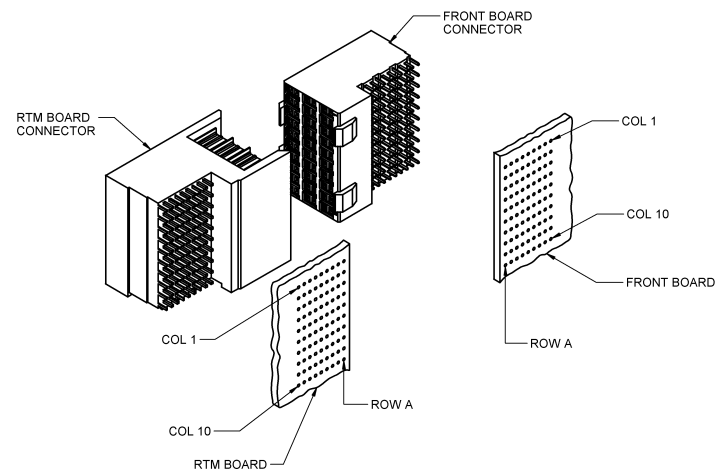


Figure A-4 Zone 3 front board and μ RTM mating diagram

☞ Note: Need 20 pair version. Reverse RTM and AMC in drawing.

A.4.2 Dimensional Information

A.4.2.1 Right Angle Receptacle Connector

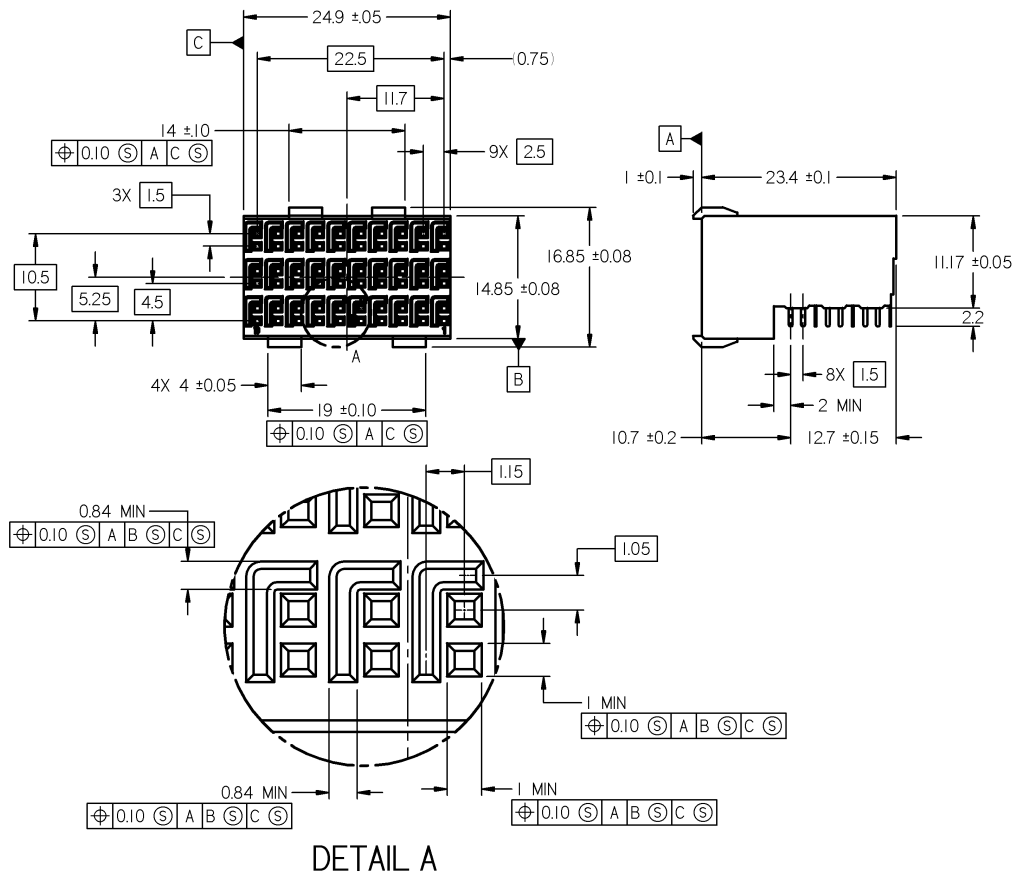


Figure -A-5 Two row μ RTM connector dimensions

Note: Need 20 pair version.

A.4.2.1.1 Terminations

See PICMG 3.0, Section A.3.4.2

Mating Right-Angle with Right-Angle Connectors

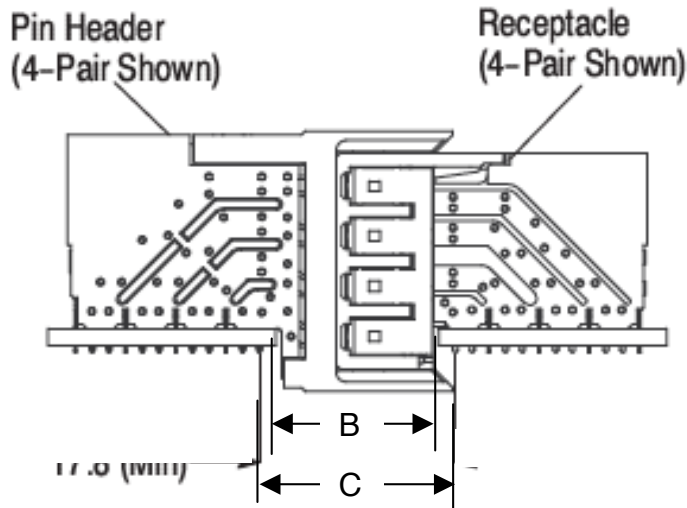


Figure A-7: Right Angle – Right Angle Connector Mating

☞ Note: Need 30 pair version.

The dimensions for mating are the same for the 20 pair connectors.

Table A-2: Connector Mating Sequence

Product Family	Dim B (mm) fully mated	Contact	Dim C (mm)	
			Reliable mate	Fully mated
ADF	14.8	Ground Shield	22.4	21.0
		Signal Level 2	20.8	17.8
		Signal Level 1	Connector not available	

☞ This table should be carefully checked!

A.5.2 Perpendicular to engagement direction

See PICMG 3.0, Section A.3.2.3

A.5.4 Inclination

See PICMG 3.0, Section A.3.2.4

A.6.3 Mounting information for 30 Pair μ RTM connectors

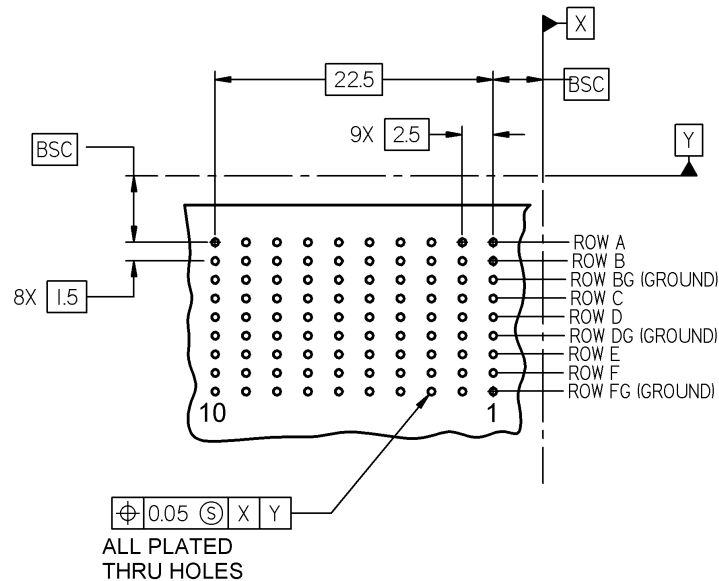


Figure A-9: Three-row connector μ RTM PCB hole layout
View from component side 2

☞ To be checked! Reverse 10 and 1??

The 30 pair ADF right angle pin connector **shall** use the hole pattern in Figure A-9.

A.6.4 Mounting information for 20 Pair μ RTM connectors

The hole pattern for the 20 pair pin connector **shall** be the same as Figure A-9 except that rows E, F and FG (Ground) are not used.

A.4 Characteristics

This section same as PICMG 3.0 R3.0, Appendix A.4 except as noted in the following sections.

A.4.1 Propagation delay

Remove G and H Pins from PICMG 3.0 R3.0 Table A-9 for three connectors and E, F, G, and H for the two-row connector,

B. Keys

B.1 Male Key Dimensions

The male key/alignment pin in Figure B-1 **shall** be used on the μ RTM. Orientation codes are in Table B-1.

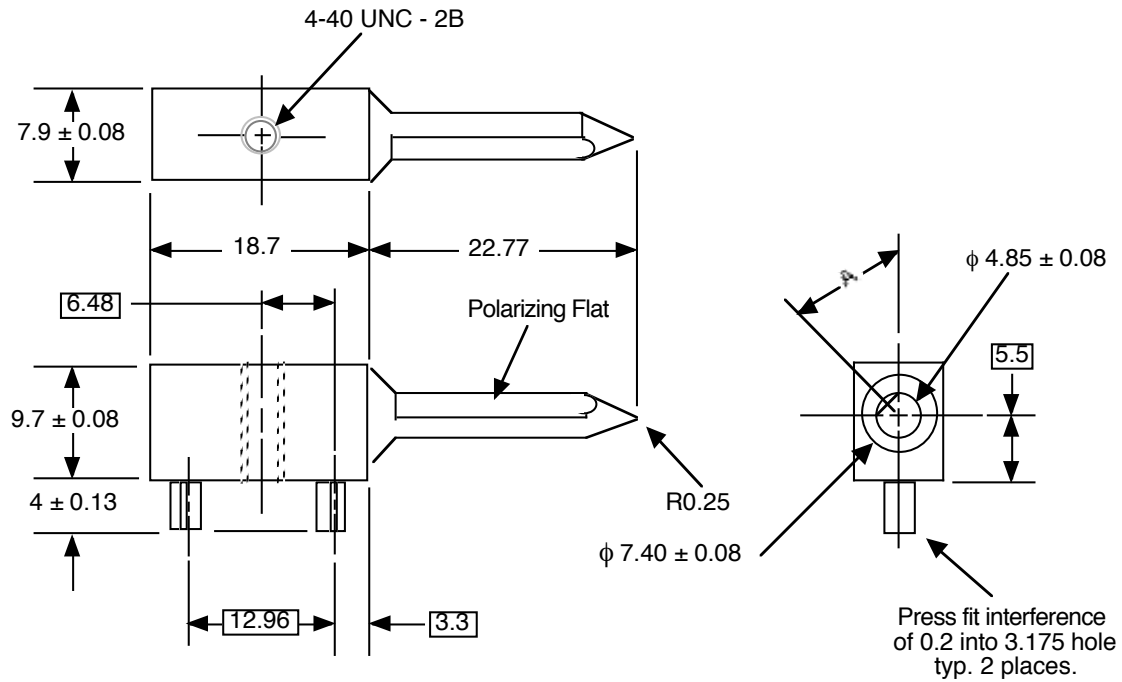


Figure B-1 Male key

B.2 Female Key Dimensions

The female key block shown in Figure B-2 **shall** be used on the Physics AMC module.

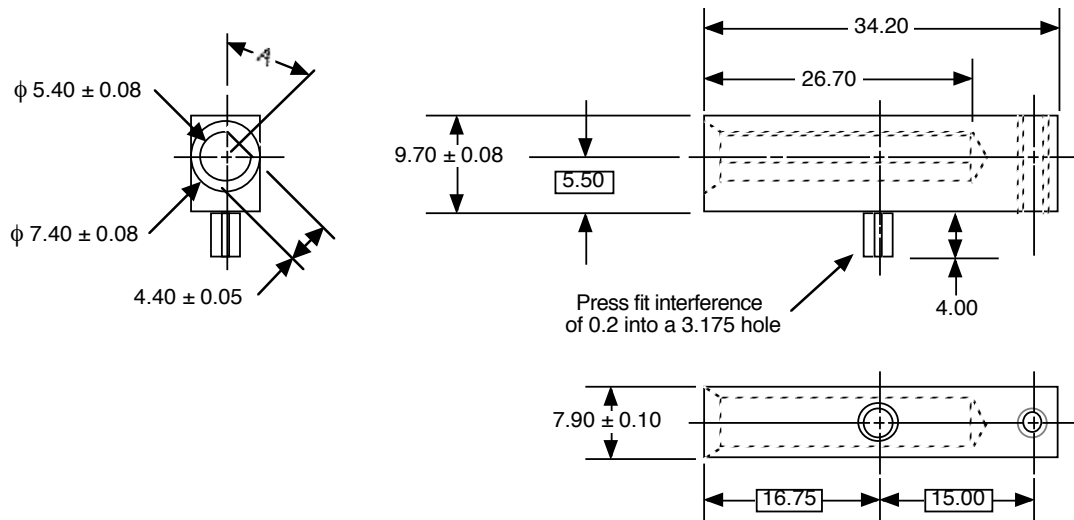





























Figure B-2 Female key

For cases where keying is not used (e.g. some test equipment) an un-keyed version of the female block is available. The un-keyed version is entry 0 in Table B-1.

B.3 Key Orientation

Table B-1 indicates the orientation of the male and female keys. The meaning of the codes is contained in Table 2-1 of this document.

Table B-1: Key positions (standard orientation)

Value “A”	Rotation (degrees)	View from front of Shelf		View from rear of Front Board
		Receptacle	Post	Receptacle
1	0			
2	45			
3	90			
4	135			
5	180			
6	225			
7	270			
8	315			
0	NA			

The value “A” of zero for has a unique position in the table. If the receptacle does not have a flat (i.e. A = 0) any post will fit into it. The receptacle just serves as an alignment mechanism. This feature might be of use in test fixtures. A post that does not have a flat will only fit into a “zero” receptacle.

C. Appendix C

This and following appendices are reserved for connectors other than the ADF types