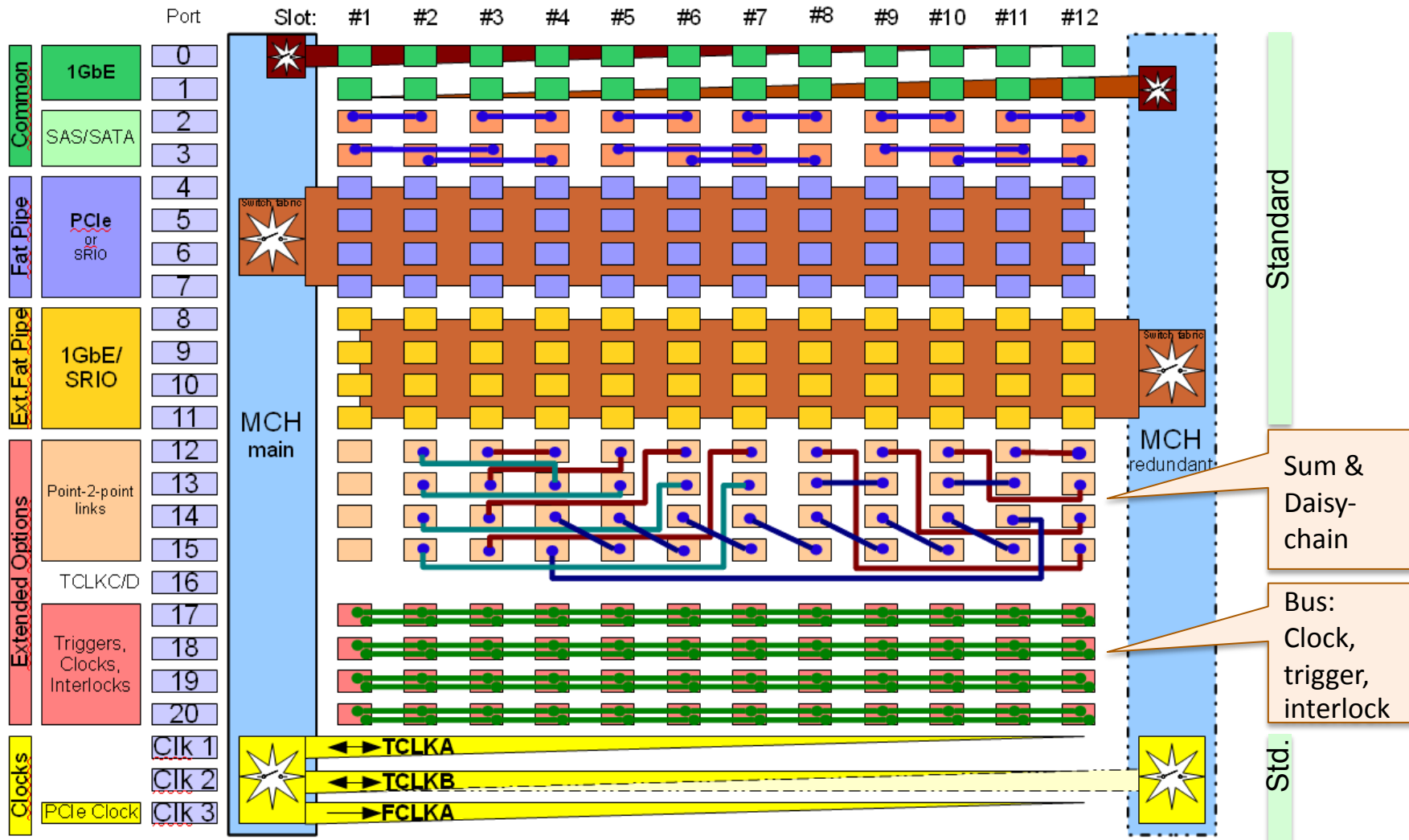
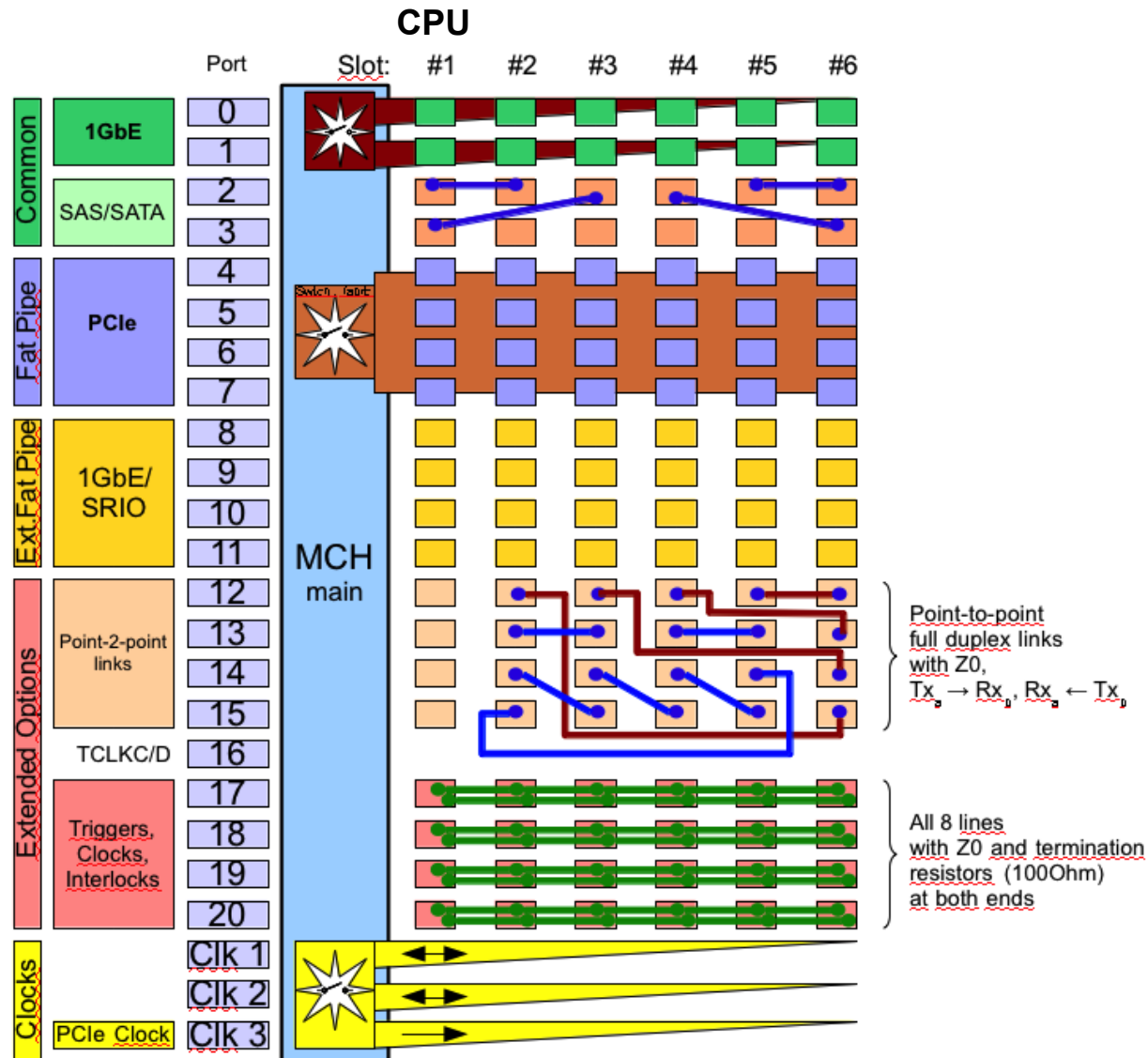


Backplane Status

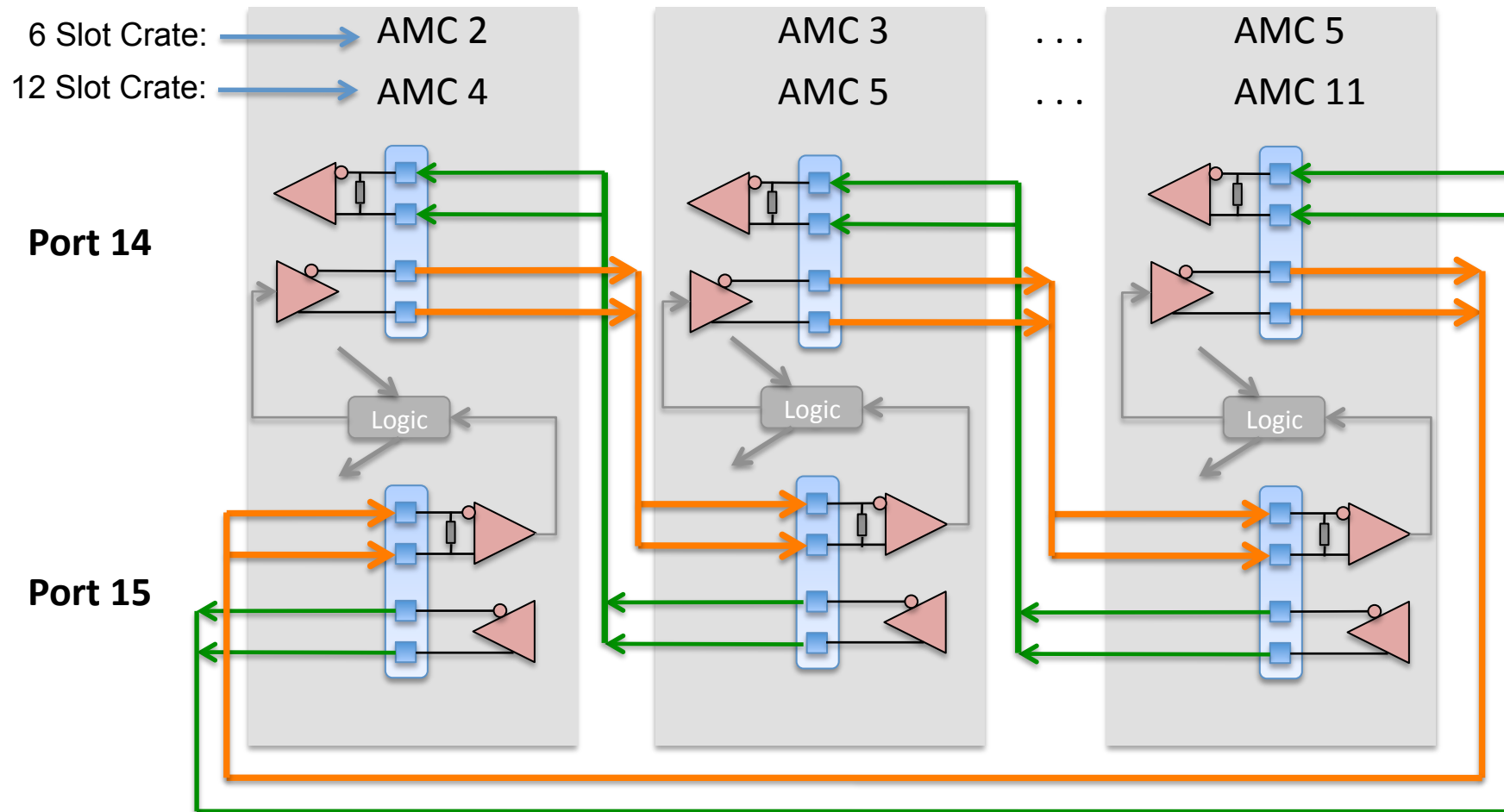
Kay Rehlich (DESY), 22.6.2010



6 Slot Backplane

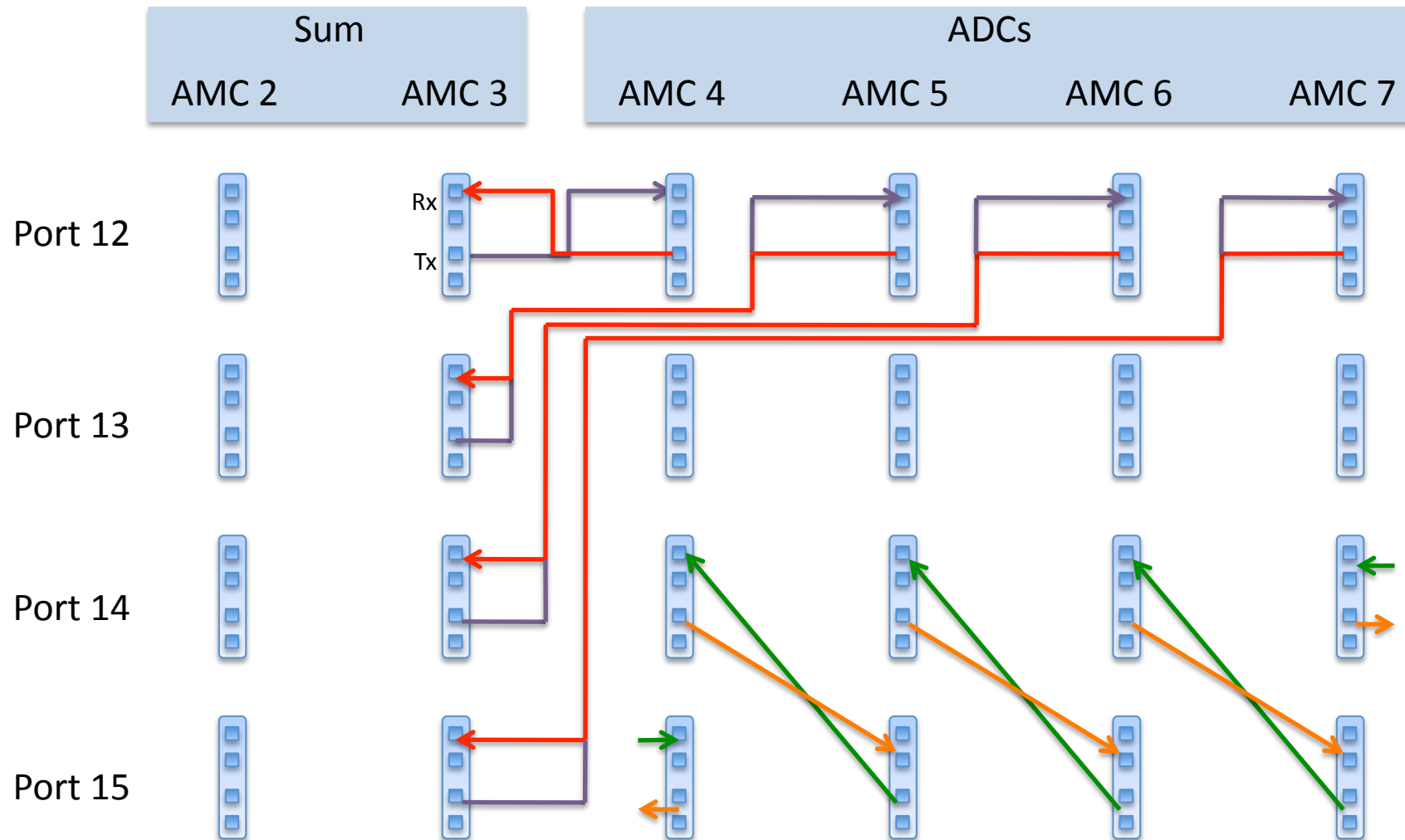


Daisy Chain: Ports 14/15

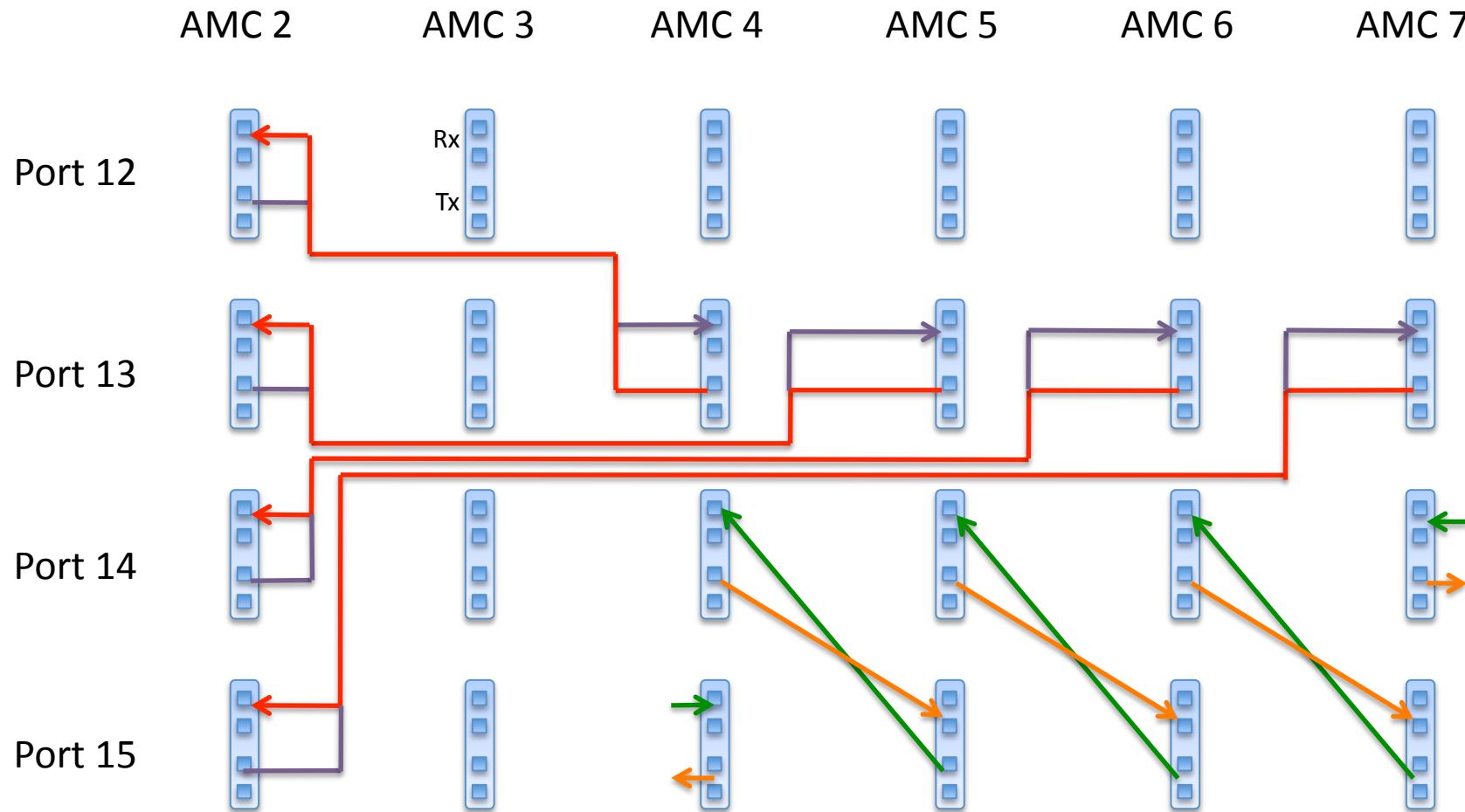


Backplane connections: **forward**, **backward**

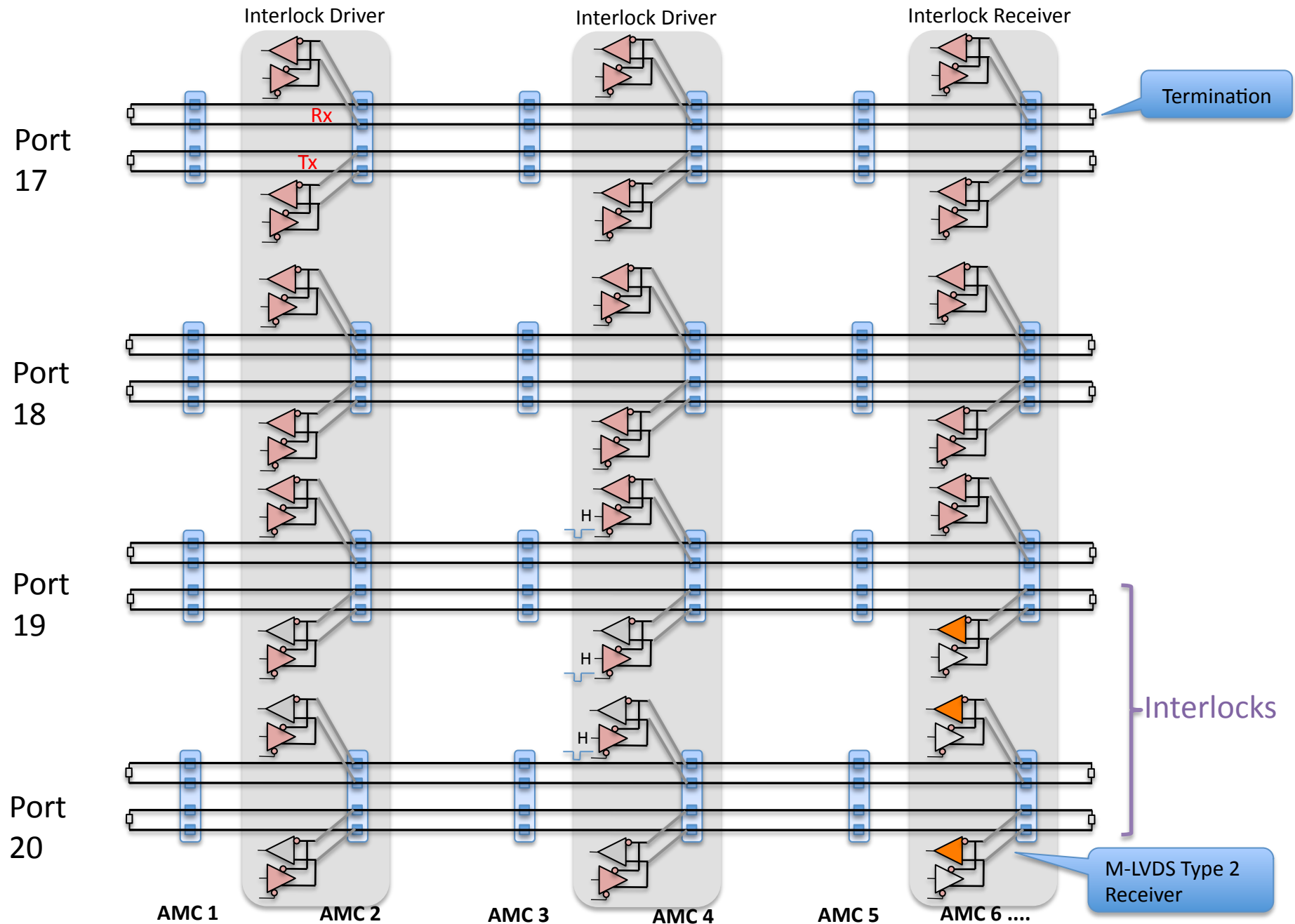
„Summing“ Ports Slot 3 (12 Slot Shelf)



„Summing“ Ports Slot 2 (12 Slot Shelf)



Bussed Lines



M-LVDS Driver

e.g. SN65MLVD080:
8*T_x, 8*R_x; 250Mbps

e.g. SN65MLVD082:
8*T_x, 8*R_x; 250Mbps

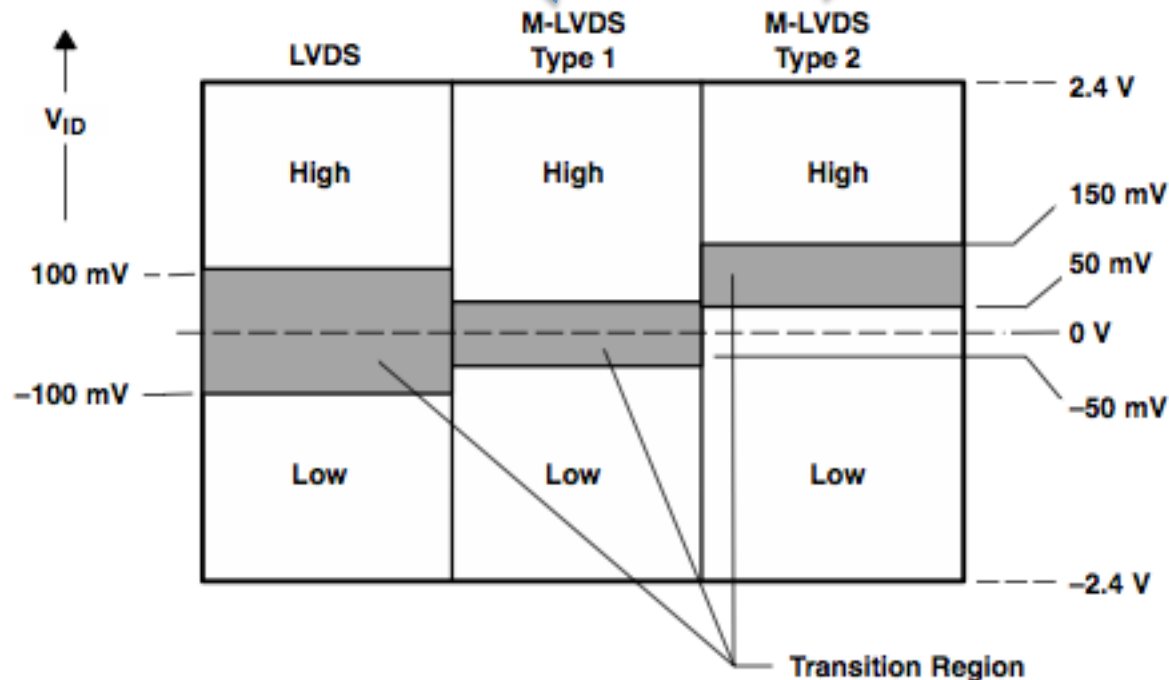


Figure 2-3. LVDS and M-LVDS Differential Input Voltage Thresholds

The M-LVDS standard defines two types of receivers, designated as Type-1 and Type-2. Type-1 receivers (SN65MLVD080) have thresholds centered about zero with 25 mV of hysteresis to prevent output oscillations with loss of input; Type-2 receivers (SN65MLVD082) implement a failsafe by using an offset threshold. In addition, the driver rise and fall times are between 1 and 2.0 ns, complying with the M-LVDS standard to provide operation at 250 Mbps while also accommodating stubs on the bus. Receiver outputs are slew rate controlled to reduce EMI and crosstalk effects associated with large current surges. The M-LVDS standard allows for 32 nodes on the bus providing a high-speed replacement for RS-485 where lower common-mode can be tolerated or when higher signaling rates are needed.

Open Items:

- Management items needed to insure compatibility.
 - What is needed in the EEPROM tables?
 - Port usage; for bussed lines: port Rx/Tx usage
 - Possible port types: p2p, clock, trigger, interlock, other?
 - Criteria for enabling a board
 - Handle the two section (p12-15, p17-20) independent
 - Allow if not conflicting with section usage
- Consequences of improper module insertion.
 - How does one detect a missing daisy chain module?
 - Depends on the implementation of the logic:
open = error/interlock active
 - What happens if fabric port on one of these physics ports?
 - Board should not be enabled
 - Other?