Clock and control fast signal specification

M.Postranecky, M.Warren and D.Wilson 02.Mar.2010

1 Introduction

This document defines fast signals (protocols, connectors and cables) used by the Clock and Control (CC) system of XFEL 2D pixel detectors. Clearly the document's content may have to be modified; known open issues are highlighted with **bold text**.

The latest version of the document can be found at:
http://www.xfel.eu/project/organization/work_packages/wp_76/daq/2d_pixel_detectors/clock_and_control/

Three 2D pixel detector collaborations (AGIPD, DSSC and LPD) are building detectors for use at XFEL. These detectors will use common backend DAQ and control (CC) systems and consist of three sub-systems:

- Front End Electronics (FEE) of the detectors. The FEEs are detector specific custom implementations.
- Train Builder (TB) data readout. The TB is used to build data into frame ordered bunch train specific contiguous blocks, which are then sent on to a computing farm layer for processing.
- Clock and Control (CC). The CC interfaces to the XFEL timing system, generates and receives fast signals used to synchronize detector FEEs, and distributes configuration information using the fast signals or network messages.

2 Fast signal connectors and cables

A schematic showing the CC fast signal connectivity is show in Figure 1.

RJ45 connectors are used for both the inputs and outputs. CAT5 (or better) cables will be used. Socket A is the default input from the XFEL Timing Receiver (TR) board. Socket B is used for the

external non-XFEL timing sources like LCLS. The pin assignments of A and B are defined so that the sockets can be combined into a single socket if there are physical space limitations. Timing input cable lengths are expected to be short, e.g. the XFEL TR resides in the same crate as the CC.

The inputs from the TR board and the external inputs will normally be DC-coupled, but should the option of being AC-coupled be included?

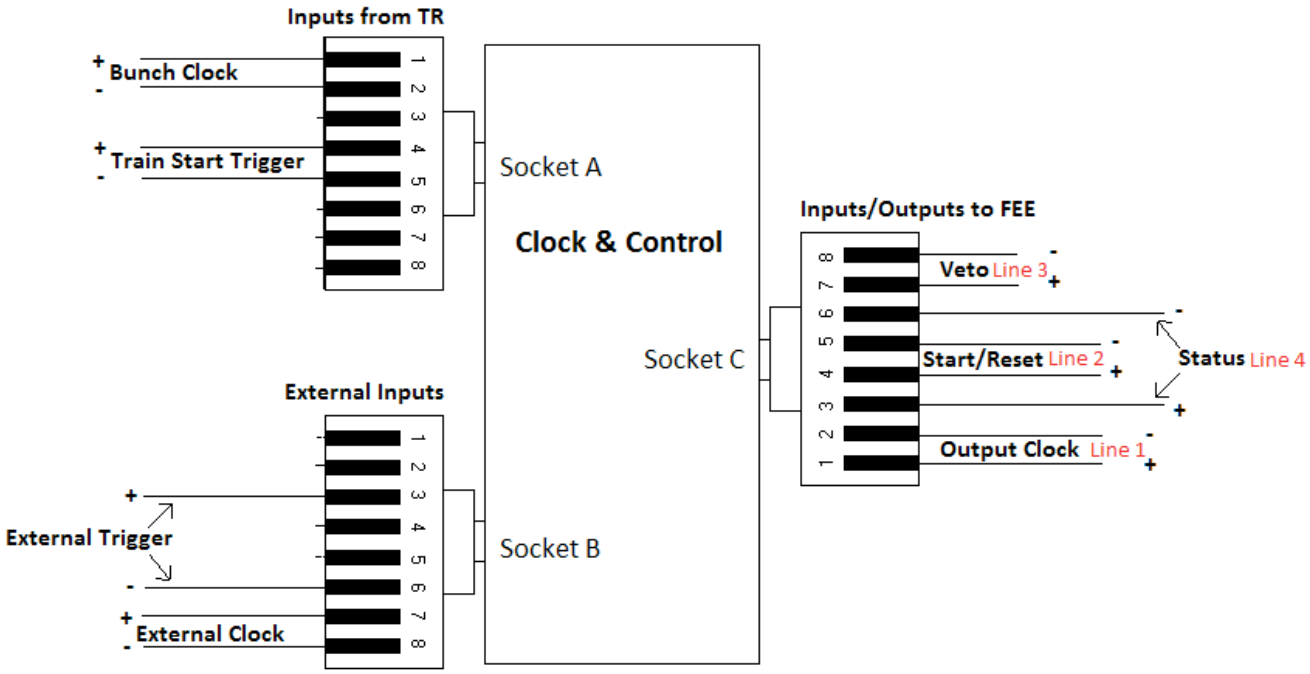

Figure 1 Timing and FEE connection schematic

The CC fan-out board(s) perform fan-out and fan-in of the fast signals to and from the FEEs.

It has yet to be determined how the Veto signal will be inputted to the CC master. Multiple Veto sources are defined and the interface between the CC master and the Veto unit still needs to be decided on.

3 Timing interfaces

Timing interfaces (clocks and triggers) are required to allow detector operations at XFEL and other, non-XFEL, light sources like LCLS. Additionally standalone running using internally generated timing signals is required. The different timing interfaces required are described below.

XFEL Timing Interfaces

The XFEL TR board will provide front panel and backplane timing signal outputs.
Four 5-pair har-link (http://www.harting-connectivity-networks.de/en/produkte/produktauswahl/interface-steckverbinder/metrische-interface-steckverbinder-im-20-mm-kontaktraster-har-link) front panel connectors provide access to the encoded trigger message data stream, the 4.51 MHz bunch clock and to programmable outputs. The later can provide trigger pulse (train START, STOP…), delayed trigger pulses (START + 15ms…), gates, bursts and

patterns. The backplane PCIe will allow interrupt driven CC crate CPU synchronization to the TR. Note that no technical or user documentation exists for the TR board which is currently being prototyped.

Table 1 defines TR signals required by the CC.

Name	Signal type	Socket / Pin	Signal	Purpose
Bunch clock	Differential LVDS	A / 1+2	4.51 MHz clock	4.51 MHz clock – used to generate the synch clock (see Line 1).
Encoded trigger message	Differential LVDS	A / 4+5	**Not Yet Known**	Used to generate control (START, STOP…) messages (see Line 2).

Table 1 XFEL TR timing signals required

The encoded trigger message stream contains START train, STOP train, and other trigger messages.

The CC requirements for trigger messages should be made known to the XFEL timing group, as should input signal characteristics (LVDS, CML…).

Non XFEL timing interface

Table 2 defines non XFEL timing signals required by the CC.

Name	Signal type	Socket / Pin	Signal	Purpose
Bunch clock	Differential LVDS	B / 7+8	750 kHz to 6 MHz clock	4.51 MHz clock – used to generate the synch clock (see Line 1).
Trigger	Differential LVDS	B / 3+6	**Pulse only?**	Used to generate START control message (see Line 2).

Table 2 Non XFEL timing signals required (not finalized)

The information in this section can only be finalized when timing interface information is know from LCLS, Spring8, FLASH, etc. **Open issues:**

- **Where do the signals come from?**
- **Must additional crate hardware be foreseen to access timing information?**
- **Are unique bunch numbers used and, if so, how can they be accessed?**

In view of these uncertainties the following will also be provided:

- Bunch clock: LVTTL or NIM, single ended, LEMO 00, permissible range 750 kHz - 6 MHz. Slower clocks below 750 kHz might require additional (external) circuitry and will not meet jitter etc. specs. Faster clocks above 6 MHz acceptable but will not permit synchronous veto.
- Trigger input: LVTTL or NIM, single ended, LEMO 00

Standalone timing interface

An internally generated 4.51 MHz clock is provided for standalone running.
This also provides, smoothly and without glitches, the 99.31 Mhz clock in case of loss of the machine clock from the TR board.

Standalone trigger could be generated by software via FPGA.

4 FEE fast signal interface

This section describes the CC FEE fast signal interface.

The FEE interface is used to distribute synchronization and bunch train configuration information train ID, bunch pattern ID…) to the FEEs. Currently only one quantity is sent from the FEE to the CC.

A schematic showing the proposed connection functionality is shown in Figure 1 and fast signal definitions in Table 3.

If shown necessary, the CC could individually skew the fast command lines 2 & 3, w/respect to the clock Line 1, using the programmable ODELAY feature of the 'Virtex-5' Xilinx FPGAs. This provides 64 steps of about 75ps delay (up to 4.8 ns range).

Name	Receiver	Signal type	Socket / Pin	Signal	Purpose
Line 1	FEE	Differential LVDS	C / 1+2	99.31 MHz clock	Synch Clock
Line 2	FEE	Differential LVDS	C / 4+5	99.31 MHz clock encoded message	Control command (START train, STOP train…)
Line 3	FEE	Differential LVDS	C / 7+8	99.31 MHz clock encoded bunch number AND / OR 4.51 MHz clock encoded yes/no	Veto command
Line 4	CC	Differential LVDS	C / 3+6	C / 3+6	FEE status

Table 3 CC FEE (FPGA-FPGA) fast signal definitions

Line 1: clock

Line 1 distributes a 99.31 MHz synchronization clock derived from the glitch less input bunch clock. It is proposed that the overall jitter of this clock at the CC output will be 100 ps or better.

Line 1 is to be AC-coupled on the FEE (see Section 5)

Line 2: control commands

Line 2 distributes control commands to the FEEs by encoding information on a 99.31 MHz carrier clock.

Command	Start bits	Payload	Purpose
START	1100	Train ID (32 bit) + Bunch pattern ID (8 bit) + ex-OR checksum (8 bit)	Notifies FEE of coming train (in N clocks = 15ms) and provides train relevant information

STOP	1010	none	Notifies FEE that train ended
RESET	1001	none	Reset FEE micro-controller, etc. via FPGA
reserved	1111		

Table 4 Line 2 control commands

The Train ID will be a unique number for each train, correlated to (or derived from) the Train ID information received from TR. It could be generated by a counter on the CC and incremented by '1' for each subsequent train (while storing the original Train ID as received from TR).

Line 2 is to be AC-coupled on the FEE (see Section 5)

Line 3: VETO and NOVETO commands

Line 3 distributes a VETO and NOVETO commands to the FEEs. Two protocols are defined for distributing the command: a 99.31 MHz clock-synchronised with the bunch number to be vetoed encoded on it, or a 4.51 MHz clock-synchronised with yes/no (high/low) encoding and with a fixed (but re-configurable) latency. The later provides backwards compatibility with the original veto signal definition. A detailed description of the two protocols is given in Section 7

As described above, the 99.31 MHz message, being acceptable to LPD, AGIPD and DSSC, will be distributed. The LPD will receive the VETO message with a fixed (but reconfigurable) latency w/respect to the pulse being VETO'd or NOVETO'd. For AGIPD and DSSC, the VETO messages will have variable latency, but still remain synchronised to the 4.51 MHz clock.

Command	Start bits	Payload	Purpose
VETO	110	Bunch ID (12 bit) + Reserved (4 bins)	Identifies the Bunch ID to be vetoed
NO-VETO	101	current Bunch ID (12 bit) + Reserved (4 bits)	No bunch veto set
reserved	111		

Table 5 Bunch ID VETO command definition

Line 3 is to be AC-coupled on the FEE (see Section 5)

Line 4: FEE status

Line 4 allows the CC to see that the fast signal cable C is correctly plugged in and that FEEs are powered up.

The signal send is currently defined to be a continuous clock derived from the 99.31 MHz clock on Line 1. It was agreed to keep open the option of encoding information onto Line 4.

Line 4 is to be AC-coupled on the CC (see Section 5)

5 AC coupling

All four fast lines need to be AC-coupled. Lines 1,2 and 3 will be AC-coupled on the FEEs, line 4 will be AC-coupled on the CC.

The suggested default capacitive AC-coupling circuit is shown in Figure 2 below. This also requires a balanced signal to operate correctly, and simple Manchester coding (using the 99.31 MHz clock) is suggested for line 2 and 3 signals (and possibly for line 4 status if any encoded information is carried)

An alternative version of capacitive AC-coupling, Figure 3**, with feedback latching – which does not require balanced signals – is being investigated and will be tested. If this proves capable of working at our frequencies, it should be adopted instead**.

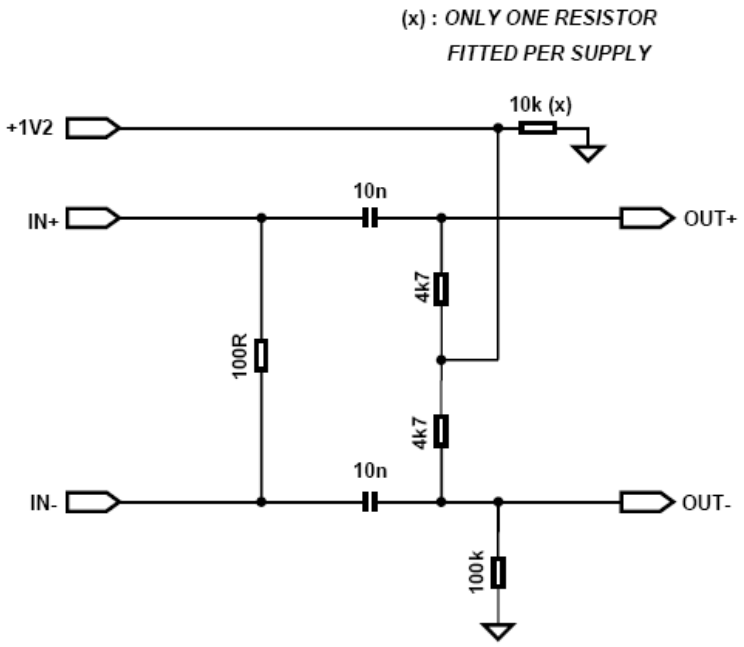

Figure 2 Suggested default AC coupling schematic

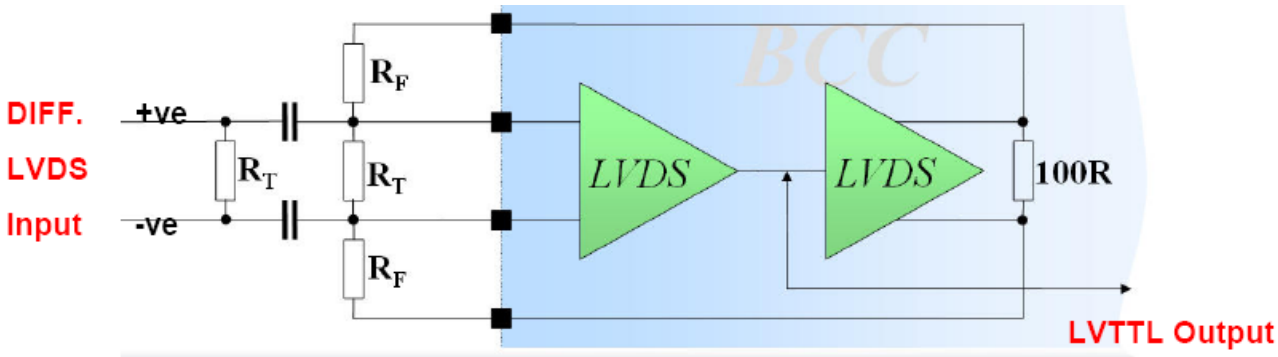

Figure 3 Alternative (preferred?) AC coupling solution

6 Grounding

The inputs from the TR board and from external inputs will have cable shielding (outer or individual twisted pair) connected directly to ground on CC via replaceable 0Ω surface mounted resistors.

Lines 1 though 4 will be grounded as follows: Any cable shielding (outer or individual twisted pair) is to be connected directly to ground on CC via replaceable 0Ω surface mounted resistors.

7 VETO and NOVETO protocol details

Details concerning the two VETO and NOVETO protocols defined are given in the following sub-sections. The protocols differ most significantly in the delay of the VETO signal; in one the delay is fixed w.r.t. the pulse being vetoed, in the other the delay is variable.

The Veto Management Unit will exist on a separate card next to the CC master or, if possible, using the existing hardware. In either case, multiple input connectors will be required. The number of connectors is determined by the number of Veto sources allowed.

Variable delay VETO protocol

Details of the variable delay VETO protocol, as seen by the FEE modules, are shown in Figure 4.

Messages are delivered at 99.31 Mbps and have encoded content: 3 command bits, 12 bunch number bits, and 4 reserved bits.

VETO messages arrive with varying delays (mT + Δt, where m = 0,1…) relative to the pulse being vetoed. NOVETO messages arrive with a fixed delay relative to the current pulse. In the schematic the fixed delay is Δt. The value of Δt is configured at the CC and applied to all VETO/NOVETO signals sent to the FEE modules.

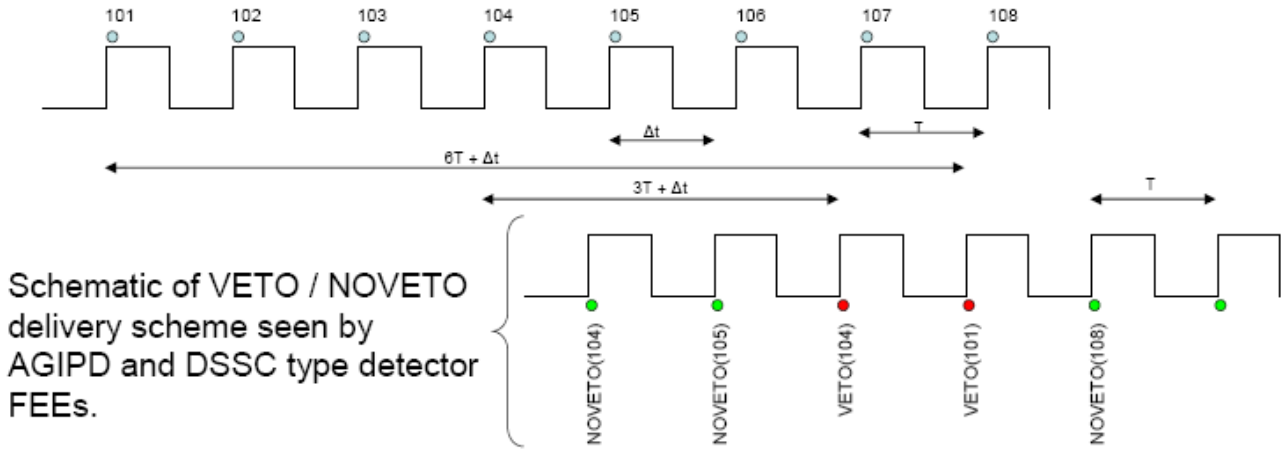

Figure 4 Variable delay VETO protocol

The following observations can be made:

- received bunch #s do NOT run from 1 to bunches-in-train in steps of 1.

- a given bunch # can be received twice (NOVETO then VETO), once (NOVETO or VETO), or never.
- a given bunch # cannot be vetoed twice.
- the bunch # of NOVETOs increases and marks the actual bunch counter
- the bunch # of VETOs is random (e.g. diagram: 104 proceeds 101)
- VETO delivery to the FEEs is pipelined by the CC. (e.g. VETOs 104 and 101 may have arrived at the CC in the same T period and have been delivered to the FEEs in consecutive T slots)
- the value of Δt is detector specific and configured and imposed at the CC
- VETO(104) means that FEE storage locations used by bunch # 104 can be reused
- receiving a NOVETO does not mean that the bunch # will never be vetoed (e.g. diagram: 104

Fixed delay VETO protocol

Details of the fixed delay VETO protocol, as seen by the FEE modules, are shown in Figure 5.

Messages can be either:

- A 4.51 MHz yes/no (e.g. 1 = accept, 0 = reject) clock, or
- the 100 MHz message as used by the variable delay VETO protocol.

The definition to be used is configuared at the CC.

VETO or NOVETO messages arrive with the same fixed delay relative to the pulse being vetoed or not vetoed, respectively. In this mode the VETOs and NOVETOs issued by the CC have a fixed latency, in the diagram above the fixed delay is 3T + Δt. The delay value is nT + Δt and is detector specific, applies to all FEE modules, and is configured and generated at the CC (n = 0,1…).

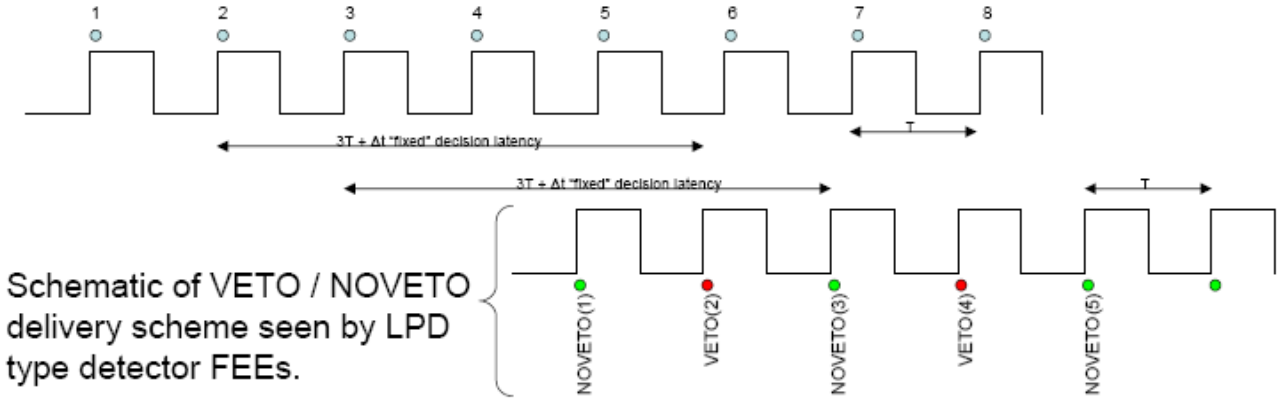

Figure 5 Fixed velay VETO protocol

The following observations can be made:

- For 99.31 MHz messages, the bunch # runs from 1 to bunches-in-train in steps of 1.
- For 99.31 MHz messages a given bunch # will be received only once.