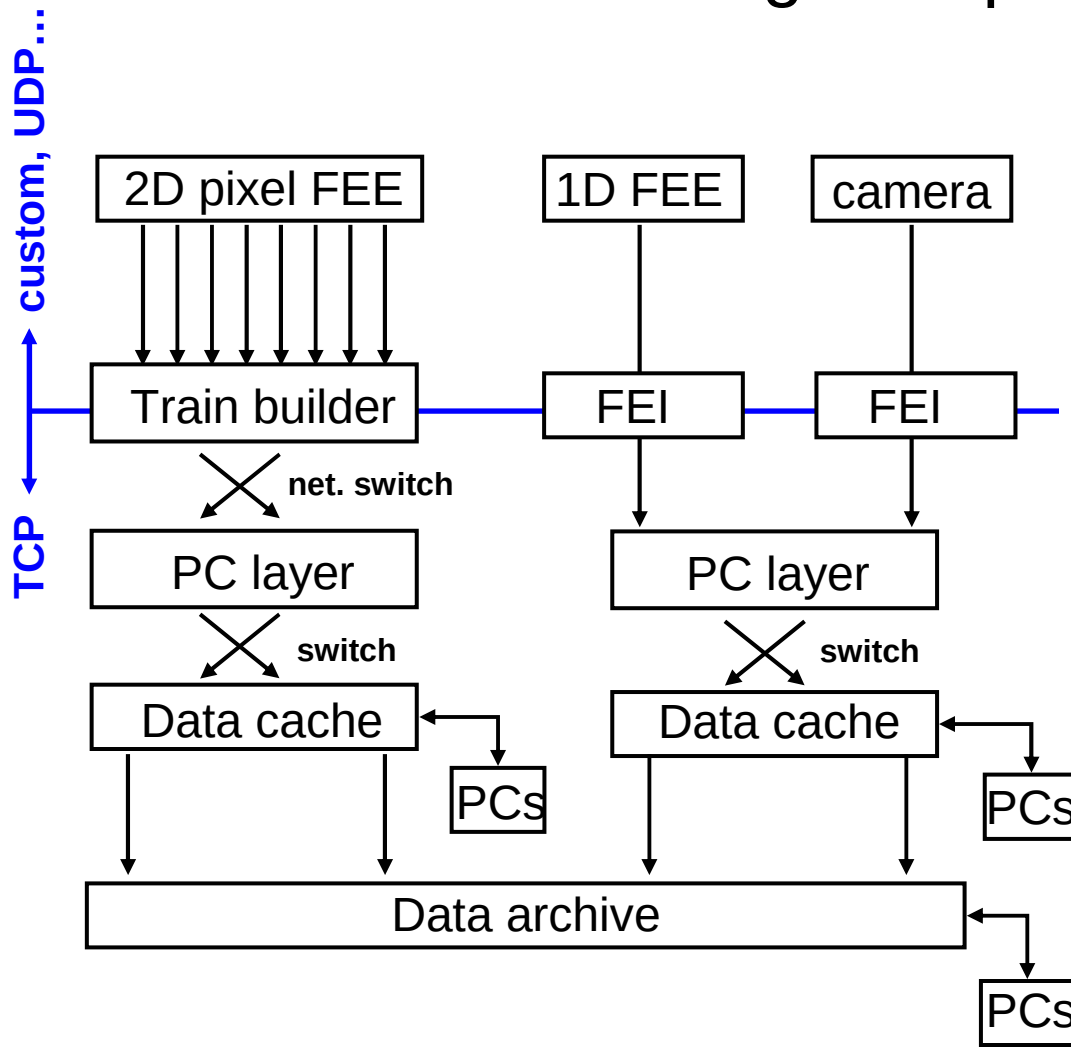
Common developments for HPAD

- Common developments, contents:
  - Readout architecture
    - Global picture
    - Train Builder (TB) status
    - With and without TB
  - Clock and control (C&C)
    - Introductory timing slides
    - XFEL timing system and experiment interface
    - proposed C&C system
  - Slow control (HV, LV, interlock, etc.)
    - Proposed system
  - Cost manpower summary for HPAD planning

Proposals should be discussed – ideally I want to buy some hardware this year.

XFEL readout the global picture (aim 9.2008)

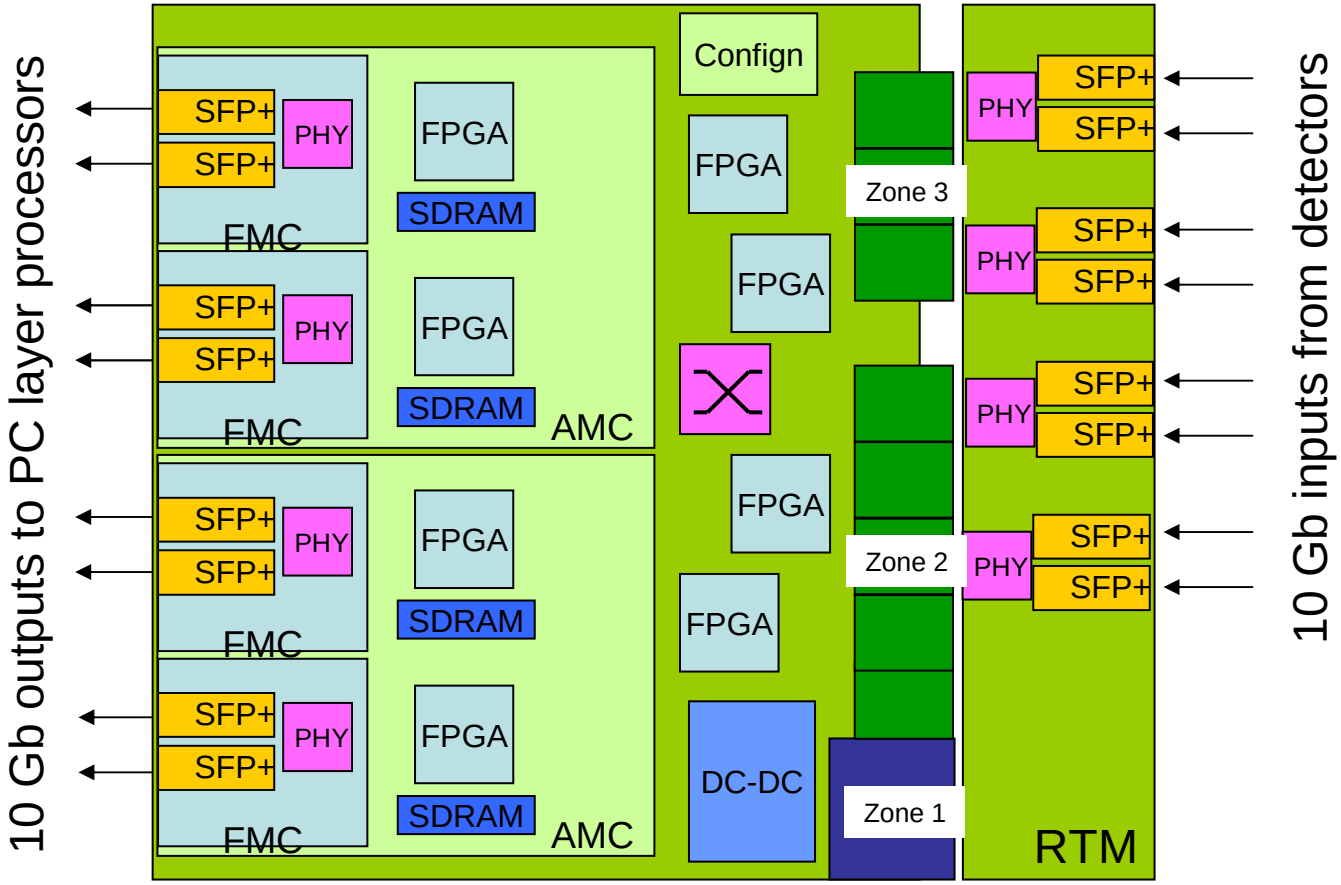


- 5 layers
  - Front End Electronics FEE
  - Front End Interface FEI
  - PC layer
  - Data cache (temporary)
  - Data archive (permanent)
- 2 data protocols
  - FEE to FEI = custom, UDP,…
  - FEI to data archive = TCP
  - Protocol conversion at FEI/TB
- Full bandwidth into cache
- Processing
  - TB (train building+reduction?)
  - PC layer (algo+rejection)
  - Data cache (algo+rejection using expt. downtime)
- Offline processing/access
  - Data archive

Train builder status

- Train builder functionality (being defined)
  - Protocol conversion = custom hardware-hardware input + TCP output
  - Train building = rebuilds and orders frames into single contiguous train
  - Processing = maybe pedestal correction, zero suppression, trigger sum counting
  - Implementation = currently ATCA + AMCs (i.e. ATCA crate)
- Project organization (being set up)
  - UK in kind contribution lead by STFC (RAL)
    - Overall design, main board, cross point switch, FPGA, ...
  - DESY – FEA (digital electronics group)
    - 10 Gb developments, possibly RTM layout and implementation
- Deliverables
  - ½ Mpixel boards = 2 boards per Mpixel detector (single Mpixel board impossible)
  - Test and diagnostic software
  - …
- Timescale = not fully defined, but compatible with HPAD rollout

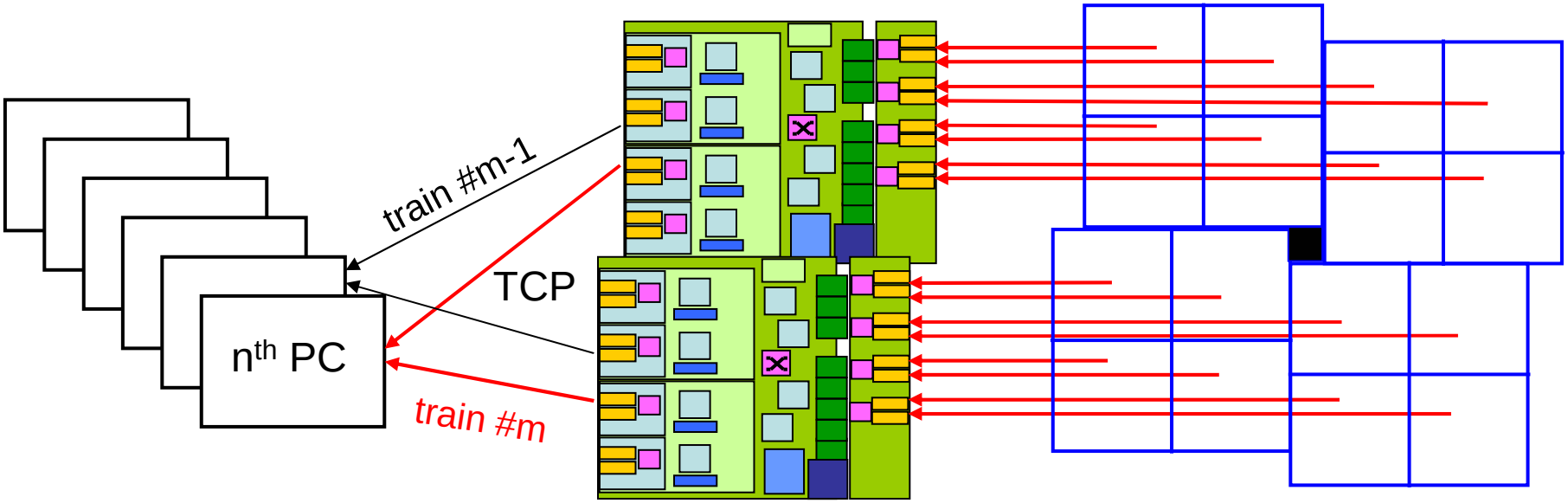
A ½ Mpixel TB ATCA implementation (J.Coughlan)



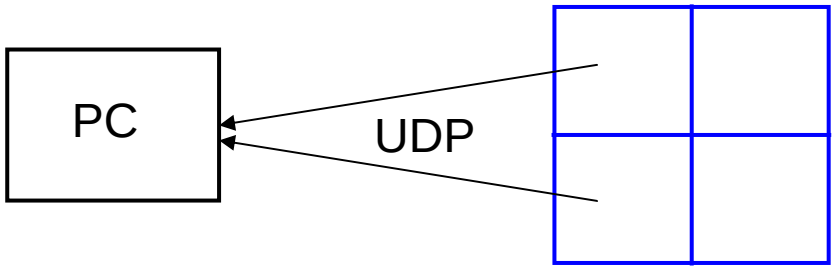
- Double width AMCs and FPGA mezzanine FMCs ease prototyping/development
  - Max. 512 frames (2B/pixel) in (8 inputs) at 10Hz, less at 30Hz; built train output 1 output
  - A single 1Mpixel board not possible: extreme bandwidth and component space requirements

With and without the TB

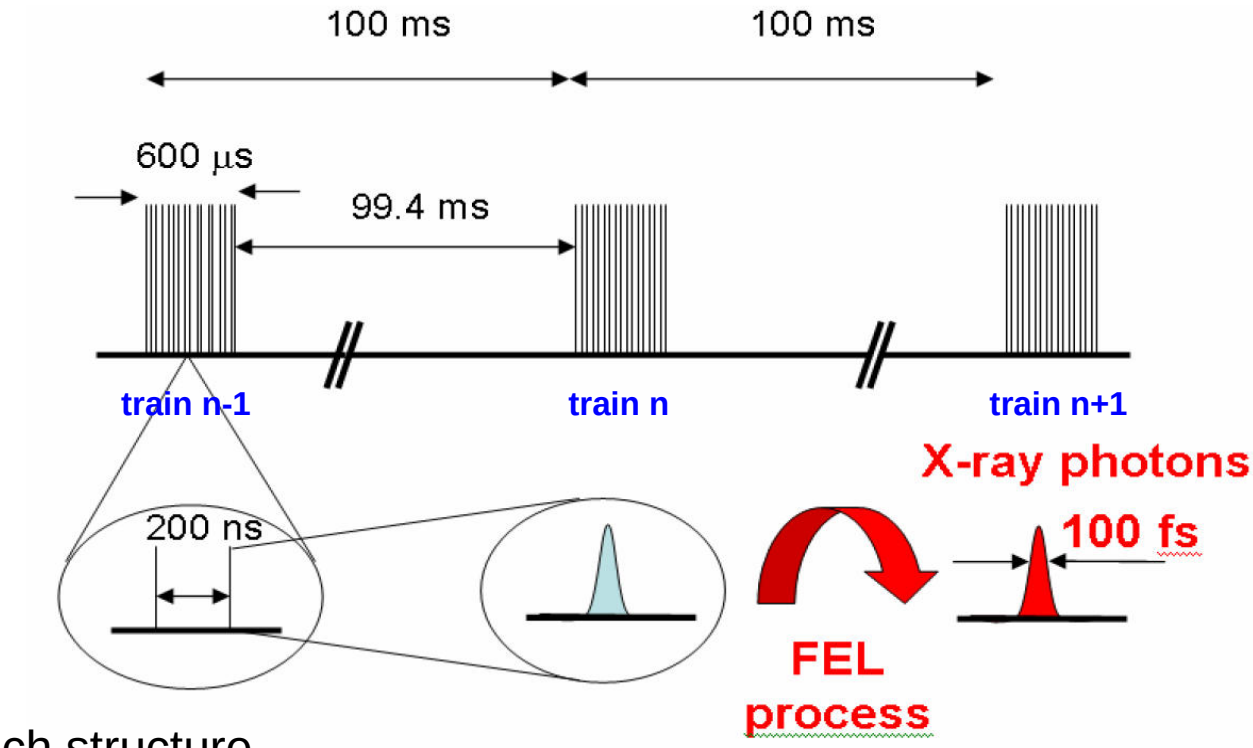
- With TB = 16 x detector readout interfaces + 2 x ½ Mpixel boards + N x PCs



- Without TB = 1 x PC + 1 x detector readout interfaces per NIC



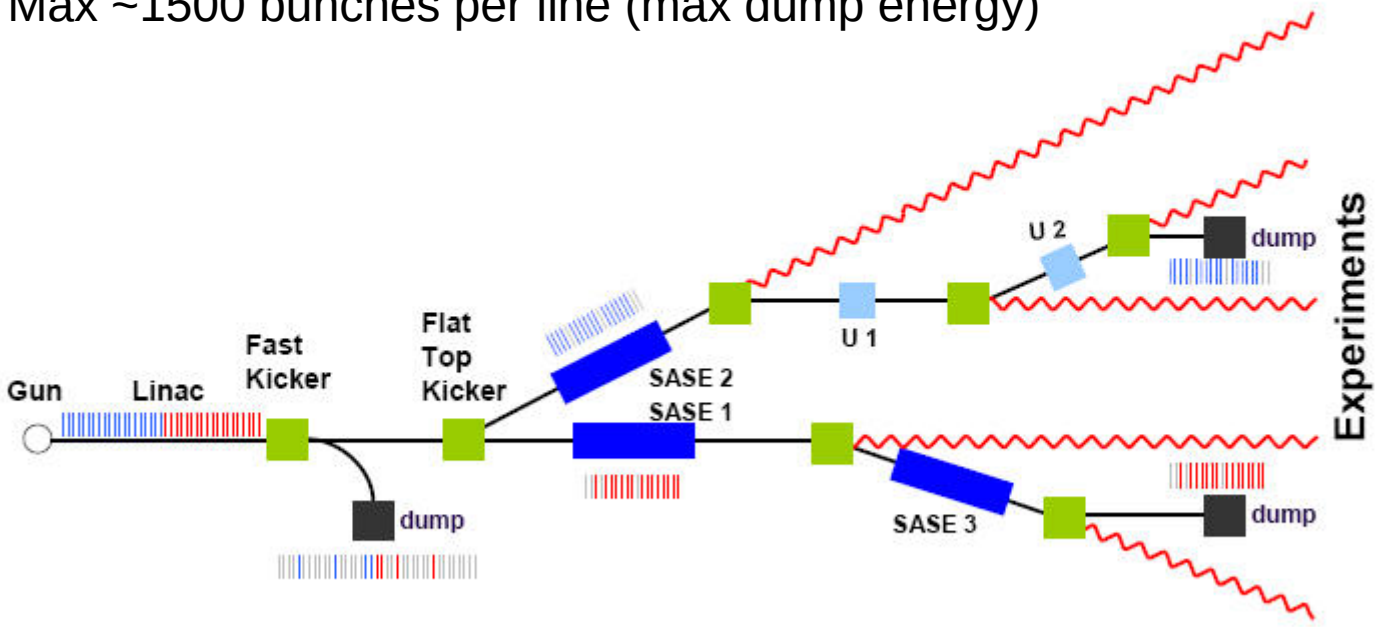
XFEL timing structure



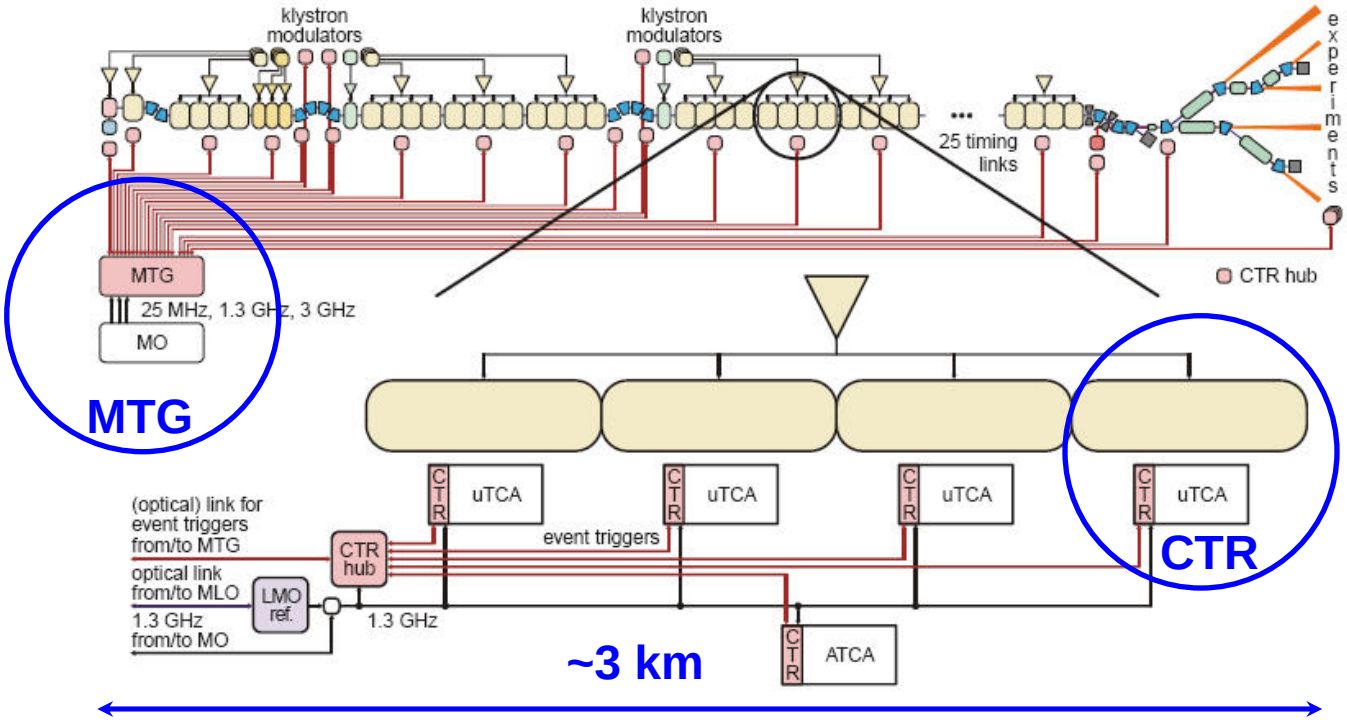
- Bunch structure
  - 10 Hz repetition rate, 30Hz option talked about.
  - 5 MHz e-bunch rate (200ns), variable
  - Fixed RF 600μs flat top = 3000 e-bunches
  - E_{beam} = 17.5 GeV, max = 22 GeV
  - Photon bunches produced when e-bunch pass FEL undulator

Beam distribution

- Beam lines
  - 5 beam lines planned, SASE 1,2+3 at XFEL startup (2013/4).
  - All lines receive photons concurrently (multiple reuse of e-beam)
  - 2-3 detectors per line (only one detector per line gets beam)
  - Flat top kicker splits e-beam, requires 20µs = 100 bunches (no dump)
  - Fast kicker removes single bunches (e.g. during flat top change)
  - Electron gun can generate any bunch pattern
  - Potentially different bunches in consecutive trains
  - Max ~1500 bunches per line (max dump energy)



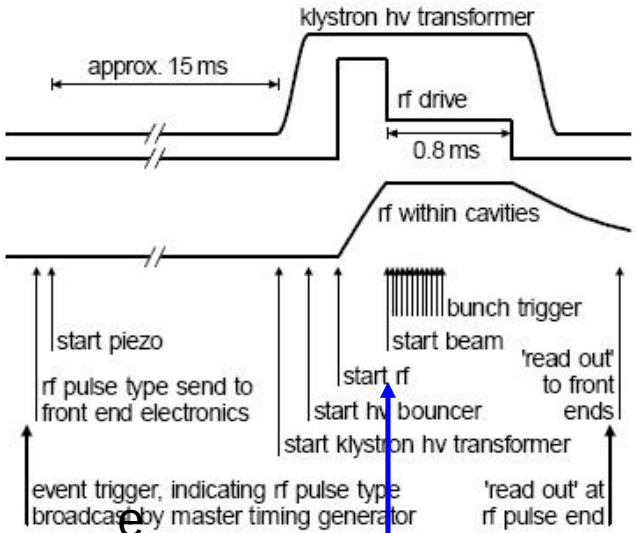
Timing signal generation and distribution



- Master Timing Generator (MTG) generates 25MHz, 1.3GHz, 3GHz
- MTG signals driven through fibre to Clock and Timing Relays (CTR)
- CTRs are used electron beam, but also in photon beam line for expts.
- Experiment's Timing receivers (TR) receive signals at the experiment
- By measuring round trip times and delay offsetting at the TRs triggers are generated with correct absolute time.
- Triggers must be sent advanced in time by > largest delay to CTR/TR

Timing Triggers and Events

Timing schematic of
e-machine RF events



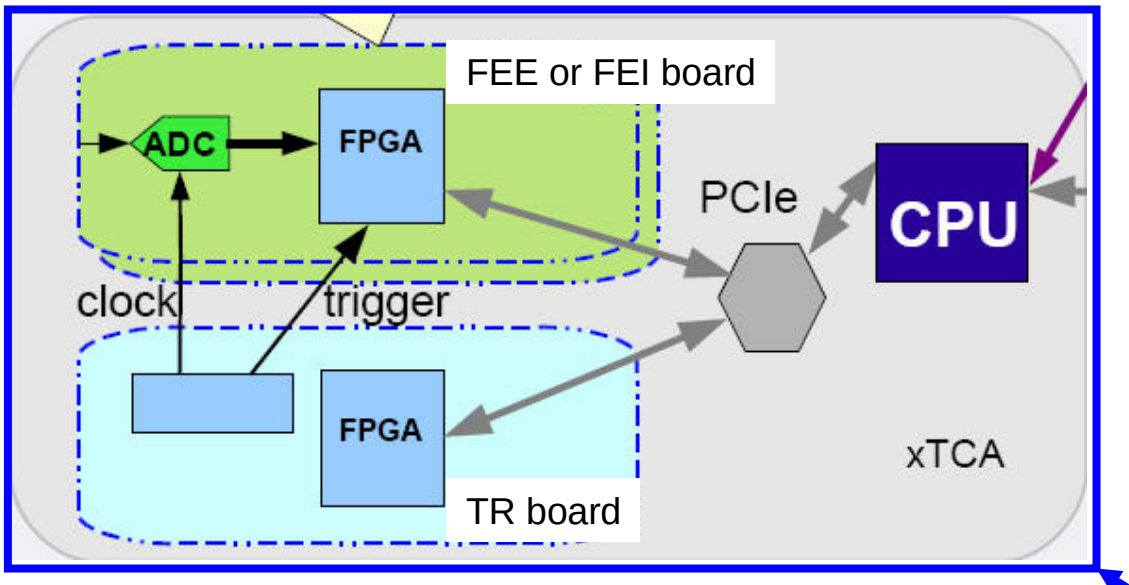
- The TR generates triggers and events
  - Trigger = a single pulse on an output connector
  - An event = Trigger + accompanying (telegram) data

Timing hardware implementation for XFEL

- Timing system development lead by K.Rehlich + in-kind Swedish contribution
- TR being implemented as an AMC board.
- Access to telegram data
  - Crate PC by PCIe backplane interrupt driven read
  - Crate DAQ board on LVDS line
  - NB. LAN distribution has been talked about, not favoured.
- Status
  - pre-prototype test of chipset stability done – results OK
  - prototype expect spring 2009

TR functionality schematic (K.Rehlich)

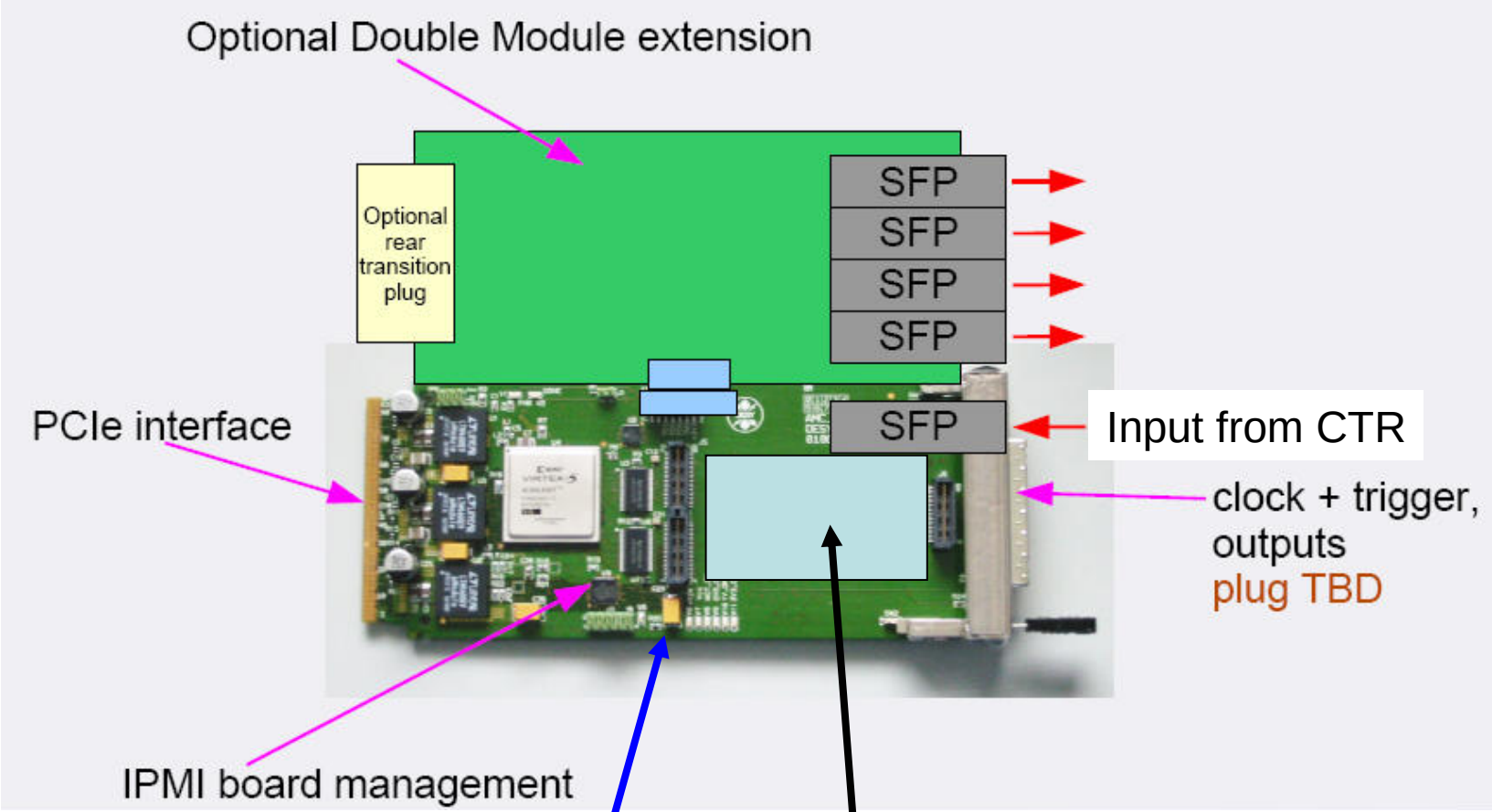
FEE or FEI:
Gets: clocks, triggers and events + telegrams (LVDS?: bunch occupancy pattern)



CPU:
Receives: interrupts
Reads: train number, modes,…
Writes: clocks (1.3MHz divider), delay offsets,…

Crate

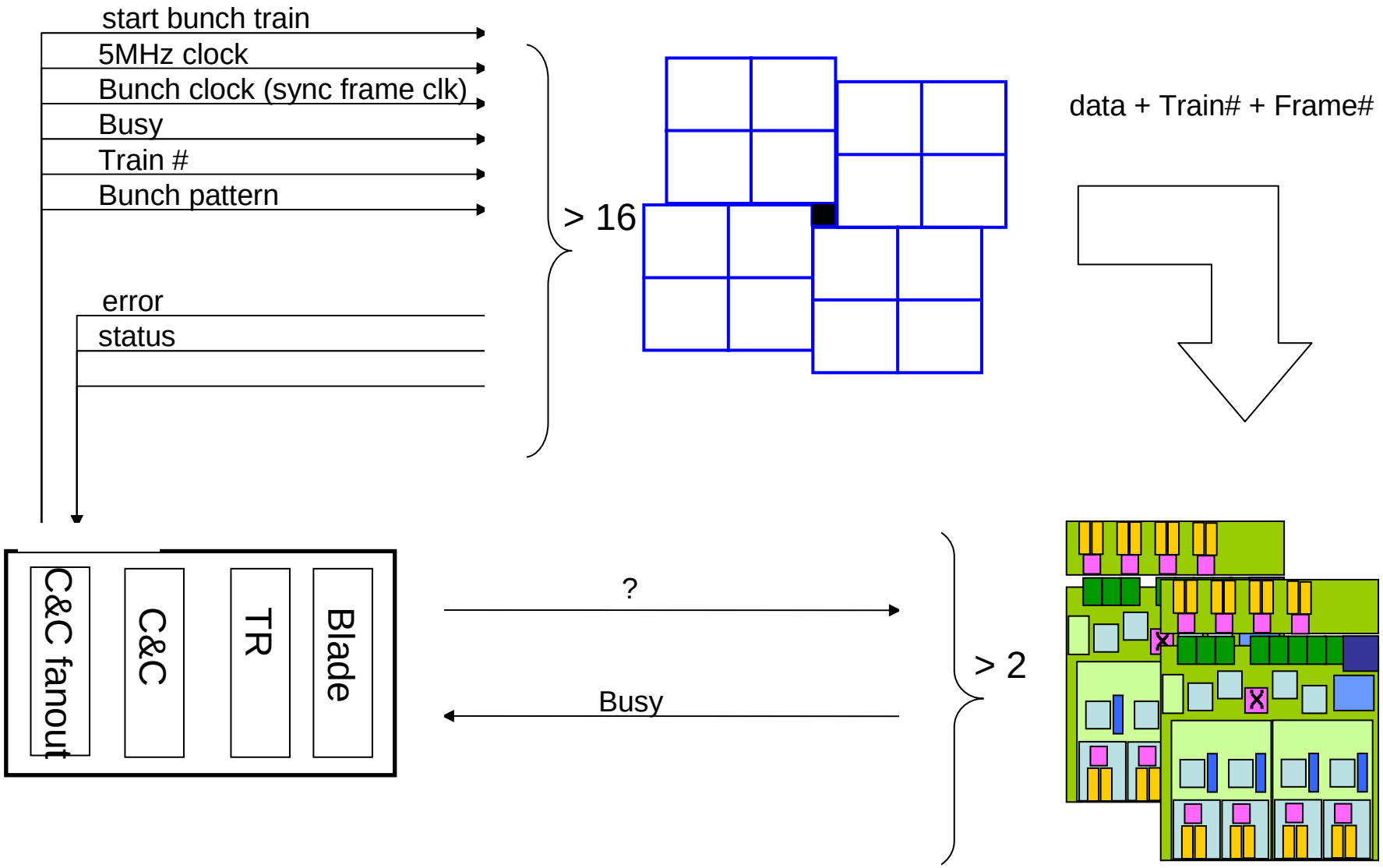
TR hardware implementation (K.Rehlich)



Proposed C&C system

- Functionality required
  - Interface to TR
  - Distribute (fanout) clocks and timing signals to FEE and TB
  - Receive (fanin) signals from FEE and TB
  - Standalone mode for running system when no timing input present, including bunch pattern generation (calibration …), etc.
  - Impose correct state of operation on control system
  - Foresee increase in detector size (replication)
- Project organization (being set up)
  - UK in kind contribution lead by UCL group
    - Overall design, hardware, test and diagnostic software
- Timescale = not fully defined, but compatible with HPAD rollout
- Open issues
  - Availability during detector prototyping phase
  - Support for operation at other light sources, e.g. LCLS, interface DAQ and timing
  - How to debug the entire system: FEE, C&C and TB
  - Here control and data paths are split (and DEPFET) ! Other solutions?

C&C signals and connections (complete?)



MVD slow control at ZEUS.

- Micro Vertex Detector slow control (PC+CANbus) at ZEUS
  - HV, LV
    - Controlled (configuration, on, off, …) and monitored by PC (each 512 channels)
  - Temperature, Humidity
    - Sensors monitored by PC (~100 channels)
  - Cooling
    - embedded PLD monitored: P, T, H, water pump, valves, ... (~10)
    - Controlled (on, off) and monitored by PC
    - warning and error thresholds settable from PC
    - if error switch off cooling and open alarm contact to interlock
  - Interlock
    - PLD/SPS monitored, inputs (cooling, switches, no control PC deadmans handle) close/open (OK/Alarm) OR'd. (~4)
    - Switch HV and LV crates off on alarm
  - Switches
    - Bimetal temp switches (4)
    - Emergency off switch (1)
- Pixel detectors may have additional requirements
  - Vacuum
    - assume controlled and monitored (P) by PC
    - assume Input into interlock

Type, size and number of subcomponents matches those of 1Mpixel detectors

HPAD slow control at XFEL

- Follow MVD implementation
  - Use TCP as field bus (instead of CANbus at MVD)
  - Use blade PC to monitor and control.
  - Independent interlock system (not part of cooling system which are often sold with such functionality) manually bridge inputs which are not required i.e. during testing phase.
  - Use similar FSM software to turn on/off system, allows “HV on only when LV on” type clauses.
  - Means that: cooling and vacuum systems need to provide open/close inputs to interlock when status OK/ALARM
- Software
  - Look at OPC over TCP for connections to components (must be linux)
  - Need control and monitoring functionality

Slow control

- Who is responsible for what
  - HV and LV = single common solution
  - Interlock = single common solution
  - Cooling = detector specific, but common sw and interlock APIs
  - Vacuum = detector specific, but common sw and interlock APIs
  - FEE sensors (temp, humidity, …) = detector specific, but common sw API. Could have interlock inputs but more likely to be sw.

- Unknowns
  - Non FEE sensors = could use common IO device, if needed.

- Manpower
  - MVD SC implementation took 1year:
    - 0.3 coordinators
    - 2 man team to build CANbus interface and program custom LV hardware from scratch
    - 1.5 programmers (interface to: HV Iseg, interlock, cooling, LV)
    - 0.25 electrical technician produce NIM&TTL to OPEN/CLOSE plus simple logic modules
  - 2D pixel
    - 1-2 FTEs of physicists programmer for selecting/testing and integrating COTS
    - If custom interlock, additional IO then ½ TFE elec. engineer required per component
    - Overall system integration ½ FTE programmer.

Example HV and LV implementation

- As and exercise
  - Asked for and received initial specification of HV+LV requirements
  - Looked at what was on the market
  - Looked at our requirements (floating, crate solutions, IP, etc.)
  - Asked principle HEP power supply manufacturers for implementations
    - ISEG/Wiener = MVD supplier = good experience w.r.t. modification, first release of ISEG hardware usually interesting, documentation interesting.
    - CAEN = usually more expensive
  - ISEG/Wiener solution suggestion received,
  - CAEN cannot provide a non radiation hard, non magnetic field inexpensive EASY crate based version available, may be later.

Initial HPAD HV+LV spec. sent to ISEG/Wiener and CAEN Aug 2008

Guesstimate of LV power supply requirements for 1Mpixel HPAD detector:

	Nr. channels	V range	I per channel	ID
ASIC	4	5 thru 8V	1A	A
	4	12 thru 14V	1A	B
	32	1.25 thru 2.5V	40A	C
	32	2.5 thru 3.5V	10A	D
Analogue	16	-1 thru -2.5V	1.6A	E
	16	1.8 thru 3V	4.5A	F
	16	5 thru 8V	2A	G
Digital	16	1 thru 5V	20A	H
	16	1 thru 5V	20A	I

Guesstimate of HV power supply requirements for 1Mpixel HPAD detector:

	Nr. channels	V range	I per channel	ID
Sensors	16	0 thru -600V	few mA	K

Answer from ISEG/Wiener – MPOD ≤ 10A chans, MDH+PL > 10A chans

MPOD modules	Number	Single price	Total price	IDs used
MPV 8015	1	1765	1765	A
MPV 8008	8	1613	12904	B+F+G
MPV 8008n	2	1613	3226	E
1EHS F010n_805	1	3380	3380	K

MPOD crates	Number	Single price	Total price	
MPOD EC-LV	1	3600	3600	B+E+F+G
MPOD Mini HV	1	2790	2790	K+A

modules	Number	Single price	Total price	IDs used
MDH	32	670	21440	C+H+I

crates	Number	Single price	Total price	
PL512	5	2600	13000	
PL 508 EX	1	1900	1900	

Grand total price 64005

Better is 6xPL512 rather than 5+PL508

Better is 2xMPOD EC-R rather than 2 different MPOD crates

Iseg/Wiener MPOD

MPOD is a crate containing LV and HV power modules.

HV = ISEG (internally CANbus)
LV = Wiener (USB)

Plus a network interface.

Note that PLxxx are crate supplies for Wiener LV modules only.

MPOD only if 20 and 40A channels are treated as an increased nr. of 10A chans

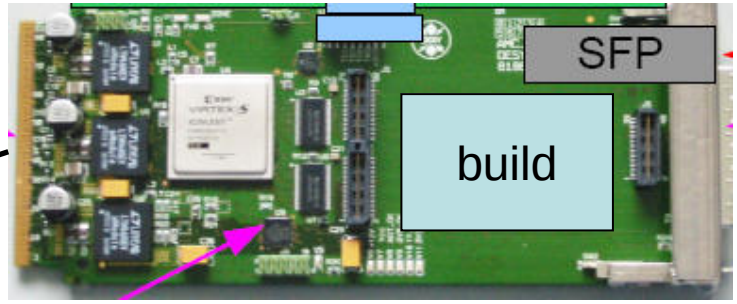
MPOD modules	Number	Single price	Total price	IDs used
MPV 8015	1	1765	1765	A
MPV 8008	8+8+16=32	1613	51616	B+F+G
MPV 8008n	2	1613	3226	E
1EHS F010n_805	1	3380	3380	K

MPOD crates	Number	Single price	Total price	
MPOD EC-LV	4	3600	14400	…
MPOD Mini HV	1	2790	2790	K+

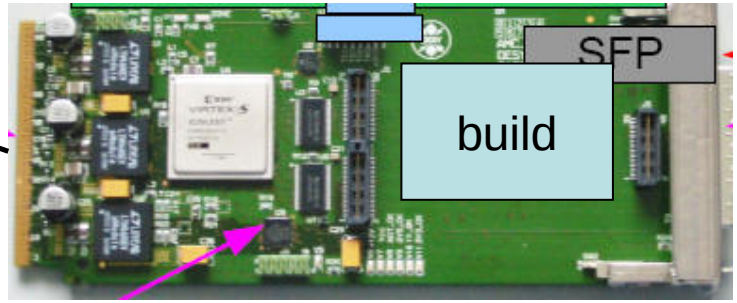
Grand total price 77177

The MPOD only solution costs 13000 € more

A slow control implementation



Open/close inputs
(vacuum, cooling,...)



Additional sensors

Interlock

More IO

C&C fanout

C&C

TR

Blade

LAN to
HV+LV crates

Cooling & vacuum??

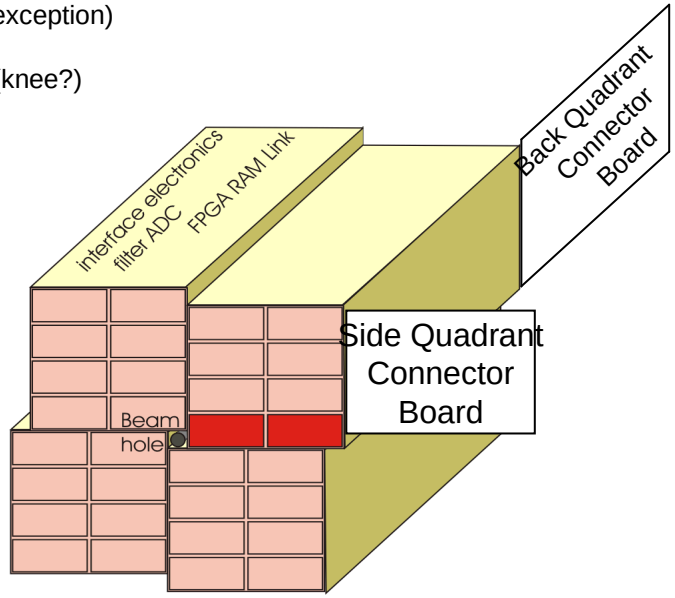
Cost and manpower summary crate side systems

- This of course is a ballpark estimate for a 1Mpixel detector

What	Price	Who pays	manpower	software
C&C crate + Hub	4000	?	0	0
Blade PC + disk	1500	?	0	0
TR	Free?	Free?	0	0
C&C + fanout …	In-kind	In-kind	In-kind	In-kind
TB	In-kind	In-kind	In-kind	In-kind
Interlock	?	?	½ FTE	¼ FTE
IO	?	?	½ FTE	¼ FTE
LV+HV	80000	HPAD	0	½ FTE
Cooling	?	?	?	?
Vacuum	?	?	?	?

Spare slides

Sensor HV (values from deliverable example EHQ F005x_106):
- 32 HV channels (1cable per sensor)
- other guard ring voltages needed?
- Vmax = 500V (might be +ve or -ve)
- ΔV settable/readable = 10mV
- Imax = 10mA (sensor = 200 μA i.e. no rad. leakage current)
- ΔI readable = 200nA
- ΔI trip settable = ?
- Safety loop (ramp down on exception)
- Vripple ≤10mV
- V ramp speed = ? settable (knee?)
- 16 channels per board
- crate based supplies
- cable connects at SQCB
- V output floating
- needed for DQM and control



Switches:
- Bimetal strip switches into interlock – needed/where?
- Emergency off switch into interlock.
- needed for DQM and interlock

Indicators:
- LEDs on boards when power ON
- Flashing lights like “magnets on”

Quadrant microProc:
- TCP receives next train setup information and distributes to FEE
- Readout temperature and humidity sensors? (anything else?)
- needed for DQM and control (via TCP)

ASIC, ADC and interface LV (MPV 80XX series 50A/board):
- ?? LV channels
- Polarity/Voltages/Currents required: +?V/?A, -?V/?A
- V, I, limits, ramps, etc. settable
- V ripple ≤10mV
- Large currents (250A/quad)
- 2 crate needed, if 10A/50W per channel - check?
- safety loop ?
- cable connects at SQCB (ASIC) and BQCB (ADC + interface)
- needed for DQM, control

Interlock:
-Inputs open/close = OK/alarm
- ?? Input channels
- interlock (cooling, HV and LV, …) so that if:
  cooling fails, or
  temperature outside limits, or
  humidity outside limits, or
  emergency off switch, or
  watchdog failed, or
  slow control software off
  then HV and LV are powered off.
- PLD or SPS system required, must be independent all other PLD
- other conditions: HV on only if LV on, etc (at interlock or software).
- needed for DQM (all input states) and control

Humidity:
- ?? channels
- where are they and who reads them out – microProc
- needed for DQM

Temperature:
- at least 32 channels
- where are they and who reads them out – microProc
- values readout every train store in TINE and data archive
- needed for DQM and interlock.

Cooling:
- Environmental parameters (P, T, H …)
- needed for DQM, control (warning & error limits) and interlock

Vacuum pump:
- ?? Channels (P)
- needed for DQM, control and interlock

Peter's 31.7.2008 guesstimate of quadrant power supply requirements
= initial specification

	Nr. channels	V range	I per channel
ASIC	1	5 thru 8V	1A
	1	12 thru 14V	1A
	8	1.25 thru 2.5V	40A
	8	2.5 thru 3.5V	10A
Analogue	4	-1 thru -2.5V	1.6A
	4	1.8 thru 3V	4.5A
	4	5 thru 8V	2A
Digital	4	1 thru 5V	20A
	4	1 thru 5V	20A

Guesstimate of quadrant sensor power supply requirements
= initial specification

	Nr. channels	V range	I per channel
Sensors	8	0 thru -600V	few mA
Guards	0	-	-