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| **FEE, TB and CC FPGA Meeting**  Wednesday, 19th October 2011  Patrick Gessler |
| **Present** |
| J. Coughlan, B. Fernandes, T. Gerlach, P. Gessler, P. Goettlicher, R. Halsall, E. Motuk, C. Youngman |
| **Next Meeting** |
| **9th November 2011, 11:00 CET** |
| **Open Points** |
| **None** |
| **Minutes** |
| 1. **Organizational things**  * A special mailing list will be prepared * The next meeting will take place on 9th November and from then on every two weeks  1. **Update of CC**  * On one of the RTM boards was a short circuit on the DC/DC converter * An external DC/DC converter was used for testing after unmounting the original one * A problem with a capacitor had been found, which lead to disconnection of 12V from DAMC2 board after a short time -> has to be checked if this has to be fixed on the DAMC2 or RTM * The clock chain with local oscillator till 99MHz was tested and worked * CC system is not that urgent for LPD as they can use the prototype system * Patrick will push timing fw development for stand-alone board for tests  1. **Clock and Control for DSSC**  * ADC input jitter has to be lower than 2.5ps @ 800MHz (comment from Carsten) * Has to be cleaned with local PLL * The currently used PLL was tested and provided the same jitter performance independly of a high or low input jitter * However, the jitter on the 99MHz reference clock should be as low as possible * The jitter of this clock should be measured * Middle of November should be a RTM and DAMC2 available for T. Gerlach for tests  1. **AoB**  * none |
| **Decisions and actions** |
| * Prepare mailing list (Patrick) * Send latest/final MTCA.4 specs to Erdem (Patrick) * Checking of capacitor requirements in MTCA.4 specification (Erdem) * Prepare more RTMs if no problem found (Erdem) * Test jitter test results from CC as well documentation should be put on the FPGA wiki (Erdem) |
| **Topics on Hold** |
| * Redesign/changes on CC RTM could wait till Summer 2012 |