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| **FEE, TB and CC FPGA Meeting** Wednesday, 30th November 2011Patrick Gessler |
| **Present** |
| J. Coughlan, T. Gerlach, P. Gessler, A. Koch, E. Motuk |
| **Next Meeting** |
| **21st December 2011, 11:00 CET** |
| **Open Points**  |
| * **Collect final change request for DAMC2**
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| **Minutes** |
| 1. **VETO specification**
* The document is not ready yet
* It will be sent around before the TB and CC meeting next week
1. **DAMC2 and RTM production**
* The RTM from the recent production are ready and tested for use in Heidelberg
* DAMC2 production delayed, as still waiting for the final three required offers
* We will use an existing board for the tests at DSSC
* Besides the DAMC2 and RTM also a uTCA crate, evtl. a timing receiver and CPU is required for the tests
* A system will be prepared till next week TB and CC meeting to be taken to Heidelberg
* Thomas will come already on Tuesday evening to join the measurements on Wednesday next week
1. **Workshop on 10G/40G Ethernet**
* Within the European CRISP project, where XFEL is participating other labs face similar tasks we have like high data rate transmission
* As 10G and in the future 40G Ethernet is a common option we had the idea of having a workshop around end of January on this topic
* It will be most likely EVO based
* Further details will be discussed and defined in the next weeks
1. **CC update**
* A working timing receiver as stand-alone version would be very helpful for the realistic measurements and tests
* Patrick is pushing it to be available for the tests next week at XFEL
* However, the final performance won’t be available, as the switch in the central MCH in the uTCA crate still uses FPGAs so a degradation of the performance is expected
* The manufacturer of the MCH (N.A.T.) will build first prototypes of a low jitter implementation of the switch based on ASICs beginning of next year
* Also the 4.5MHz clock coming from the timing receiver will be generated locally and not recovered from the actual timing stream along the accelerator 🡪 the final performance might be different
1. **DSSC update**
* Board is there
* Clock tests had been done
* A small meeting related to VETO yesterday: fixed max. latency to 128 bunches
1. **LPD, TB update**
* Things took longer than expected
* Will be reported next week at the TB and CC meeting
1. **AoB**
* none
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| **Decisions and actions** |
| * Preparation for measurements at XFEL (Patrick)
* Measurements of jitter performance CC (Erdem, Thomas, Patrick)
* Pushing stand-alone version of timing receiver (Patrick/Erdem)
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| **Topics on Hold** |
| * Redesign/changes on CC RTM could wait till Summer 2012
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