



# 16-Port, Bi-directional LVDS Clock Cross-Point Switch

**IDT8V54816I**

## ADVANCE INFORMATION DATA SHEET

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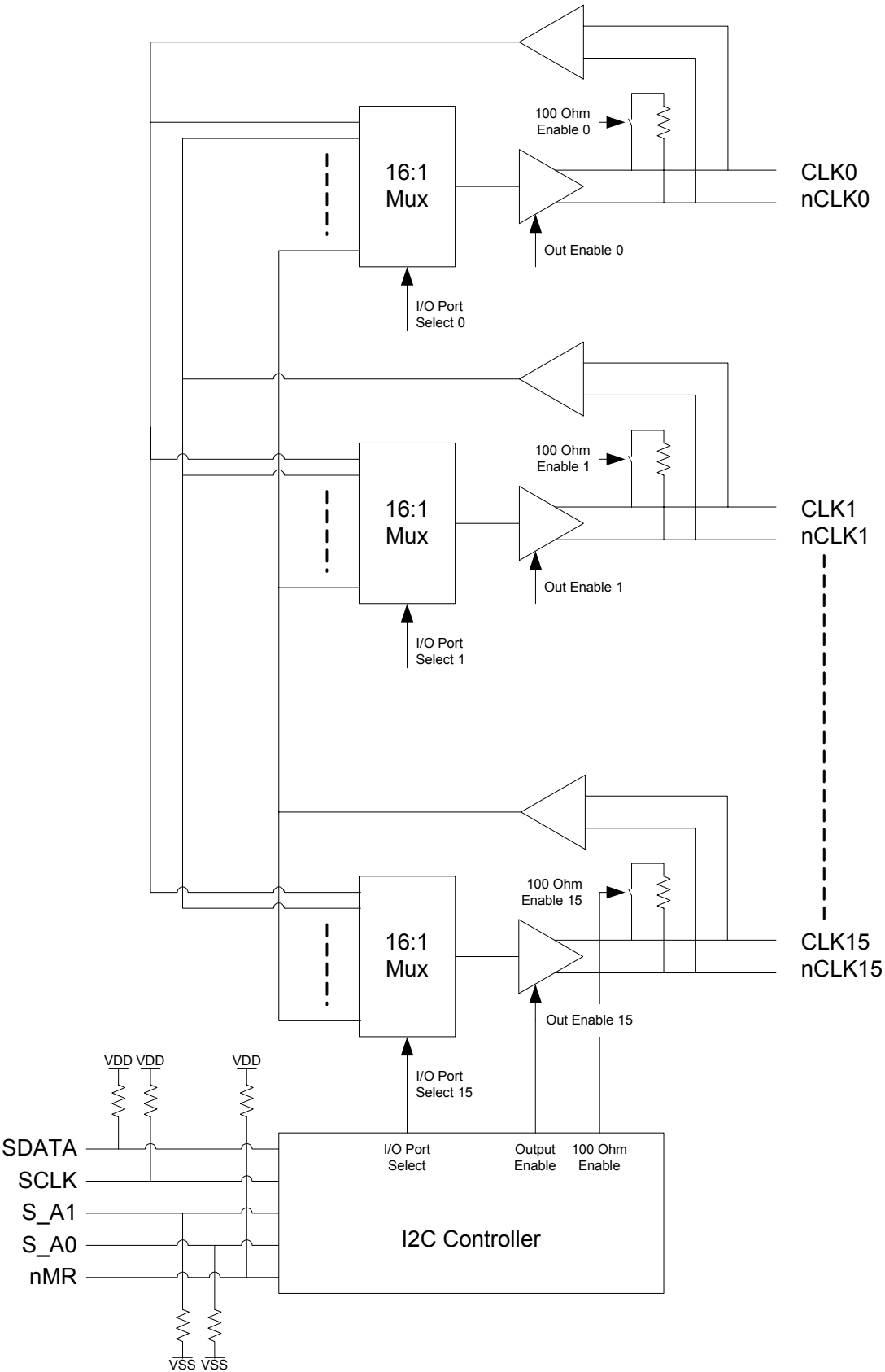
### General Description

The IDT5V54816I is a 16-port, bi-directional cross-point clock switch designed for clock distribution in MicroTCA.4 systems. It features 16 bi-directional LVDS ports. Each port can be individually set as input or output. Each output port can be connected to any port defined as input. Each port features switchable termination (ON: 100Ω, OFF: High impedance). Output ports can drive up to 19-inch PCB tracks with M-LVDS levels. The device is optimized for very low additive phase noise and cycle-to-cycle jitter. Configuration of the device is achieved by I<sup>2</sup>C. At startup, a default configuration is set where all ports are in High-Impedance mode with outputs disabled.

### Features

- Sixteen bi-directional LVDS ports
- Operating frequency: 1MHz to 650MHz
- Switchable termination resistors
- I<sup>2</sup>C support with read-back capabilities up to 400kHz
- PCI Express Gen2 and Serial Rapid IO 2.0 Jitter Compliant
- Compliant with MicroTCA.4 specification
- Output polarity inversion
- Full 3.3V supply voltage
- 12mm x 12mm x 0.65mm 100-lead VFQFN
- E-Pad size: 6.9mm x 6.9mm
- -40°C to +85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

Block Diagram





## Pin Descriptions & Characteristics

Table 1. Pin Description Table

Number	Name	Type		Description
1, 4, 50, 74, 75, 76, 98, 100	V <sub>DD</sub>	Power		Power supply pins.
2, 3, 24, 48, 73, 77	GND	Power		Power supply ground.
5	V <sub>DDO_CLK0</sub>	Power		Port 0 output power supply.
6, 7	CLK0, nCLK0	I/O		Bi-directional clock port 0.
8	GNDO_CLK0	Power		Port 0 power supply ground.
9	V <sub>DDO_CLK1</sub>	Power		Port 1 output power supply.
10, 11	CLK1, nCLK1	I/O		Bi-directional clock port 1.
12	GNDO_CLK1	Power		Port 1 power supply ground.
13, 27, 38, 49, 63, 79, 88, 97	nc	Unused		Do not connect.
14	V <sub>DDO_CLK2</sub>	Power		Port 2 output power supply.
15, 16	CLK2, nCLK2	I/O		Bi-directional clock port 2.
17	GNDO_CLK2	Power		Port 2 power supply ground.
18	V <sub>DDO_CLK3</sub>	Power		Port 3 output power supply.
19, 20	CLK3, nCLK3	I/O		Bi-directional clock port 3.
21	GNDO_CLK3	Power		Port 3 power supply ground.
22	nMR	Input		Master reset. Active Low. LVCMOS/LVTTL interface levels.
23, 28, 53	V <sub>DD_DIGITAL</sub>	Power		Digital power supply pins.
25	SCLK	Input	Pullup	I <sup>2</sup> C compatible SCLK. This pin has an internal pullup resistor. LVCMOS/LVTTL interface levels.
26	SDATA	I/O	Pullup	I <sup>2</sup> C compatible SDATA. This pin has an internal pullup resistor. LVCMOS/LVTTL interface levels.
29, 54	GND_DIGITAL	Power		Digital power supply ground.
30	V <sub>DDO_CLK4</sub>	Power		Port 4 output power supply.
31, 32	CLK4, nCLK4	I/O		Bi-directional clock port 4.
33	GNDO_CLK4	Power		Port 4 power supply ground.
34	V <sub>DDO_CLK5</sub>	Power		Port 5 output power supply.
35, 36	CLK5, nCLK5	I/O		Bi-directional clock port 5.
37	GNDO_CLK5	Power		Port 5 power supply ground.
39	V <sub>DDO_CLK6</sub>	Power		Port 6 output power supply.
40, 41	CLK6, nCLK6	I/O		Bi-directional clock port 6.
42	GNDO_CLK6	Power		Port 6 power supply ground.
43	V <sub>DDO_CLK7</sub>	Power		Port 7 output power supply.
44, 45	CLK7, nCLK7	I/O		Bi-directional clock port 7.
46	GNDO_CLK7	Power		Port 7 power supply ground.
47, 72, 78, 99	GND_S	Power		Power supply ground.
51	S_A0	Input	Pulldown	I <sup>2</sup> C address bit 0. LVCMOS/LVTTL interface levels.
52	S_A1	Input	Pulldown	I <sup>2</sup> C address bit 1. LVCMOS/LVTTL interface levels.
55	V <sub>DDO_CLK8</sub>	Power		Port 8 output power supply.
56, 57	CLK8, nCLK8	I/O		Bi-directional clock port 8.
58	GNDO_CLK8	Power		Port 8 power supply ground.
59	V <sub>DDO_CLK9</sub>	Power		Port 9 output power supply.

Number	Name	Type	Description
60, 61	CLK9, nCLK9	I/O	Bi-directional clock port 9.
62	GNDO_CLK9	Power	Port 9 power supply ground.
64	V <sub>DDO_CLK10</sub>	Power	Port 10 output power supply.
65, 66	CLK10, nCLK10	I/O	Bi-directional clock port 10.
67	GNDO_CLK10	Power	Port 10 power supply ground.
68	V <sub>DDO_CLK11</sub>	Power	Port 11 output power supply.
69, 70	CLK11, nCLK11	I/O	Bi-directional clock port 11.
71	GNDO_CLK11	Power	Port 11 power supply ground.
80	V <sub>DDO_CLK12</sub>	Power	Port 12 output power supply.
81, 82	CLK12, nCLK12	I/O	Bi-directional clock port 12.
83	GNDO_CLK12	Power	Port 12 power supply ground.
84	V <sub>DDO_CLK13</sub>	Power	Port 13 output power supply.
85, 86	CLK13, nCLK13	I/O	Bi-directional clock port 13.
87	GNDO_CLK13	Power	Port 13 power supply ground.
89	V <sub>DDO_CLK14</sub>	Power	Port 14 output power supply.
90, 91	CLK14, nCLK14	I/O	Bi-directional clock port 14.
92	GNDO_CLK14	Power	Port 14 power supply ground.
93	V <sub>DDO_CLK15</sub>	Power	Port 15 output power supply.
94, 95	CLK15, nCLK15	I/O	Bi-directional clock port 15.
96	GNDO_CLK15	Power	Port 15 power supply ground.

NOTE: *Pullup*, *Pulldown* refers to internal input resistors. See Table 2, *Pin Characteristics*, for typical values.

**Table 2. Pin Characteristics Table**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C <sub>IN</sub>	Input Capacitance			4		pF
R <sub>PULLUP</sub>	Input Pullup Resistor			51		kΩ
R <sub>PULLDOWN</sub>	Input Pulldown Resistor			51		kΩ

## Serial Interface Configuration Description

The IDT8V54816I has an I<sup>2</sup>C-compatible configuration interface to access any of the internal registers (Table 3A) for frequency and PLL parameter programming. The IDT8V54816I acts as a slave device on the I<sup>2</sup>C bus and has the address 0b10110xx, where xx is set by the values on the S\_A0 & S\_A1 pins (see Table 3B for details). Data bytes (registers) are accessed in sequential order from the lowest to the highest byte (most significant bit first, see Table 3D, 3E). Read

and write block transfers are not supported. It is recommended to terminate I<sup>2</sup>C the read or write transfer after accessing byte #15.

For full electrical I<sup>2</sup>C compliance, it is recommended to use external pull-up resistors for SDATA and SCLK. The internal pull-up resistors have a size of 50k $\Omega$  typical.

**Table 3A. I<sup>2</sup>C Address**

1	0	1	1	0	S_A1	S_A0	R/W
---	---	---	---	---	------	------	-----

**Table 3B. I<sup>2</sup>C Register Map**

Register	Binary Register Address	Function
0	0x00	Port 0 configuration
1	0x01	Port 1 configuration
2	0x02	Port 2 configuration
3	0x03	Port 3 configuration
4	0x04	Port 4 configuration
5	0x05	Port 5 configuration
6	0x06	Port 6 configuration
7	0x07	Port 7 configuration
8	0x08	Port 8 configuration
9	0x09	Port 9 configuration
10	0x0A	Port 10 configuration
11	0x0B	Port 11 configuration
12	0x0C	Port 12 configuration
13	0x0D	Port 13 configuration
14	0x0E	Port 14 configuration
15	0x0F	Port 15 configuration

**Table 3C. Control Bit Table**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
<b>Description</b>	Port I/O Configuration	Termination Enable	Polarity of Differential Interface	Reserved	Output Port Select [3]	Output Port Select[2]	Output Port Select [1]	Output Port Select [0]
<b>Function if Bit = 0</b>	Port Configured as Input	Termination Off (High-Impedance)	Non-inverted Polarity		Port outputs the signal present at port defined by Bits[3:0]			
<b>Function if Bit = 1</b>	Port Configured as Output	Termination Enabled	Inverted Polarity					
<b>Startup Condition</b>	0	0	0	0	0	0	0	0

## Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, $V_{DD}$	3.63V
Inputs, $V_I$	-0.5V to $V_{DD} + 0.5V$
Outputs, $I_O$ Continuous Current Surge Current	10mA 15mA
Package Thermal Impedance, $\theta_{JA}$	22.9°C/W (0 mps)
Storage Temperature, $T_{STG}$	-65°C to 150°C

## DC Electrical Characteristics

**Table 4A. Power Supply DC Characteristics,  $V_{DD} = V_{DD\_DIGITAL} = V_{DDO\_X} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DD}$	Power Supply Voltage		3.135	3.3	3.465	V
$V_{DD\_DIGITAL}$	Digital Supply Voltage		3.135	3.3	3.465	V
$V_{DDO\_X}$	Output Supply Voltage		3.135	3.3	3.465	V
$I_{DD}$	Power Supply Current					mA
$I_{DD\_DIGITAL}$	Digital Supply Current					mA
$I_{DDO\_X}$	Output Supply Current					mA

NOTE:  $V_{DDO\_X}$  denotes  $V_{DDO\_X[0:15]}$ .

**Table 4B. LVCMOS/LVTTL DC Characteristics,  $V_{DD} = V_{DD\_DIGITAL} = V_{DDO\_X} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage		2		$V_{DD} + 0.3$	V
$V_{IL}$	Input Low Voltage		-0.3		0.8	V
$I_{IH}$	Input High Current	S_A0, S_A1	$V_{DD} = V_{IN} = 3.465V$		150	$\mu A$
		nMR, SCLK, SDATA	$V_{DD} = V_{IN} = 3.465V$		5	$\mu A$
$I_{IL}$	Input Low Current	S_A0, S_A1	$V_{DD} = 3.465V, V_{IN} = 0V$	-5		$\mu A$
		nMR, SCLK, SDATA	$V_{DD} = 3.465V, V_{IN} = 0V$	-150		$\mu A$

NOTE:  $V_{DDO\_X}$  denotes  $V_{DDO\_X[0:15]}$ .

**Table 4C. M-LVDS DC Characteristics,  $V_{DD} = V_{DD\_DIGITAL} = V_{DDO\_X} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{OD}$	Differential Output Voltage		200 (*target)	400 (*target)		mV
$\Delta V_{OD}$	$V_{OD}$ Magnitude Change			30 (*target)		mV
$V_{OS}$	Offset Voltage			1.6 (*target)		V
$\Delta V_{OS}$	$V_{OS}$ Magnitude Change			50 (*target)		mV
$I_{SC}$	Output Short Circuit Current					mA

NOTE:  $V_{DDO\_X}$  denotes  $V_{DDO\_X[0:15]}$ .

\*NOTE: Design Target specs.

## AC Electrical Characteristics

**Table 5A. AC Characteristics,  $V_{DD} = V_{DD\_DIGITAL} = V_{DDO\_X} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{IN}$	Input Frequency				650	MHz
$t_{sl(o)}$	Output Slew Rate	Measured at the Differential Waveform, $\pm 200\text{mV}$ from the Center				V/ns
$\Delta V_{AC}$	AC Swing					V
$t_{jit}(\emptyset)$	RMS Phase Jitter, (Random); NOTE 1	125MHz, Integration Range 12kHz – 20MHz				ps
$t_R / t_F$	Output Rise/Fall Time	20% to 80%				ps

NOTE:  $V_{DDO\_X}$  denotes  $V_{DDO\_X[0:15]}$ .

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 1: Refer to the phase noise plot.

**Table 5B. Serial Rapid IO Switch Jitter Specification,  $V_{DD} = V_{DD\_DIGITAL} = V_{DDO\_X} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	IDT sRIO Specification	Units
$J_{CLK\_REF}$	Total Phase Jitter, RMS; NOTE 1, 2, 3, 4			0.64	1.55	3	ps

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions. For additional information, refer to the *Serial Rapid IO Application Note* section in the datasheet.NOTE 1: Total phase jitter after applying the evaluation bands to the system transfer function for the IDT sRIO Tsi57x and Tsi620 Product Families. The transfer function is defined and illustrated in the *Serial Rapid IO Application Note* section in the datasheet and the IDT hardware manual of the Tsi57x and Tsi620. Total RMS phase jitter allowed on the reference clock of the Tsi57x and Tsi620 is specified at 3ps (max).

NOTE 2: Evaluation band with sRIO mask applied: 10Hz - 40MHz.

NOTE 3: Total phase jitter includes random and deterministic jitter.

NOTE 4: Jitter data is measured with Agilent E5052A Signal Source Analyzer.



**Table 5C. PCI Express Jitter Specifications,  $V_{DD} = V_{DD\_DIGITAL} = V_{DDO\_X} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$** 

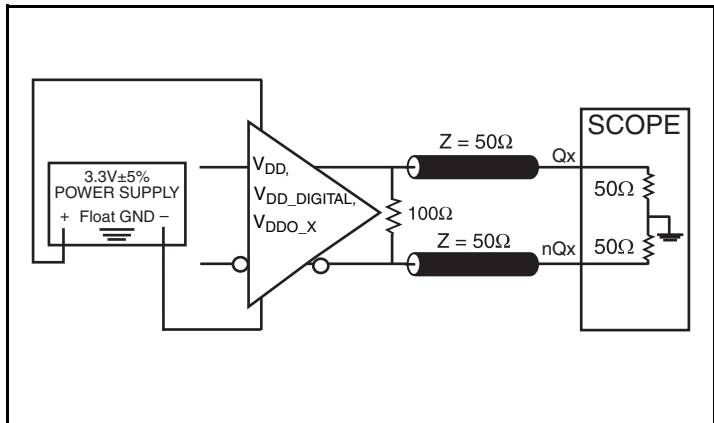
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	PCIe Industry Specification	Units
$t_{REFCLK\_HF\_RMS}$ (PCIe Gen 2)	Phase Jitter RMS; NOTE 1, 2	$f = 100\text{MHz}$ , High Band: 1.5MHz - Nyquist (clock frequency/2)				3.10	ps
$t_{REFCLK\_LF\_RMS}$ (PCIe Gen 2)	Phase Jitter RMS; NOTE1, 2	$f = 100\text{MHz}$ , Low Band: 10kHz - 1.5MHz				3.0	ps

**NOTE:** Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions. For additional information, refer to the *PCI Express Application Note section* in the datasheet.

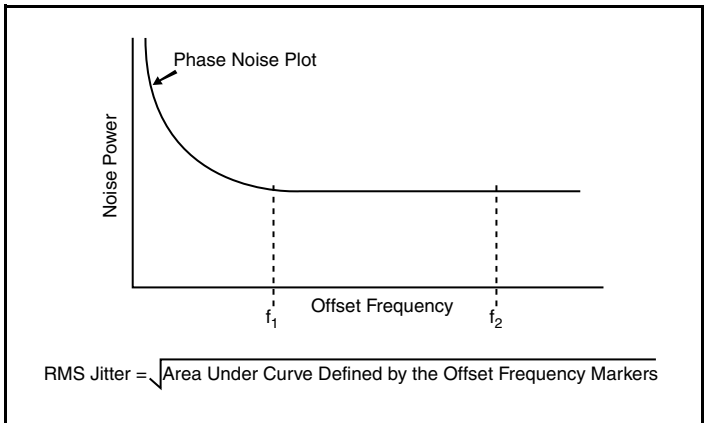
**NOTE 1:** RMS jitter after applying the two evaluation bands to the two transfer functions defined in the Common Clock Architecture and reporting the worst case results for each evaluation band. Maximum limit for PCI Express Generation 2 is 3.1ps RMS for  $t_{REFCLK\_HF\_RMS}$  (High Band) and 3.0ps RMS for  $t_{REFCLK\_LF\_RMS}$  (Low Band).

**NOTE 2:** This parameter is guaranteed by characterization. Not tested in production.

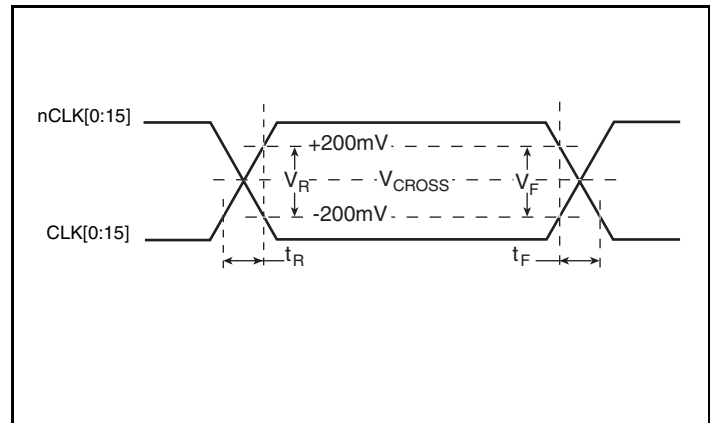
Parameter Measurement Information



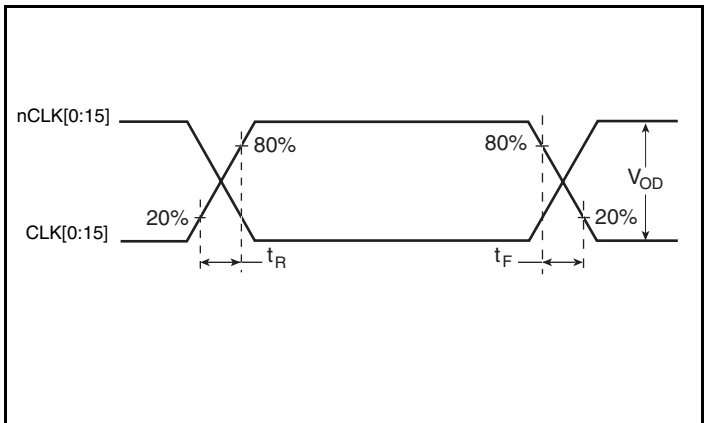
3.3V M-LVDS Output Load AC Test Circuit



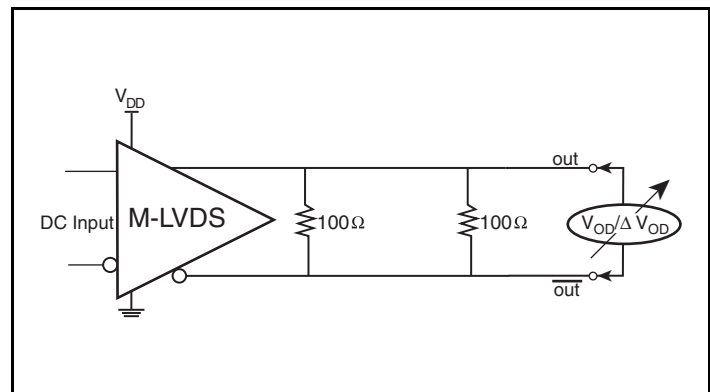
RMS Phase Jitter



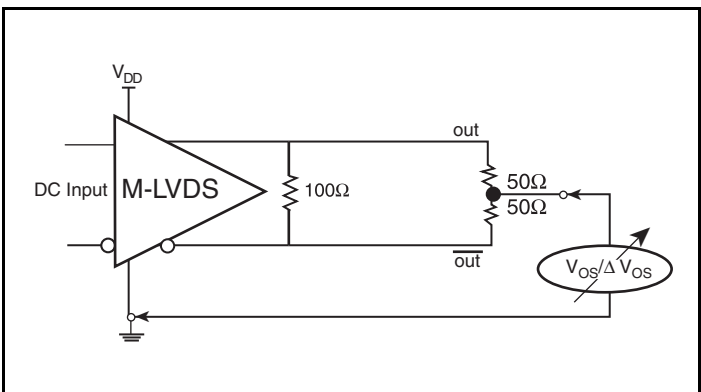
Output Slew Rate



Output Rise/Fall Time



M-LVDS Differential Output Voltage Setup



M-LVDS Offset Voltage Setup

## Applications Information

The IDT8V54816 is a clock crosspoint switch designed to distribute clocks in  $\mu$ TCA.4 systems. The 8V54816 distributes clock coming from an AMC Timing card to other AMC cards.

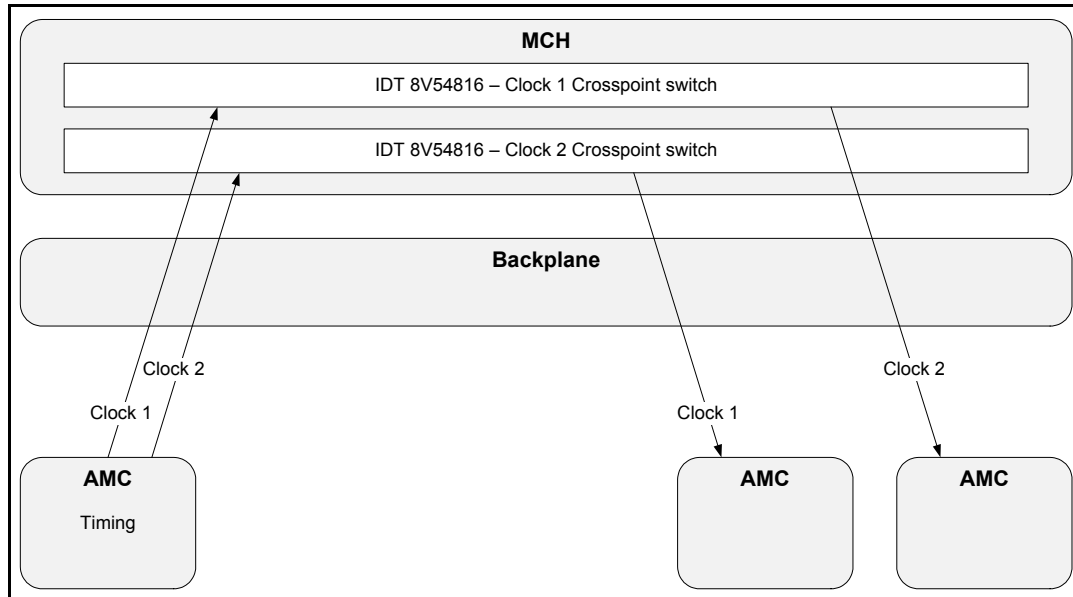


Figure 1. 8V54816 Application Drawing.

### Port Termination

All 16 bi-directional clock ports (CLKx, nCLKx) feature a switchable,  $100\Omega$  termination. External  $100\Omega$  termination may be used. In that case the internal termination shall be disabled.

Internal termination is enabled by setting Bit 6 of the configuration register corresponding to the considered I/O port to 1.

#### Case 1: Terminations present on the backplane

In case  $100\Omega$  terminations are present on the backplane, terminations of the corresponding ports of the 8V54816 shall be disabled. No termination shall be present on AMC cards. See Figure 2.

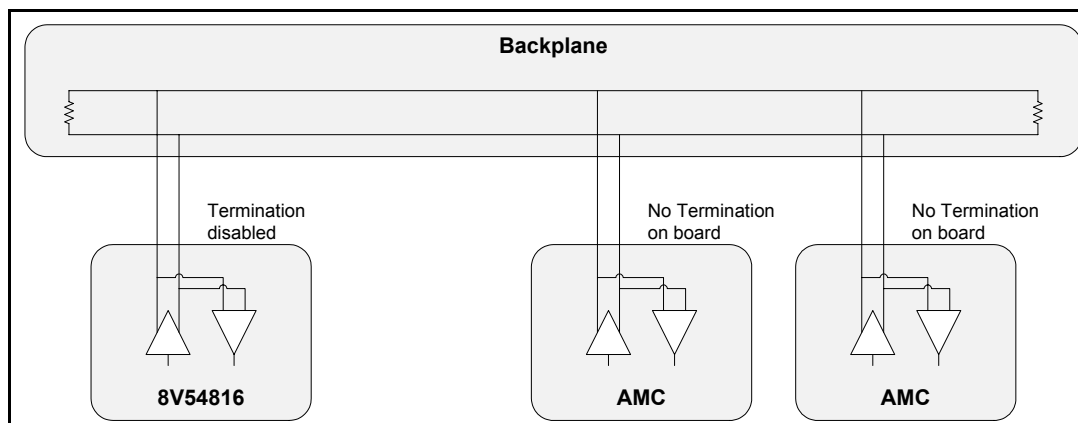
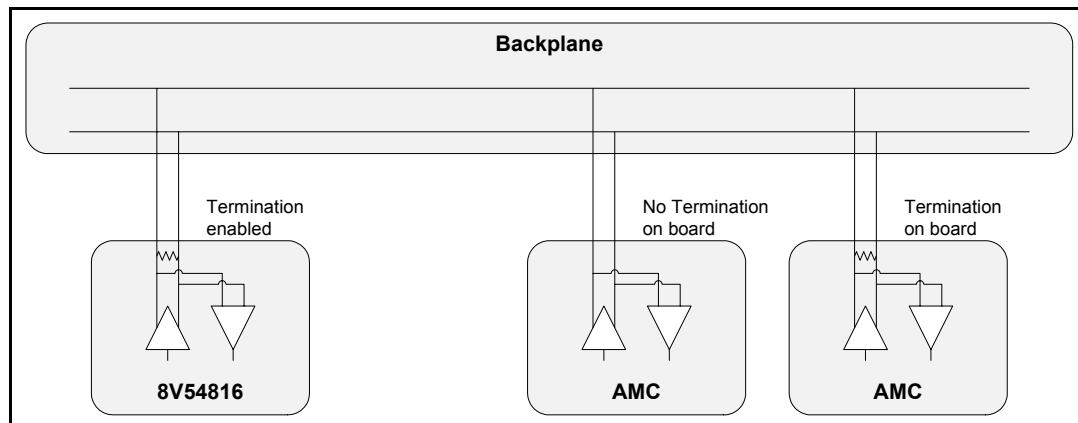


Figure 2. Termination on Backplane

**Case 2: No terminations present on the backplane**

When no terminations are present on the backplane, two terminations shall be activated in order to realize a multipoint M-LVDS configuration. See Figure 3.



**Figure 3. No Termination on Backplane**

**Polarity Inversion**

Polarity inversion of each port can be used in order to facilitate board layout. Polarity inversion is enabled by setting Bit 5 of the register corresponding to the considered port to 1. If polarity inversion is enabled,

- CLKx becomes the negative input or output of port x
- nCLKx becomes the positive input or output of port x

## Port Configuration Example

Any CLKx, nCLKx port of the IDT8V54816 can be configured as either input or output. Let's consider the following examples:

- 100MHz clock source routed to port 2
- 100MHz clock to be distributed to ports 3, 5, 8 and 9
- 25MHz clock source routed to port 6
- 25MHz clock to be distributed to ports 1, 11 and 12
- Ports 13, 14 and 15 are not used

**Table 6. Port Configuration Table**

I <sup>2</sup> C Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit Description	Port I/O Configuration	Termination Enable	Polarity of Differential Interface	Reserved	Output Port Select [3]	Output Port Select[2]	Output Port Select [1]	Output Port Select [0]
0	n/a	Depend on Hardware Configuration		Reserved	n/a			
1	1				0	1	1	0
2	0				X	X	X	X
3	1				0	0	1	0
4	n/a				n/a			
5	1				0	0	1	0
6	0				X	X	X	X
7	n/a				n/a			
8	1				0	0	1	0
9	1				0	0	1	0
10	n/a				n/a			
11	1				0	1	1	0
12	1				0	1	1	0
13	0	0	X		X	X	X	X
14	0	0	X		X	X	X	X
15	0	0	X		X	X	X	X

## Recommendations for Unused Input Pins

### Inputs:

#### LVCMOS Control Pins

All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A 1k $\Omega$  resistor can be used.

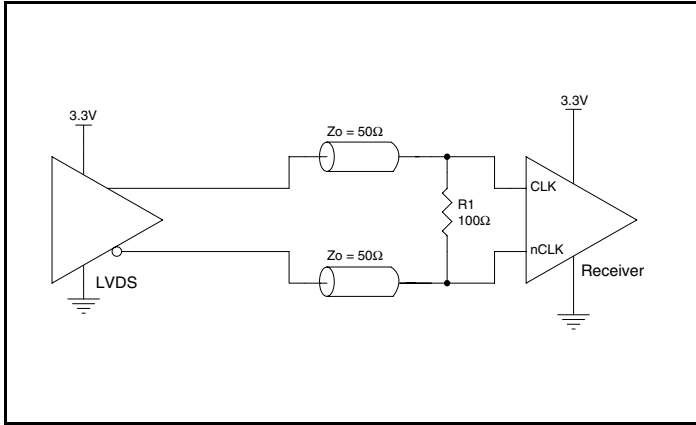
#### Bi-directional CLK/nCLK Ports

It is recommended to configure unused CLKx and nCLKx ports as input, and disable the internal 100 $\Omega$  termination. Pins can be left unconnected.

## Differential Clock Input Interface

The CLKx /nCLKx accepts LVDS and other differential signals. Both differential signals must meet the  $V_{PP}$  and  $V_{CMR}$  input requirements. *Figure 4* shows an interface example for the CLKx/nCLKx input driven by the most common driver types. The input interfaces

suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. If the driver is from another vendor, use their termination recommendation.

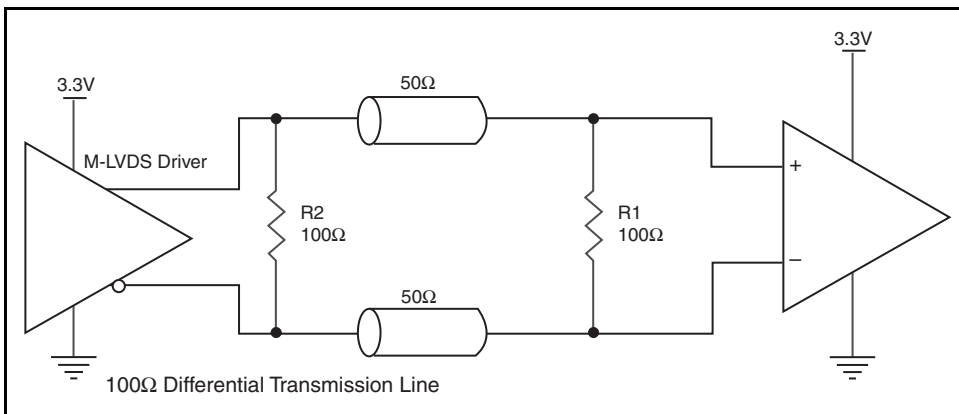


**Figure 4. CLK/nCLK Input Driven by a 3.3V LVDS Driver**

## 3.3V M-LVDS Driver Termination

A general M-LVDS interface is shown in *Figure 5* In a 100Ω differential transmission line environment, M-LVDS drivers require a matched load termination of 100Ω across near the receiver input. For

a multiple M-LVDS outputs buffer, if only partial outputs are used, it is recommended to terminate the unused outputs.



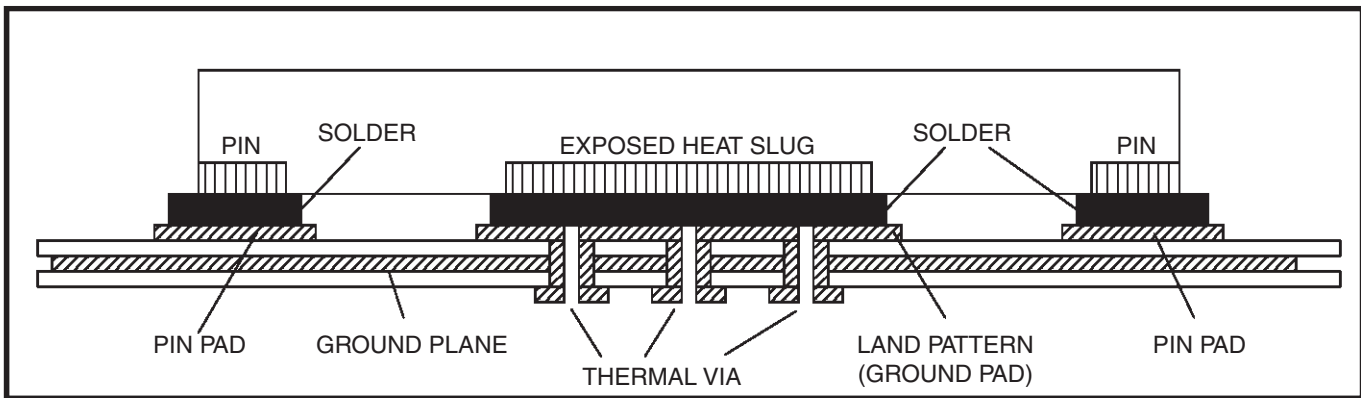
**Figure 5. Typical M-LVDS Driver Termination**

## VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 6*. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific

and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor's Thermally/Electrically Enhance Leadframe Base Package, Amkor Technology.



**Figure 6. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)**

## PCI Express Application Note

PCI Express jitter analysis methodology models the system response to reference clock jitter. The block diagram below shows the most frequently used *Common Clock Architecture* in which a copy of the reference clock is provided to both ends of the PCI Express Link.

In the jitter analysis, the transmit (Tx) and receive (Rx) serdes PLLs are modeled as well as the phase interpolator in the receiver. These transfer functions are called H1, H2, and H3 respectively. The overall system transfer function at the receiver is:

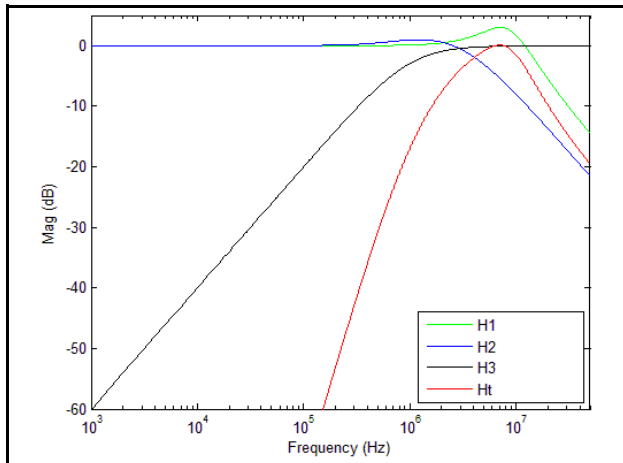
$$Ht(s) = H3(s) \times [H1(s) - H2(s)]$$

The jitter spectrum seen by the receiver is the result of applying this system transfer function to the clock spectrum X(s) and is:

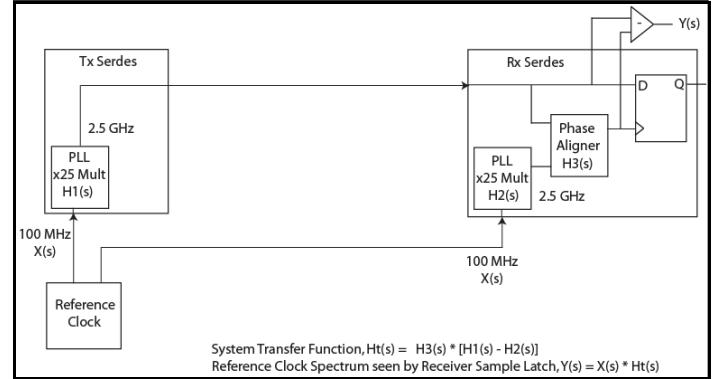
$$Y(s) = X(s) \times H3(s) \times [H1(s) - H2(s)]$$

In order to generate time domain jitter numbers, an inverse Fourier Transform is performed on  $X(s) \times H3(s) \times [H1(s) - H2(s)]$ .

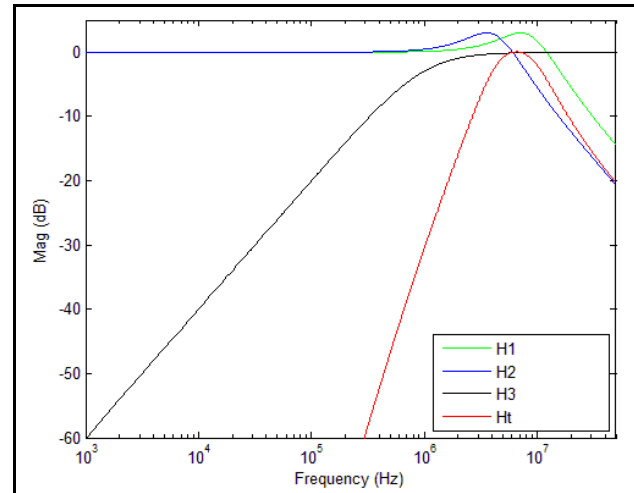
For **PCI Express Gen 2**, two transfer functions are defined with 2 evaluation ranges and the final jitter number is reported in rms. The two evaluation ranges for PCI Express Gen 2 are 10kHz – 1.5MHz (Low Band) and 1.5MHz – Nyquist (High Band). The plots show the individual transfer functions as well as the overall transfer function Ht.



PCIe Gen 2A Magnitude of Transfer Function



PCI Express Common Clock Architecture



PCIe Gen 2B Magnitude of Transfer Function

For a more thorough overview of PCI Express jitter analysis methodology, please refer to IDT Application Note *PCI Express Reference Clock Requirements*.



## Reliability Information

Table 7.  $\theta_{JA}$  vs. Air Flow Table for a 100-lead VFQFN Package

$\theta_{JA}$ vs. Air Flow			
Meters per Second	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	22.9°C/W	18.0°C/W	16.0°C/W

## Transistor Count


The transistor count for IDT8V54816I is: 174,219

Technical drawing of a 12.0 x 12.0 mm body package outline. The drawing includes a TOP VIEW, SIDE VIEW, and BOTTOM VIEW. The TOP VIEW shows a square package with dimensions 12.0 x 12.0 mm. The SIDE VIEW shows the package height and lead dimensions. The BOTTOM VIEW shows the lead pitch and dimensions. The drawing includes a detail 'A' showing the lead cross-section and a tie bar mark option. The drawing is titled '12.0 x 12.0 mm BODY' and is a standard package outline.

DCN	REV	DESCRIPTION	DATE	APPROVED
00	00	INITIAL RELEASE	09/10/09	PKP
01	01	REMOVE EPAO VARIATION & OTHER LEADCOUNT	09/23/11	RT

REVISIONS	
DCN	REV
00	00
01	01

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TOLERANCES UNLESS SPECIFIED	 <b>IDT™</b> 6024 Silver Creek Valley Road San Jose, CA 95138 PHONE: (408) 284-8200 FAX: (408) 284-8591 <a href="http://www.IDT.com">www.IDT.com</a>		
DECIMAL ANGULAR			
X1			
XX4			
XXX4			
APPROVALS	DATE	TITLE <b>N/INLG PACKAGE OUTLINE</b> 12.0 x 12.0 mm BODY PUNCH Type SIZE DRAWING No. <b>PSC-4286</b> DO NOT SCALE DRAWING	
DRAWN 09/30/09	09/10/09		
CHECKED			
		REV 01	SHEET 2 OF 3

Package Outline and Package Dimensions, continued

NOTES:

1. DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM(.012 INCHES MAXIMUM)

2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. – 1994.

3. N IS THE NUMBER OF TERMINALS.

ND IS THE NUMBER OF TERMINALS IN X-DIRECTION & Ne IS THE NUMBER OF TERMINALS IN Y-DIRECTION.

4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP.

5. THE PIN #1 IDENTIFIER MUST BE EXISTED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.

6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.

7. ALL DIMENSIONS ARE IN MILLIMETERS.

8. THE SHAPE SHOWN ON FOUR CORNERS ARE NOT ACTUAL I/O.

9. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

10. APPLIED ONLY FOR TERMINALS.

11. Q AND R APPLIES ONLY FOR STRAGHT TIEBAR SHAPES.

12. FOR 0.40mm LEAD PITCH, THE LEAD POSITION TOLERANCE MUST BE 0.07mm AT THE ACTUAL MEAN VALUE OF BODY SIZE.

13. MOLD FLASH OR PLATING COVERAGE ON THE RING PAD AREA SHALL BE ALLOWABLE

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
	00	INITIAL RELEASE	09/10/09	PKP
	01	REMOVE EPAD VARIATION & OTHER LEADOUT	09/23/11	RT

TOLERANCES  
UNLESS SPECIFIED

DECIMAL ANGULAR

XX±

XXX±


APPROVALS

DRAWN *pkp*

CHECKED

DATE

09/10/09

 IDT

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San Jose, CA 95138  
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TITLE NL/NLG PACKAGE OUTLINE  
12.0 x 12.0 mm BODY  
PUNCH Type

SIZE C

DRAWING No. PSC-4286

DO NOT SCALE DRAWING

REV 01

SHEET 3 OF 3

## Ordering Information

Table 8. Ordering Information Table.

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8V54816NLGI	IDT8V54816NLGI	Lead-Free, 100-lead VFQFN	Tray	-40°C to 85°C
8V54816NLGI8	IDT8V54816NLGI	Lead-Free, 100-lead VFQFN	500 Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an “G” suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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