Clock & control video conference (19.11.2009)

C.Youngman 20.11.2009 (last revised 20.11.2009)

1 Introduction

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The C&C signal line definitions were discussed; see decisions, questions and comments interleaved in Martin's spec. email (9.11.2009). The aim is to work towards a final C&C specification. The status of the contract was also discussed.

2 Discussion of Martin's email signal spec

C&C signal definitions

>> 1) C&C PCB - hardware - inputs from T.R. :
>> ---
>>
>> Clock Inputs : a) Bunch Clock from T.R. board in crate :
>> 5 MHz or 4.5 MHz, Differential LVDS
>> on RJ45 input socket A pins 1+ and 2-
>>

The decision on the XFEL bunch frequency will be made at the mid January meeting of XFEL-MAC (Machine Advisory Committee). The email from K.Rehlich suggest that 4.5MHz will be chosen.

>> b) External clock inputs :
>> i) Differential LVDS,
>> on RJ45 input socket B pins 7+ and 8-
>> ii)LVTTL or NIM, single ended, LEMO 00
>> permissible range 750 kHz - 6 MHz
>> (slower clocks below 750 kHz acceptable
>> but will not meet jitter etc. specs)
>> (faster clocks above 6 MHz acceptable
>> but will not permit synchronous veto)
>>

An internally generated clock (4.5 or 5MHz) is provided for standalone running. The external clock input discussed here is provided by the light source timing system XFEL, LCLS, Spring8 where the C&C system operating.
What is available at LCLS, Spring8, etc. has to be determined.

>> TRAIN-START (Trigger) Inputs :
>>
>> a) TRAIN-START pulse from T.R. board in crate
>> Single pulse, ~15msec before the first bunch
>> on RJ45 input socket A pins 4+ and 5-
>>
>> b) External Trigger input
>> i) Differential LVDS,
>> on RJ45 input socket B pins 3+ and 6-
>> ii)LVTTL or NIM, single ended, LEMO 00
>>
>> Inputs a) for run-mode with XFEL detectors and T.R. installed
>> Inputs b) for stand-alone/test mode or other unknown detectors
>>

Cable lengths between the C&C and FEE modules are ≤5m. TR and C&C are in the same crate and cable lengths are short.

>> 2) C&C PCB - hardware - outputs :
>> ---
>>
>> Fast Commands Lines : Line 1: CLOCK
>> On RJ45 socket C pins 1+ and 2-
>> Line 2: START and RESET Commands
>> On RJ45 socket C pins 4+ and 5-
>> Line 3: VETO / NO-VETO Commands
>> On RJ45 socket C pins 7+ and 8-
>>
>>
>> Proposed Details : Line 1: CLOCK is an integer multiple of the input
>> ---------- Bunch Clock.
>> - If input Bunch Clock is 5.0 MHz,
>> this output clock will be 100.00 MHz
>> - If input Bunch Clock is 4.5 MHz,
>> this output clock will be 99.00 MHz
>> It is PLL-ed to the Bunch Clock
>> It is un-interrupted during a run
>> It is in fixed phase relationship to the
>> Bunch Clock
>>
>> Line 2: A) START Command consists of the following data

>>
>> a)Start = 1100 (4 bits)
>> b)Train-ID = 32 bits, counts-up by '1' for
>> each train
>> (ie. no GPS-derived
>> timing info)
>> c)Bunch-Pattern-ID = 8 bits
>> d)CheckSum of b) and c) = 8 bits
>> ----------
>> Total = 52 bits of data
>>
>> NOTE : simple CheckSum = ex-OR of five
>> ------ 8-bit words of b) and c)
>>
>>
>> after all ~3000 bunches have been sent :
>>
>> e)Stop = 1010 (4 bits)
>>
>> B) RESET Command (to reset the FE
>> micro-controller
>> via the FE FPGA)
>> Reset = 1001 (4 bits)
>>
>> C) -Reserved-
>> Reserved = 1111 (4 bits)
>>
>> NOTE : using four bit 1100/1010/1001/1111
>> ------ commands prevents single-wrong-bit error
>>
>>

More that 4 opcodes can be defined later by increasing the number of bits.

The bit error rate (BER) should ideally be none and certainly not more than a few/day. If high BER rates are seen during running this means that there is a fault, which must be repaired, or the timing is wrong and must be corrected.

The magnetic couplers targeted have (specs) large slew times: ~2ns between channels and ~10ns between devices. Individual programmable timing delays will be used to equalize the slews. The delay value used is determined by measuring a delay curve (how often?) – should be an automated procedure using either external or internal clock trigger.

What happens when an error occurs during running, i.e. the system is already timed in? A possible scenario for START events is:

- the error is identified at the FEE using the checksum and an error counter incremented. Counting errors is a must.
- the counter has to be readable by the monitoring system (e.g. PC in the C&C crate) using the snapshot messages over the network connection.

How are the event driven FEE, TB and PCL data flows affected by an error?

- the FEE modules have a three deep data processing pipeline (digitize, format and link – true for LPD and DSSC?) which means that data received in train i is sent to the TB during the gap following train i+2.
- if an error occurs the corresponding clock of the FEE data processing chain is missed and the data flows between FEE modules are no longer train-id synchronized (unless all FEEs saw an error, in which case a train-id is missing)
- the TB is effected because data from the affected module will not be sent. The TB will wait for the data. The PCL level is not affected.
- If all FEE modules see an error data from that train-id would be missed, but the data flows remain synchronized. The TB is not affected.

To prevent unsynchronized data propagating through the TB and backend, the C&C has to stop issuing STARTs. Two possibilities exist to do this:

- The monitoring software must see the error increment and stop the C&C issuing STARTs. This has to be done before the START of the next train-id is generated by the TR: between 0 – 85ms for 10Hz and 0 – 15ms for 30Hz operation.
- The Line 4 signal is used to feedback the error state from FEE modules to the C&C master via a fan-in. This error state is cleared by the control software.

What happens once the C&C is inhibiting STARTs?

- stop the run and throw away all data in the FEEs and TB.
- insert a clock in the effected FEE modules to unblock the TB, clear data flows associated with the last START (or all) data in all FEE data flows, and continue by enabling STARTs. Bookkeeping of the cleared train-ids is required. Note that the cleared data flow steps propagate so they need to be identifiable to the backend.
- continue by enabling STARTs if all FEE modules saw an error.
- Bookkeeping of the missed and cleared train-id is required.
- **The FEE and TB groups need to be involved in this discussion – what is possible and sensible.**

>> Line 3: A) VETO Command consists of following data
>>
>> a) Veto = 110 (3 bits)
>> b) Bunch-ID = 12 bits
>> c) Reserved = 4 bits
>>
>> B) NO-VETO Command consists of following data
>>
>> a) No-Veto = 101 (3 bits)
>> b) Bunch-ID = 12 bits ????
>> c) reserved = 4 bits
>>

>> NOTE : using three bit 110 / 101 commands
>> ------ prevents single-wrong-bit error
>>
>>

The proposition for Line 3 was agreed to. The bunch-id should be set to a defined value for no-veto decisions.

>> 3) C&C PCB - hardware - input from FEEs :
>> ----------
>>
>> FE Status Line: Line 4: STATUS Feedback from all FEEs
>> On RJ45 socket C pins 3+ and 6-
>>
>>
>> Proposed Details : Line 4: Feedback to indicate that each FEE is
>> ---------- powered-up and cable plugged in correctly
>>
>> OK : Continuous clock (derived from the
>> ~100 MHz clock received from C&C
>> on socket C pins 1 and 2)
>>
>> ERROR : no clock
>> (high / low / floating)
>>

There was a discussion of whether Line 4, on/off status, could be used to disable data taking. **It was agreed to keep open the option of encoding information onto Line 4.** Line 4 is the only place where information from all FEE modules is available – some of us think that encoding information onto line 4 will be required!