Notes from the 26.7.2010 telephone conference.

26.7.2010 v1 CY

1   Attendance

FEA: M.Zimmer
UCL: E.Motuk, M.Wing, M.Postranecky and M.Warren
WP28: K.Rehlich
WP76: D.Wilson and C.Youngman

2   Discussion

The first six bullets, the DAMC2 requirements Section 9, see draft XFEL_CC_DRAFT-2-2_Implementation_ALL_09-07-2010 document, were discussed:

- All requirements are supported by the DAMC2 baseline design.

The second group of three bullets, the wish list, were discussed:

- Taking the design lock-stock-and-barrel and modifying it at RAL was accepted as difficult.
- The question is when can modifications be put in and what is the likelihood that the wished for modifications will be made.
- Always having a TR in the crate acting as the interface to EuXFEL and any other timing system discussion:
    - TCLKA/B (nominal 4.5MHz/99MHz) could be driven by the TR. The data sheet of the Nat. Semiconductor LMK01000 chip on TCLKB (driven by SFP or external CML input), see block diagram in P.8 of timing note. TCLKA is proceeded by a 9515 chip and a divider (LMK chip) – <u>Kay will check his statement.</u>
    - Would any DAMC2 modifications then be required?
    - Should it be assumed that the TR is always in the crate?
    - **Always having the TR in the crate is a possibility – does UCL want it?**
- Modifying the DAMC2
    - Discussion of the 3 bullets with P.Vetrov: PLL on FMC is possible, DAMC2 layout changes are needed to allow the DAMC2 to drive TCLKA/B (rather than just receiving them). Not certain what is meant by flexibility improvement (bullet 3).
    - Bi-direction clock driving using Attila's template would increase the cost of the boards. This requires a layout change to the DAMC2 (output drivers must be added).
    - Remember that the accuracy of the clock (jitter…) is currently 100-200ps, which is driven by the current MCH implementation.
    - The original requirement of the DAMC2 driving the 99MHz line originated form the from the requirement of driving more slave (DAMC2) boards, so if this feature can be provided in a reasonable time scale on a planned upgrade of the DAMC2 then its non availability in the initial DAMC2 would be acceptable. **Kay and Manfred have no problem with this approach.**

TR related issues raised during the DAMC2 discussion:

- If the 99 MHz clock can be driven by the TR, can 99 MHz be used for the Telegram encoded line?
  - Kay agreed that a strobe clock and a data line would make life easier for telegram handling (Manchester coding is FPGA expensive) this should be done:
    - costs 1 line more,
    - the protocol to be defined (start, stop bits…)
  - Kay suggests having TCLKA or B on the bussed lines.
  - There was no statement that 99 MHz could be configured for use with the telegram.
- Note that the current version of the TR (this is the double height (VME naming convention) version?) has only 4 bussed lines implemented (the DAMC2 implements all 8).
  - CC needs reset, trigger and telegram strobe/data pair = OK not a problem..

Summary of discussion so far w.r.t. DAMC2:
- **Manfred – planned upgrades (the UCL wish list) can be implemented into the next DAMC2 version.**
- **Kay – TR 99 MHz can be distributed and strobe/data pair telegram handling are possible and favoured.**
- **UCL – single board phase 1 prototype based on the DAMC2 does not need the wish list features, these would have to be implemented in the next planned update.**

It was agreed that the UCL wish list items can be incorporated into the next DAMC2 version – Petr Vetrov should check for show stoppers when he returns (+4 weeks).

The TR related items in section 8 of the draft were discussed:
- 1, The 99 MHz can be driven
- 2, Strobe/data pair is sensible (but no willingness to distribute at the 99 MHz clock)
- 3, Kay will check with other customers if the strobe/data pair is a problem
- 4, signal definition
- 5, external inputs: 4 are required (bunch clock, bunch trigger, laser clock, and one spare) – Kay counted: there are 3 – the spare might not exist – OK can live with, but Kay asked to give a definite statement of what is there.
- 6, Required telegrams – all were accepted including a DAQ ready (maybe synchronous with START in 30 Hz mode)
- 7, bunch pattern content – if sent might be used, expecting to use the bunch index and have the pattern provided at configuration
- 8, interrupts will be generated as expected.
- 9, bunch clock is contiguous with no phase changes (Kay – yes)
- 10, standalone options – not discussed.
- 11, the current TR has no RTM (again is this the double height (VME) version?). Additional SFP connections for daisy chaining are likely to appear on the next version which will fit into the xTCA crate and plug standard being used and purchased now.

Summary of hardware availability of DAMC2 and TR boards:
- **Kay – STRUCK FADC and TR firmware are two different items – expect STRUCK to be ready before or at the same time as the TR.**
- **Kay – TR with basic firmware (not full functionality) expect to get hardware in Sept 2010.**
- **Manfred – DAMC2 (with similar caveats as for TR) expect to see a first hardware board ~1st Oct 2010.**

Above assumes no show stoppers – so UCL must plan a work schedule that allows for these dates (e.g. generating and handling telegram on a strobe/data pair – a suggestion for a protocol with an IP core would be appreciated by Kay – could this be done?)

3 Actions

UCL were asked to discuss and define what they want to do and make this known.

Kay was asked to update the RTM specification and distribute this to UCL.

Kay was asked to give confirm that the TR could distribute the 99 MHz (99.305558 MHz = nominal bunch clock * 22)