

Electronics for the European XFEL: AGIPD a high frame rate camera

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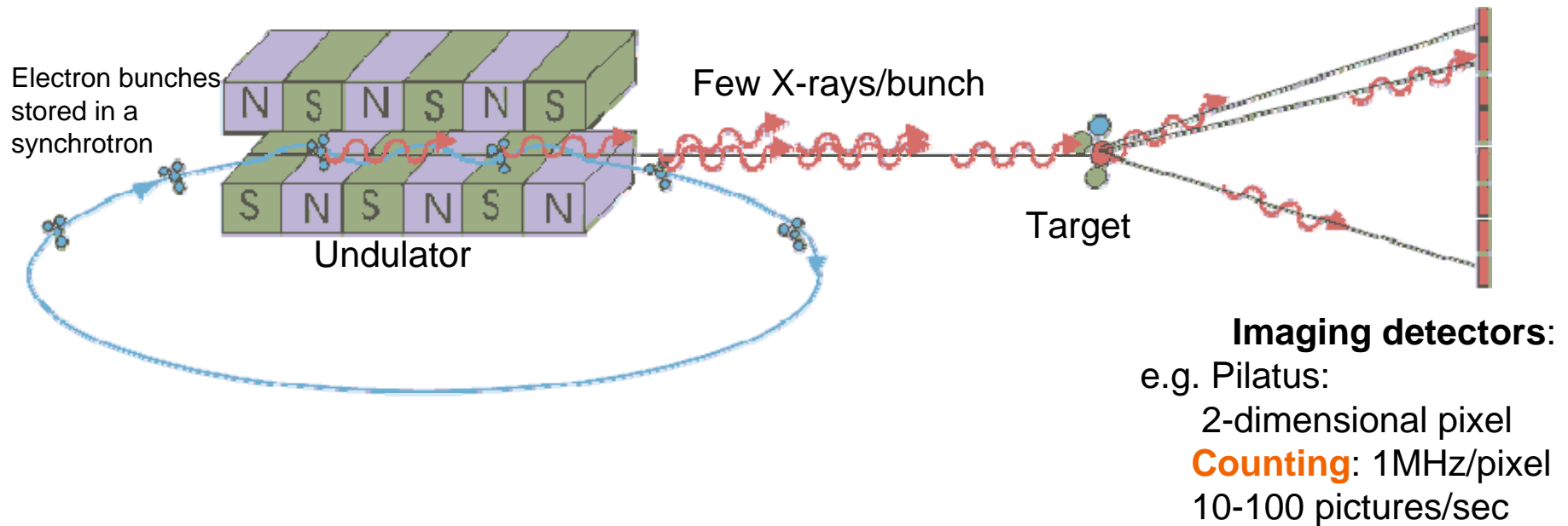
Electronics for the European XFEL: AGIPD a high frame rate camera

- > Motivation for new X-ray sources and detectors
- > Free Electron Laser as 4th generation sources : European XFEL
 - I am involved in some control electronics
- > Detectors and data acquisition : 2 dimensional cameras
 - AGIPD (I am involved), DSSC and LPD
- > Status of the project
- > Outlook



Science with X-ray from nowadays synchrotrons

3rd Generation



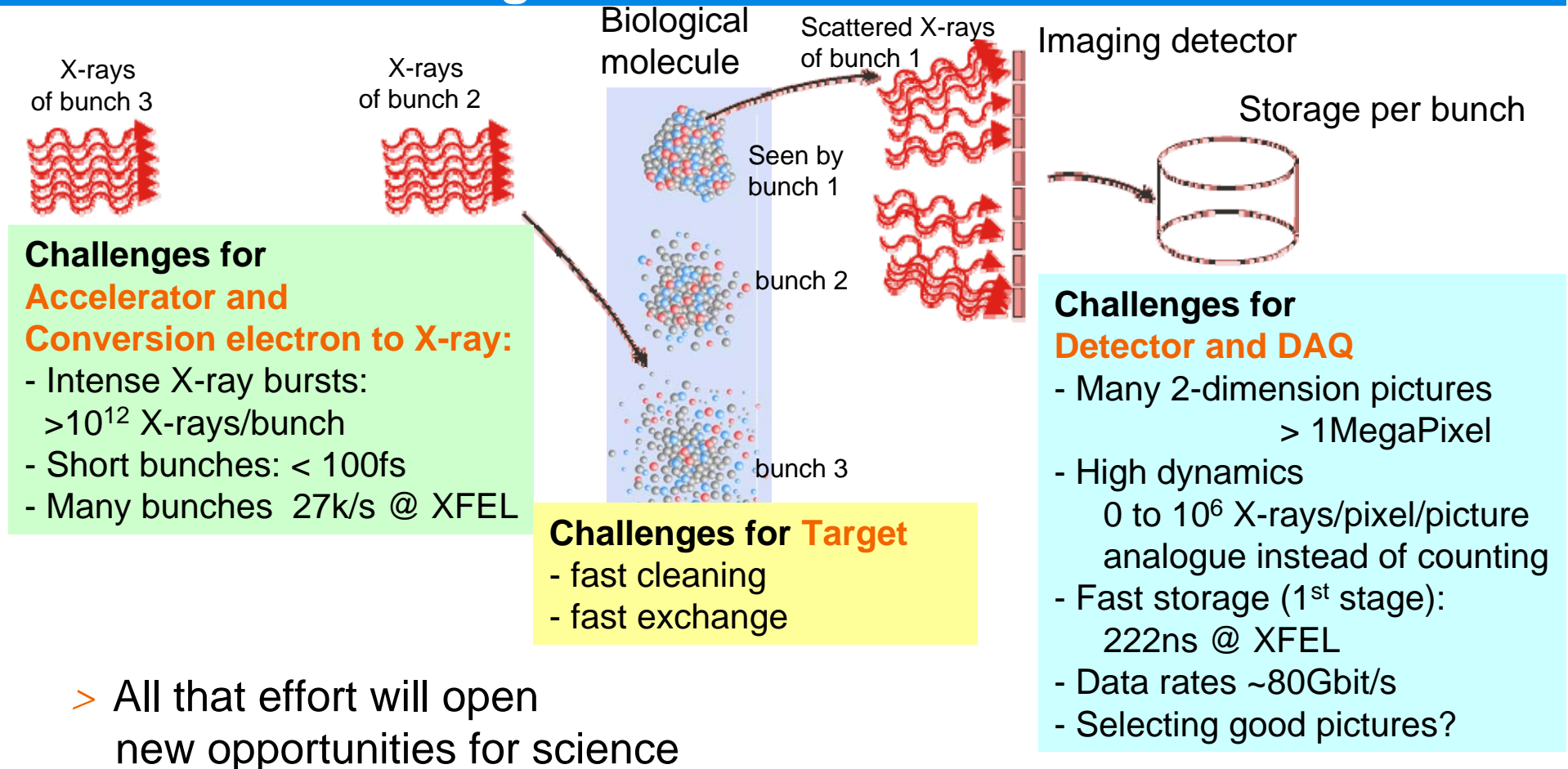
> Nice systems, but more wishes for the future

- Intensity,
- coherence for holography
- Overcome by many photons/bunch, the fact
First X-ray destroy the target, next sees already other structure
changed molecular structure or fragments



Dream of user's : Challenges for the designers

4th generation



- View to structure and dynamics in complex systems
molecules, clusters, biological objects, plasma
- Physics, chemistry, material science, biology, medicine



The technique to realize:

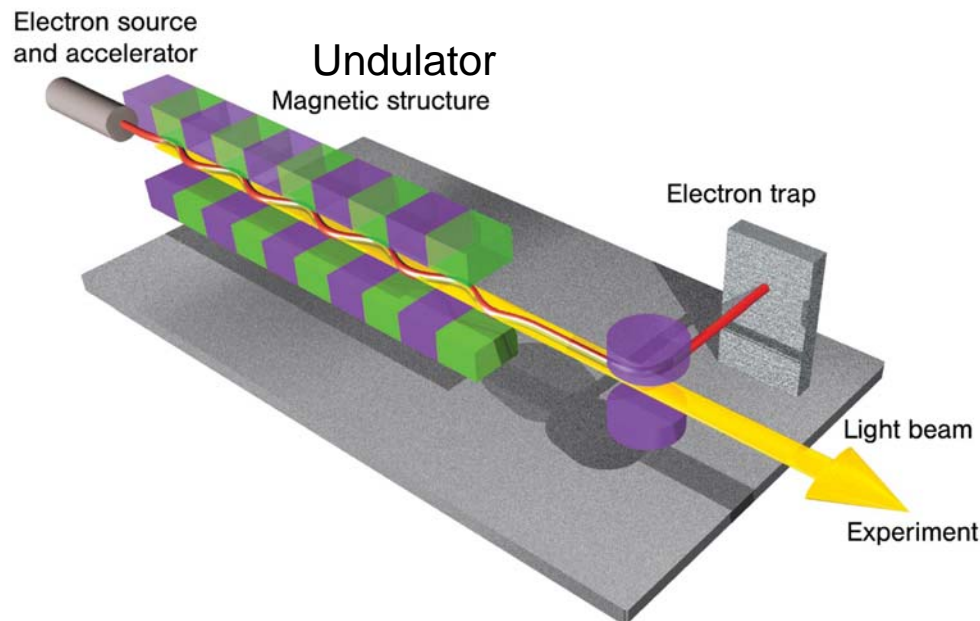
Free Electron Laser

Lasing depends strongly on density of excited states
Needs high density inside bunch of electrons

To provide high density bunches

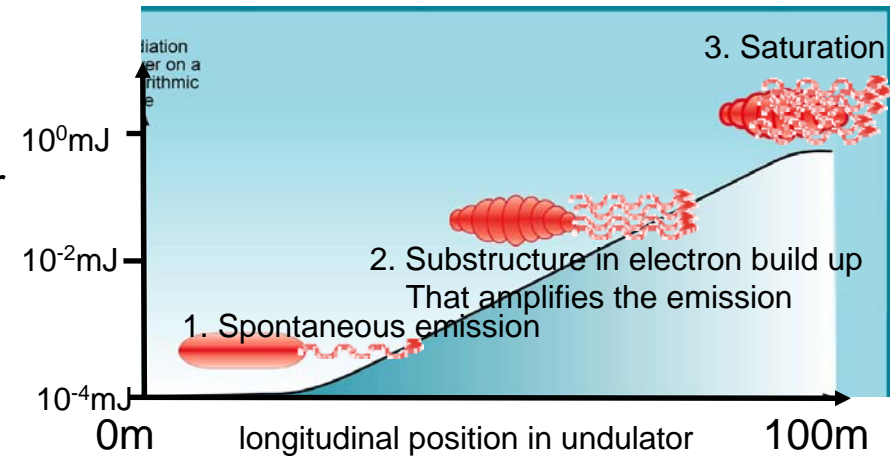
- a short pulse at **the source** is needed (50ps)
- optimization in the low energy part of accelerator
- maintaining the bunch quality while accelerating

Linear acceleration with very good RF-control
... complex electronics,
defining the standards for XFEL



The SASE principle

Self amplified spontaneous emission



Basic requirements, for
electron source and accelerator

$$\lambda_{X-ray} = \frac{\lambda_{undulator} (3.6cm)}{2(E/m)^2_{electron}} \left(1 + \frac{K^2}{2}\right) \quad \text{with} \quad K = \frac{eB_0 (\sim 1T) \lambda_{undulator}}{2\pi m_e c}$$

0.1nm requires 17.5GeV electrons

Power of X-ray growth with $e^{\sqrt{j} \dots}$

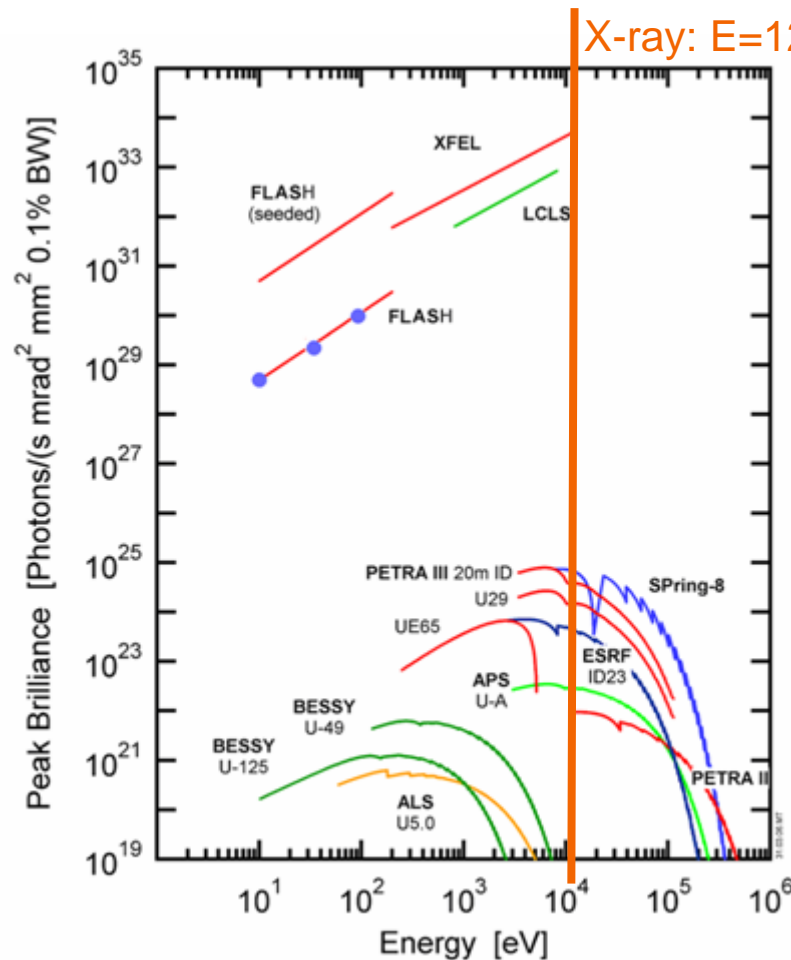
Need for short bunches $\sim 20\mu\text{m}$ with $Q=1\text{nC}$

$20\mu\text{m}$ convert to 70fsec



Comparison 3rd and 4th generation

Intense light gets delivered by lasers, now developing that for X-ray
Three sides have / are building light sources



Laser based sources

LCLS: Operation since 2009: X-ray

SCSS: Planned for 2010/11: X-ray ?????

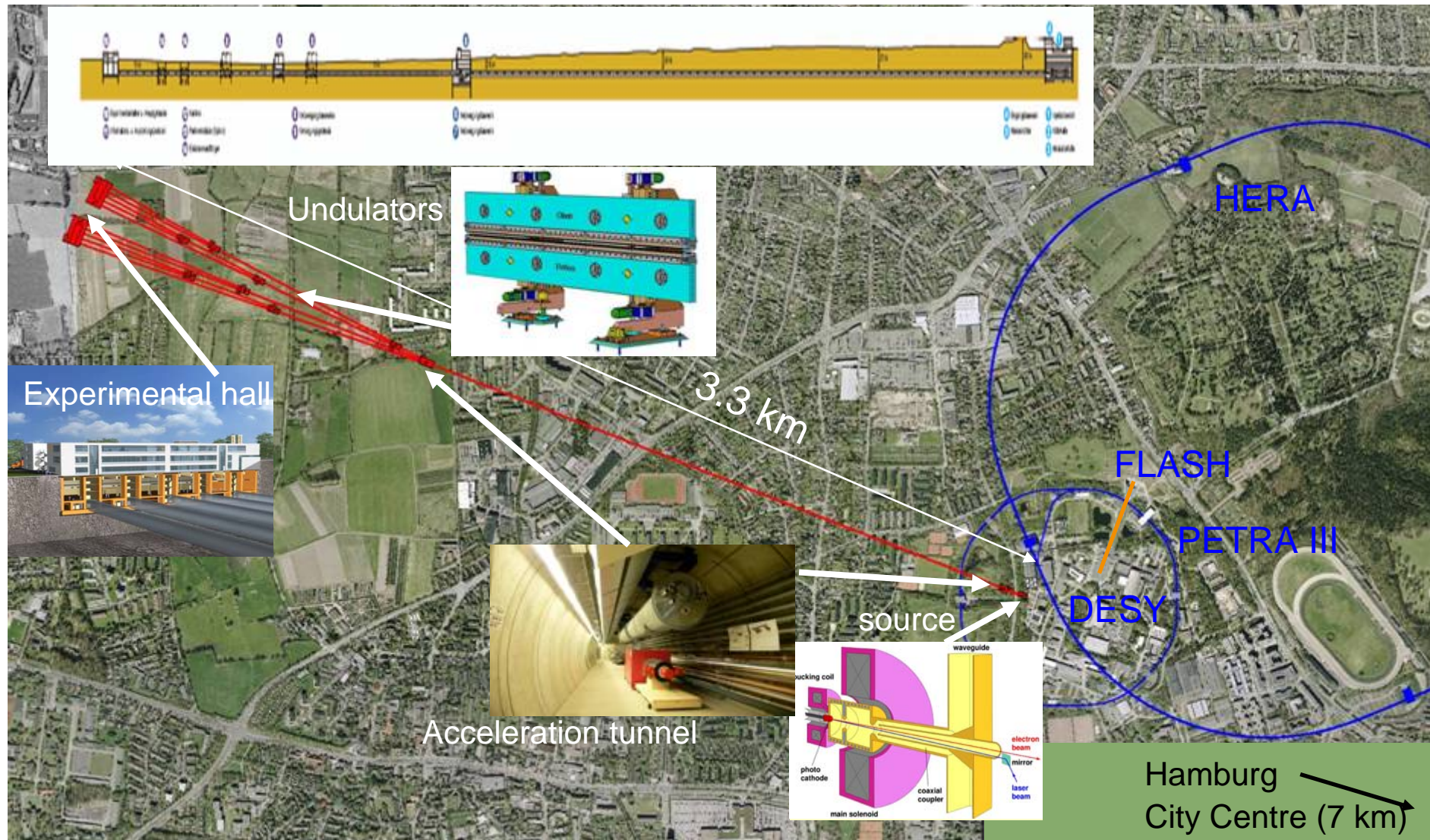
FLASH: Operation since 2005: VUV-light
User-operation and test facility for XFEL

XFEL: Construction until 2014: X-ray

Synchrotron based sources



The European XFEL:



The Cavity

- > Picture of cavity
niob, electropolishing
- > Quality picture
- > Superconductivity
- > Consequence: Heat development needs duty cycle of accelerator



Train structure

> Picture

> Advantage: still 27000 bunches/sec

> Consequence: All systems has to handle 222ns bunch to bunch

> 4.5MHz operation for 27k-bunches/sec.



LLRF

- > Pulse field of cavities
- > Pulse beam taken energy from field
- > Strong requirement of field flatness and phase
- > Feed forward networks: Train to train
- > begin of train to useful bunches: μs -response

To be contacted:
Schlarp, Ludwig

Requires complex electronics: Sets the standard for XFEL, “power user”



LLRF data handling

- > To be contacted:
- > Schlarp, Ludwig



xTCA as platform

- > Multi-gigabit serial via backplane
- > Configurable backplane: PXI, Ethernet, Aurora,

High availability:

- > Power management
 - redundant power supplies and fans
 - Module switch on only after verify: Less handling errors.
- > Dual star: redundant CPU's

Multi projects in one crate:

- > Hot swap
- > bei Rehlich nachsehen



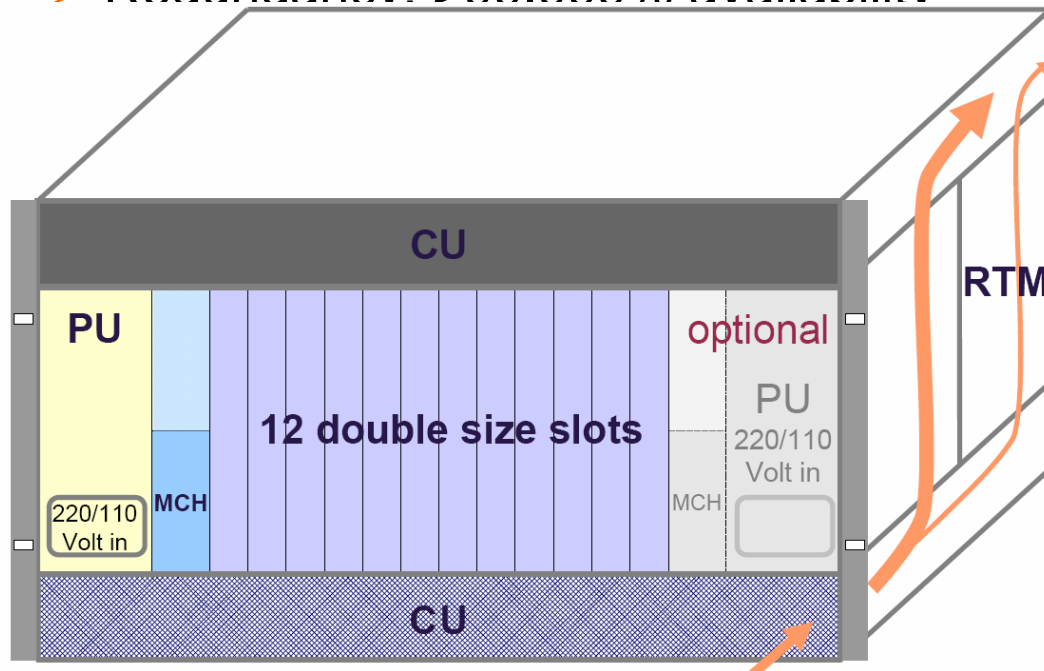
XTCA as physics standard for μ TCA: PICMG®



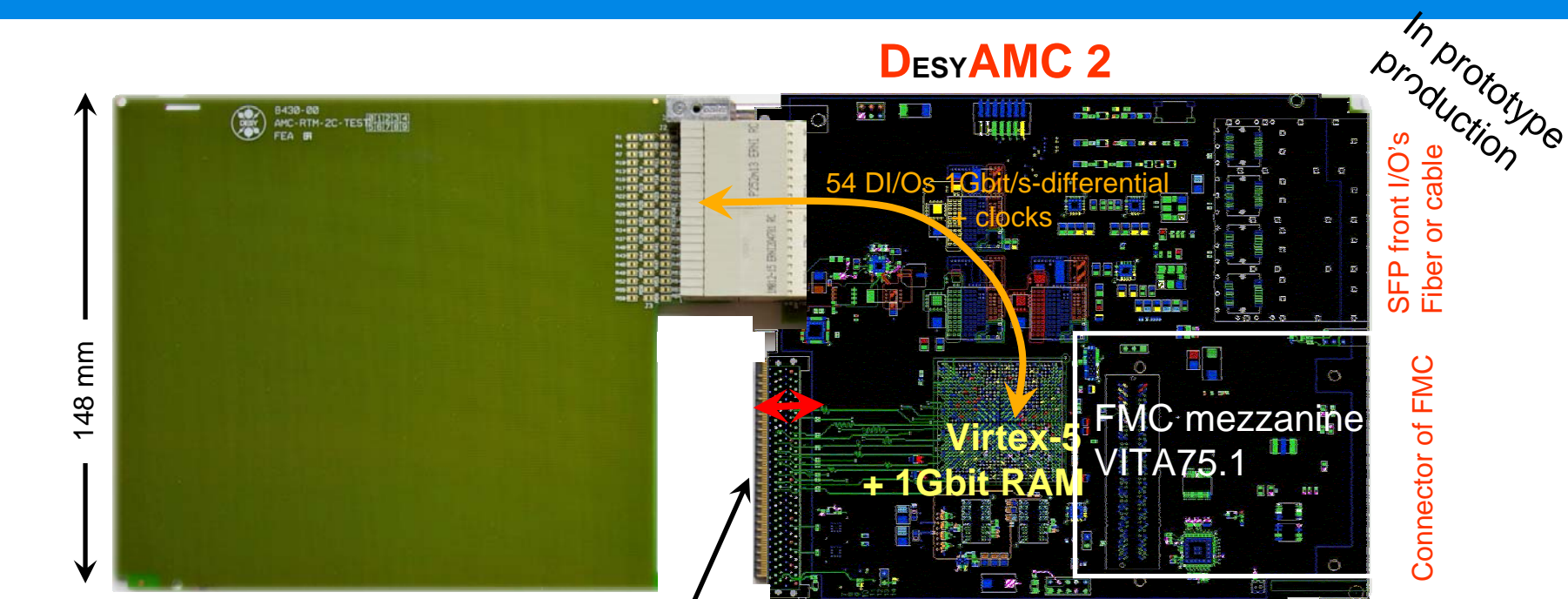
uTCA crate for XFEL

- > Crate picture
- > CPU module
- > Timing module
- > Backplane: which specialities
- > Redundancy: >99.999% availability

Rehlich:
what is public?
what is like to be presented?



XFEL standardization of AMC boards



RTM: Rear transition module

- User specific hardware
- Simpler design
- ADC's, test pulser, shapers, Custom I/O's

DESY-AMC1

as real prototype

Virtex-5, RAM, 125MS/s ADC's and DAC's

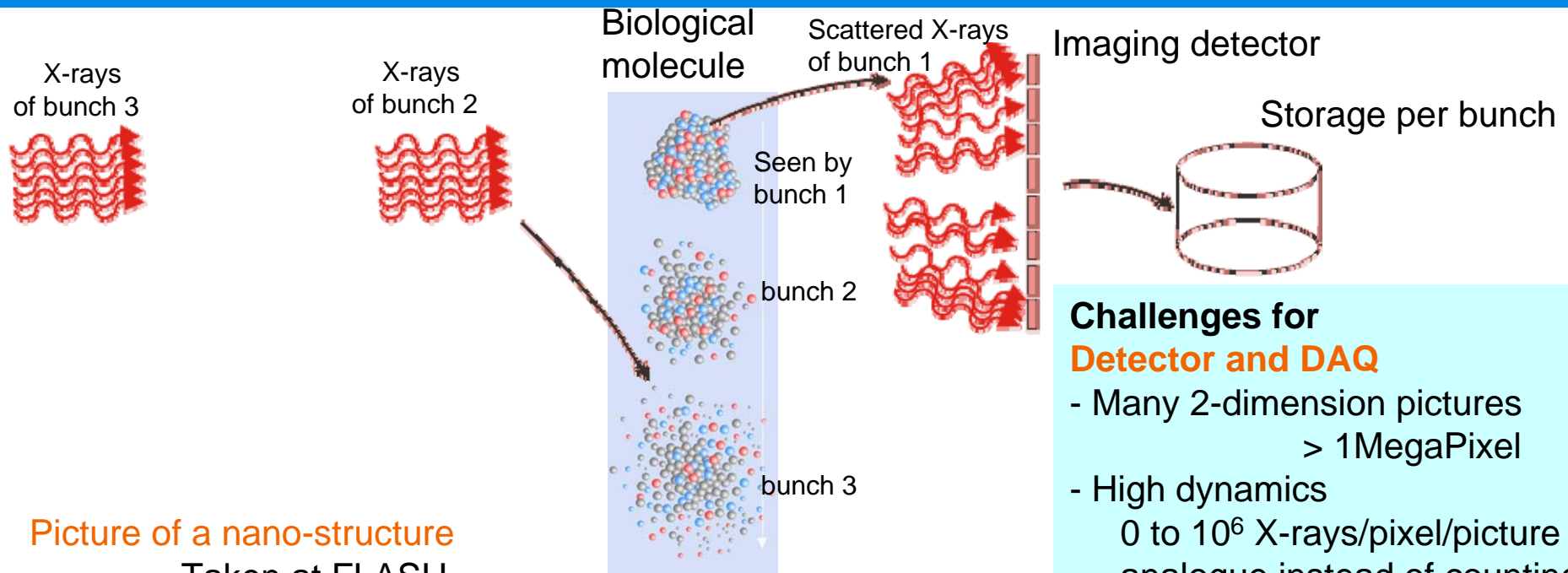


AMC: Front boards:

- double width standard
- A few standard hardware developments: digital interface, ADC's, carriers
- custom and industrialized designs
- Code as VHDL hardware drivers + higher level (MATLAB) user application



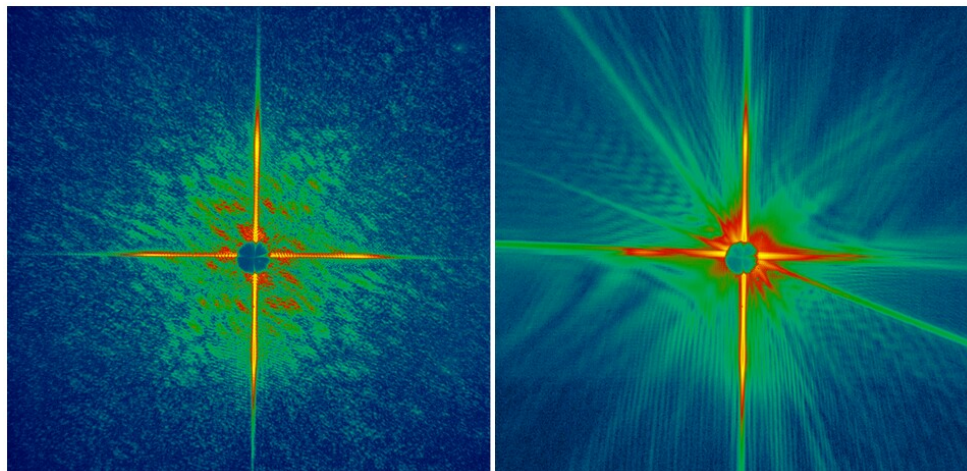
Detectors for the dream: 2-dimensional Cameras



Picture of a nano-structure
Taken at FLASH

First hit

destroyed target



Challenges for

Detector and DAQ

- Many 2-dimension pictures
> 1MegaPixel
- High dynamics
0 to 10^6 X-rays/pixel/picture
analogue instead of counting
- Fast storage (1st stage):
222ns @ XFEL
- Data rates ~80Gbit/s
- Selecting good pictures?

Information are in the details

- only lossless data compression
- high contrast
 $n_{\text{photon}} = 0, 1, 2, 3, \dots$ to be distinguished
for high signals, better than statistics

$$\text{resolution} < \sqrt{n_{\text{photon}}}$$

User requirements

Order of magnitude ↓		Different physic cases					Requirement to detector:	
		Pump/probe none crystalline	Pump/probe crystalline	Coherent diffractive imaging	Single Particle Imaging	X-ray Correlation Spectrosc.		
Photons and radiation								
E _{photon}	keV	6-15	12	0.8-12	12.4	6-15		500 μm Si
Quan. Effic.	%	>80	>80	>80	>80	>80		Exceed 1GGy at sensor surface
Rad. Toler.	10 ¹⁶ photons	1	1	2	0.2	0.02		
Geometry							Pixels 100-500μm	
Camera size	Target-angle	200 ⁰	120 ⁰	120 ⁰	120 ⁰	0.2 ⁰	Target-detector: 1-5 meters	
Pixel size	mrad	7	100μm	0.1	0.5	0.004	1mega-pixel	
No. of pixels	kilo x kilo pixel ²	0.5 x 0.5	3 x 3	20 x 20	4 x 4	1 x 1		
Dynamics for sensor and electronics							Demanding dynamics !	
Local rate	10 ⁴ photons /pixel/picture	5	300	10	1	0.1		
Global rate	10 ⁷ phot. /picture	3	1	1	1	1		
Elec. Noise+ dark-current	Photons /pixel/picture	<1	<1	<1	<1	<1	10 ⁹ e-h-pairs in less than a pixel	
Phot. spread	pixel	<1	<100μm	<1	<1	<1		
Picture rate	/train, /time	1, 10Hz	1, 10Hz	All, 27kHz	1, 10Hz	All, 27kHz	Possible total? Pict-pict: 222ns	

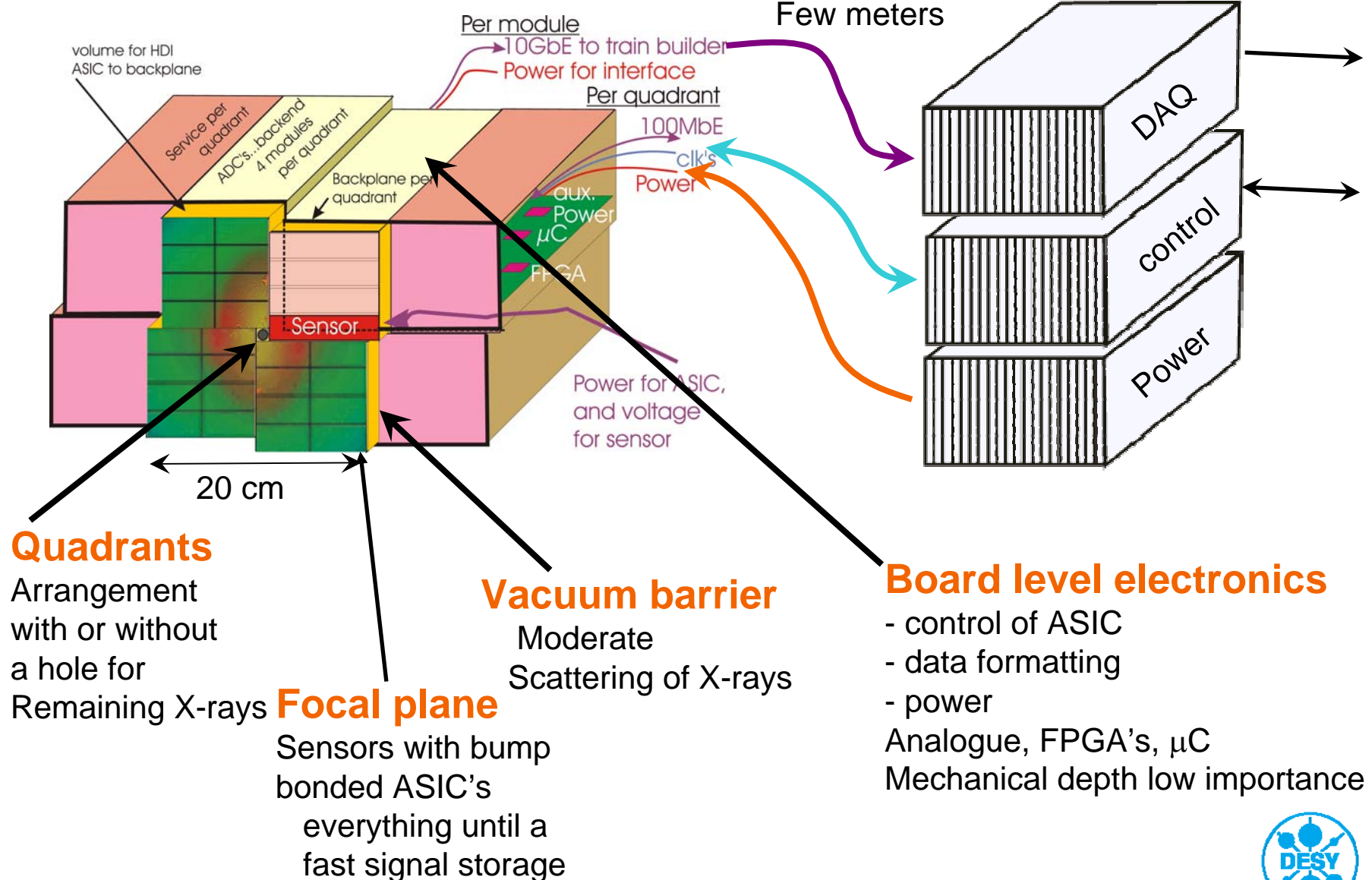
Need a few detector to cover all
Same challenges looks not feasible: compromises



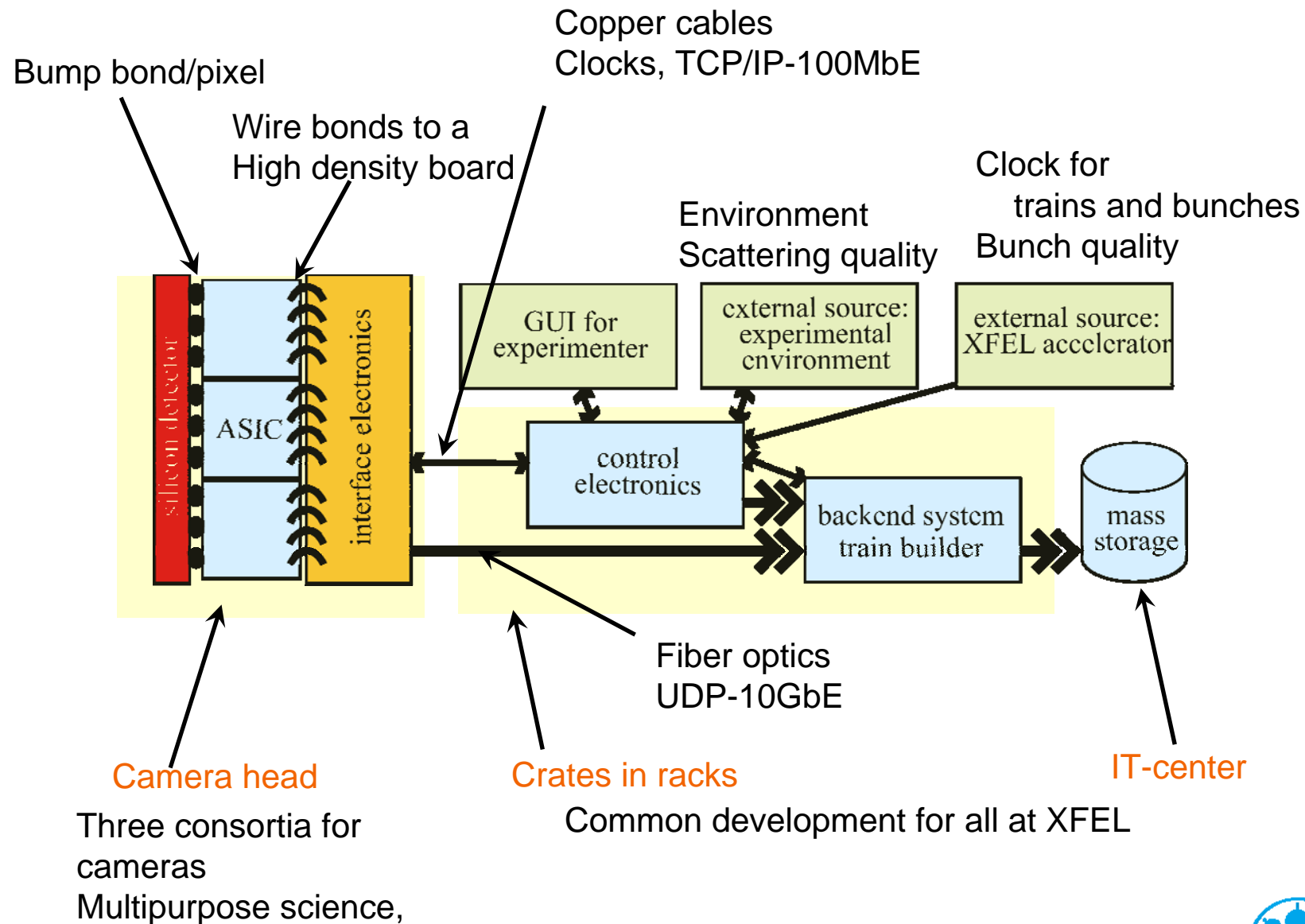
General detector concepts: Mechanical view

Camera head at the beamline

Crates in racks



General detector concepts: Electrical and Connectivity



Three consortia for 2 dimensional cameras

Each facing different physics by different technical approaches



Adaptive Gain Integrated Pixel Detector

Si-sensor with $200\mu\text{m} \times 200\mu\text{m}$ pixel

automatic gain selection in input stage for dynamic

analogue storage behind pixel, multiplexed analogue output of ASIC

Institutes: Bonn(University), DESY, Hamburg(University), PSI(Villingen)

Reference: B. Henrich, et al., Nucl. Instr. and Meth. A (2010), doi:10.1016/j.nima.2010.06.107

DSSC

DEPMOS Sensor with Signal Compression

Si-sensor with $236\mu\text{m}$ -hexagons

DEPFET integrated into pixel, non-linear design to compress the dynamics

low noise for low energetic photons

digitizing inside ASIC and digital storage behind pixel

Institutes: Heidelberg(Univ.) MPI-HLL Munich , Poly. Milan, Bergamo(Univ.) , DESY

Reference: G. Lutz, et al., Nucl. Instr. and Meth. A (2010), doi:10.1016/j.nima.2010.03.002

LPD

Large Pixel Detector

Si-sensor with $500\mu\text{m} \times 500\mu\text{m}$ pixel

three parallel gain stages for dynamics

analogue storage behind pixel, multiplexed digitizing inside ASIC

Institutes: STFC/RAL, Glasgow(University)

Reference: A. Blue et al., Nucl. Instr. and Meth. A 607 (2009) 55–56



Sensor

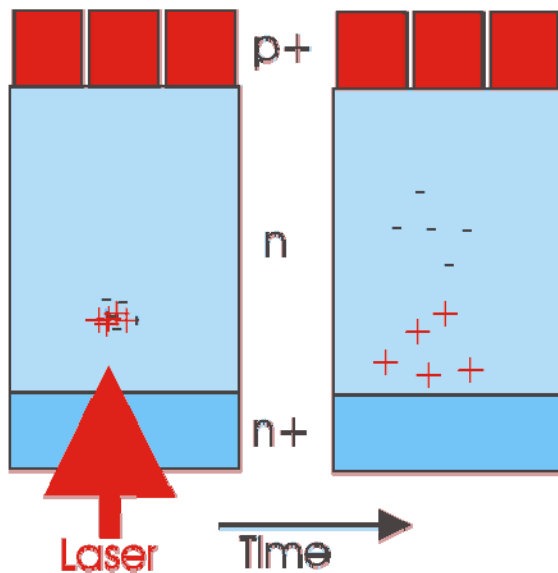
J. Becker, et al., Nucl. Instr. and Meth. A (2010), doi:10.1016/j.nima.2010.01.082

Charge explosion:

$3 \cdot 10^{16}$ charges/cm³

Electrostatic forces cause

Widening of charge cloud



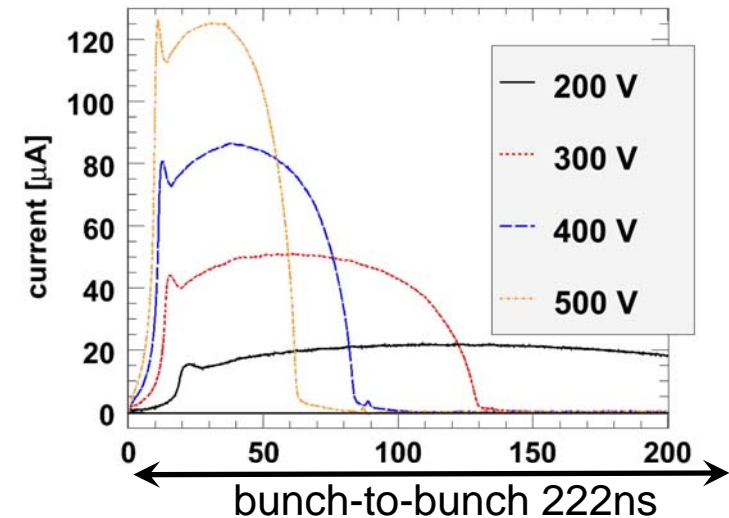
500V for 500μm thick Si-sensors

sufficient to keep charge

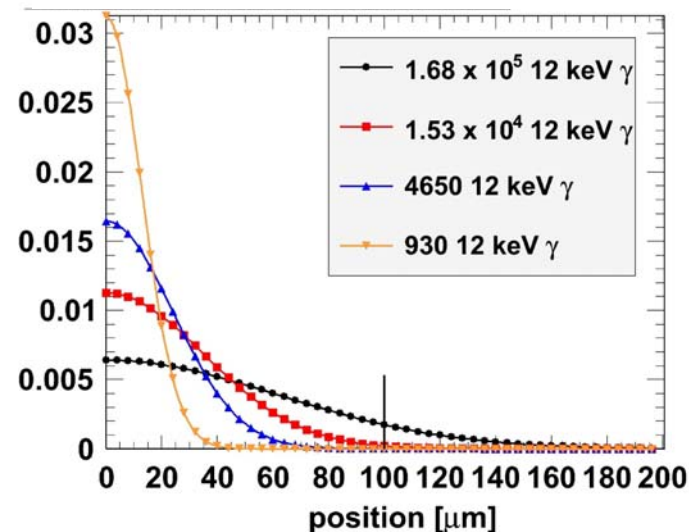
in pixel and in time of bunch

(200μm-pixel, 222ns/bunch)

Pulse shape for 450μm Si

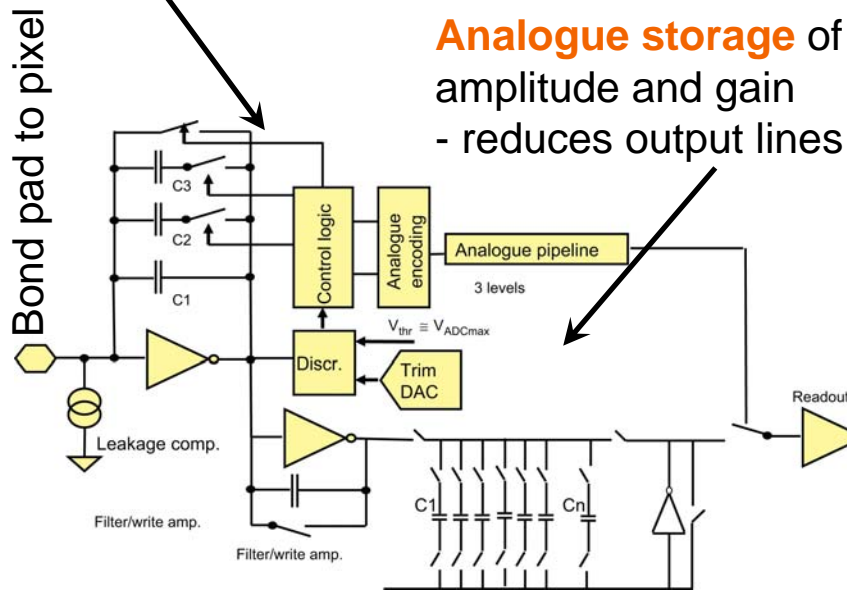


Lateral widening for different intensities

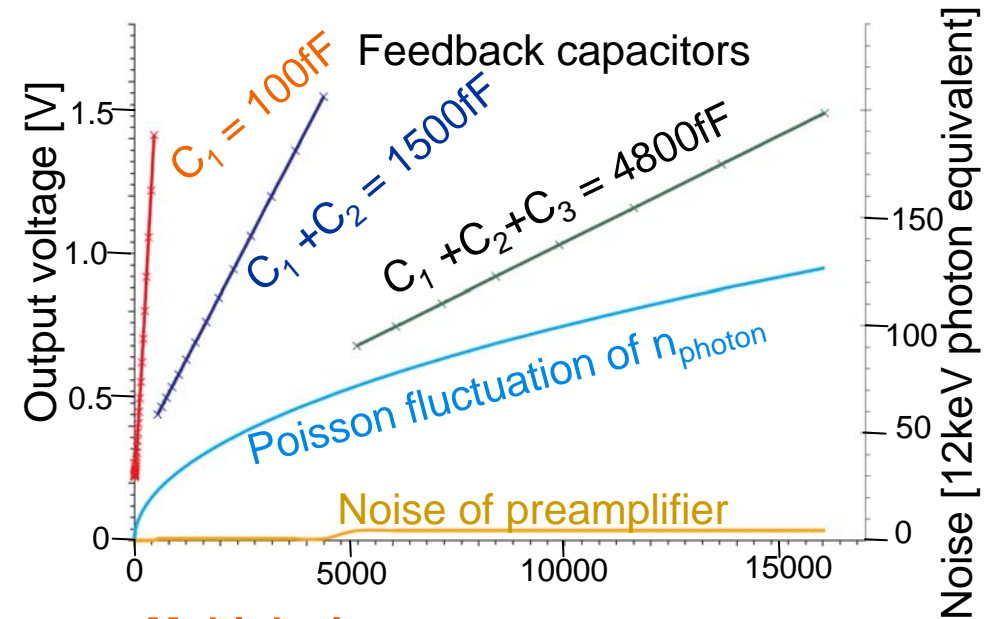


Automatic gain switch:

Gain switches,
when output exceed threshold
Adding instead of replacing C's
avoids charge losses



Analogue storage of
amplitude and gain
- reduces output lines



Multiplexing:

Just one differential output
For 32 x 32 pixels

Everything has to fit behind
The pixel 200µm x 200µm

Optimizing capacitors to store
maximum number of picture of a train
not all 27000 will be possible
realistic: ~ 200

random address overwriting
allows selection of best scatterings

Controlling and reading out the ASIC's

One sensor 512 x 128 pixel : 10.3 cm x 2.8 cm to one PCB-module

16 ASIC's bump bonded to it, each 4 outputs: 64 ADC's/module
connectivity and space!

16 modules for 1 Mega pixel

Digitizing as fast as possible to keep analogue storage time low

50MS/s 8-channel ADC's (medical imaging), 14 bit for <256 photons

0, 1, 2, ... has to be well separated

Activities synchronized to train structure of accelerator

Most critical
Within 8.8ms

Gain-bits on same
lines to same ADC's
safes connections
and space

Digital activity delayed by one train
- Allow access to full data for sorting, selecting
May be no activity while digitizing the critical values

Train of XFEL

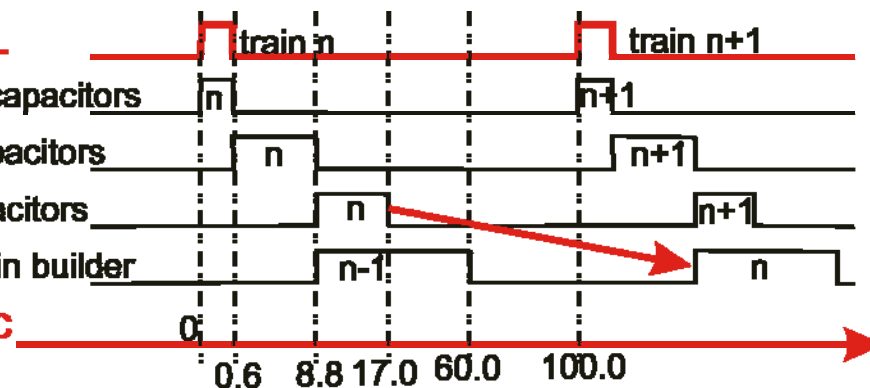
Signals into ASIC-capacitors

Digitizing value capacitors

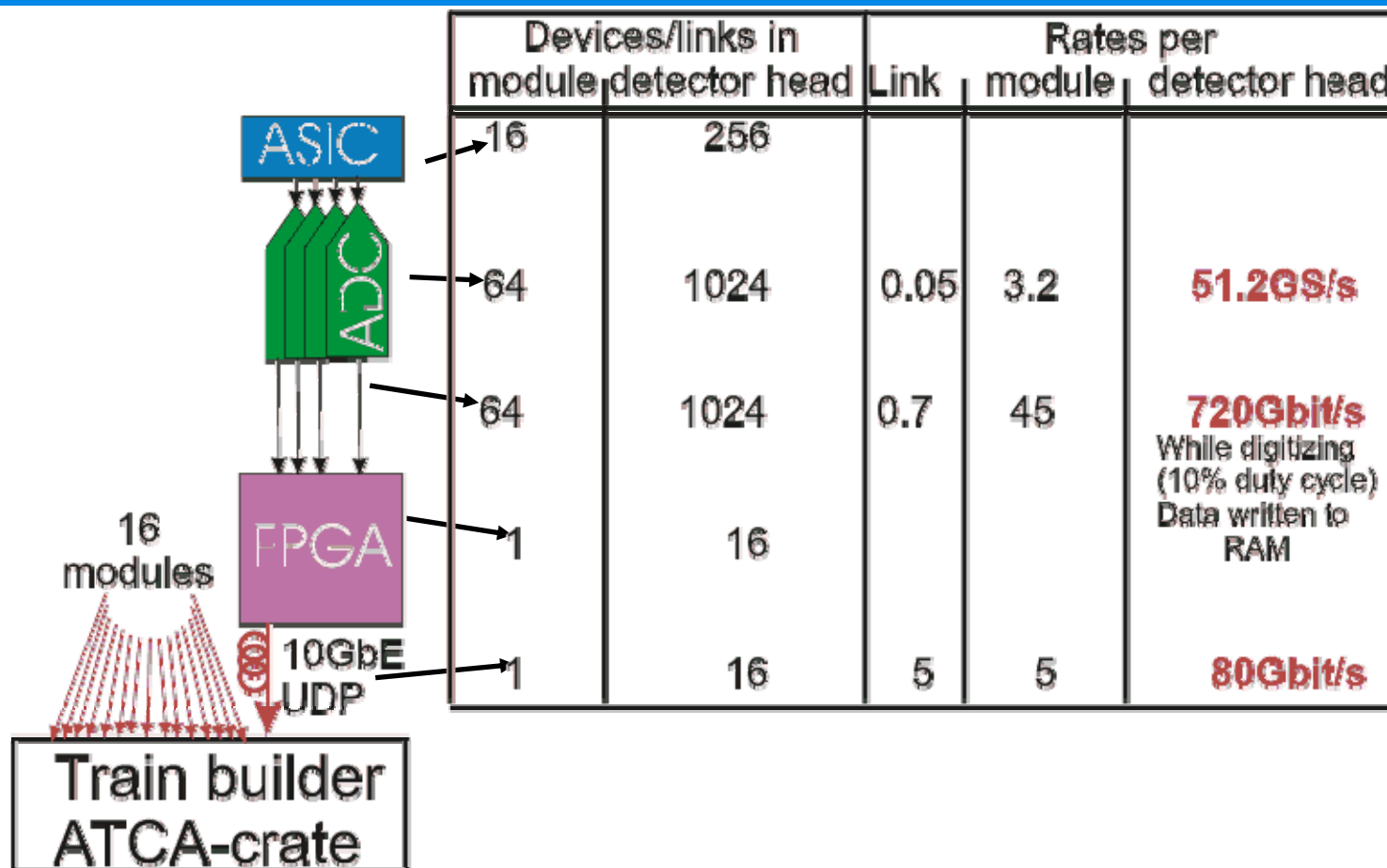
Digitizing gain capacitors

Data transfer to train builder

Time in msec



Signal rates



Very high internal data rates requires plenty parallel lines

Still high continuous data flow to crates:

require modern data transfers: 10Gbit/s on fibers

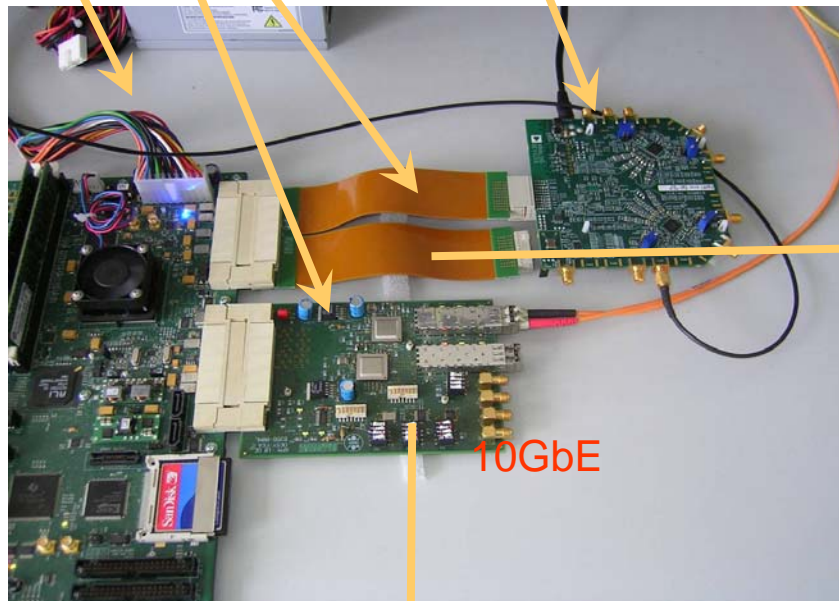
and high performace crate electronics: xTCA



Evaluation of high speed data transfers

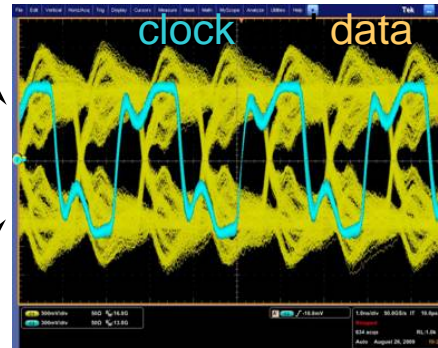


XILINX evaluation board + custom VHDL-UDP-core
+ custom designs + ADC-evaluation board

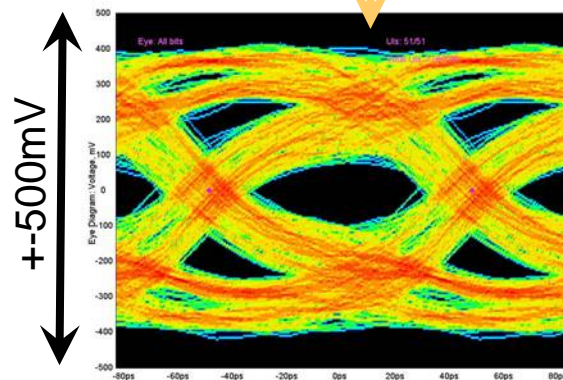


LVDS

ADC: 700Mbit/s



Performance limited by no-impedance
on XILINX-evaluation board

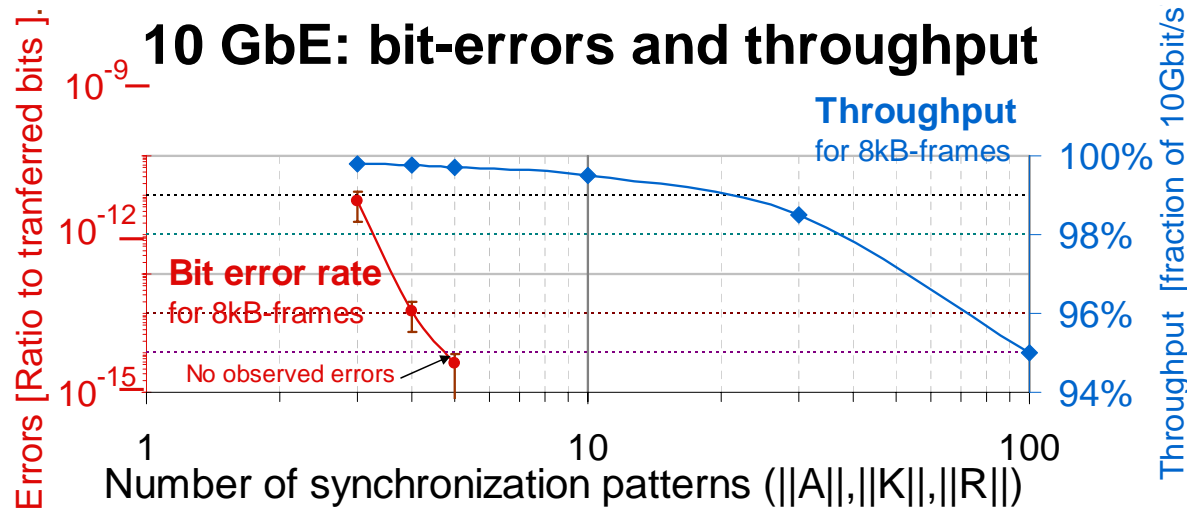


10 gigabit-Ethernet
... limited by
16GHz-scope

1bit@10Gb/sec



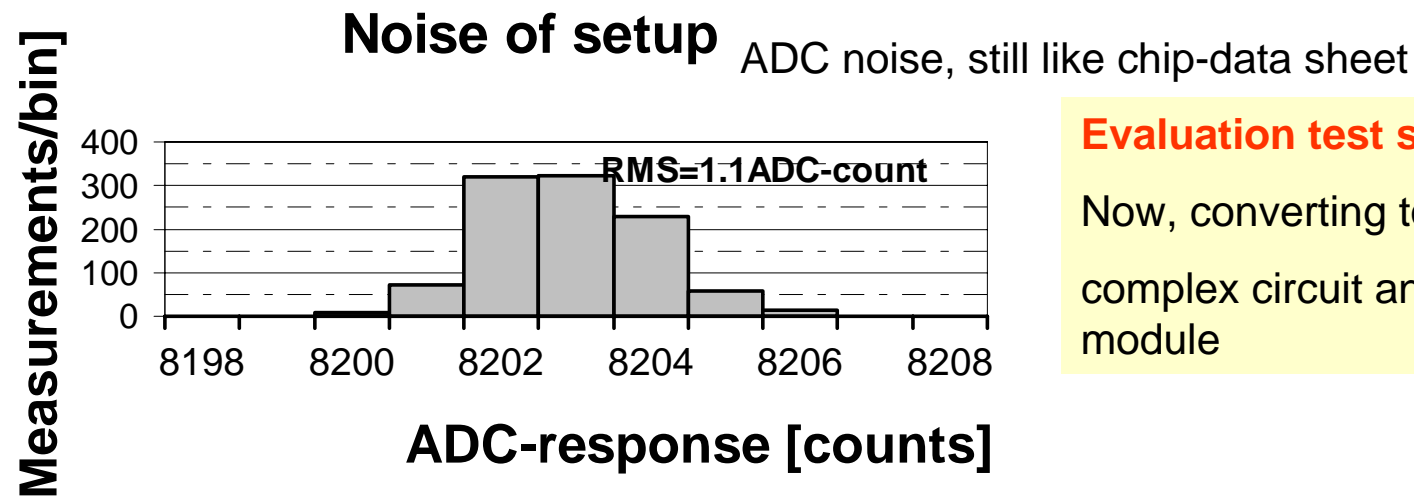
Performance of technical evaluation tests



~ 55% -efficiency needed

Measurement limit
converts for 80Gbit/s
to train losses
1 out of 20 000

OK,
also for using UDP
anyway no time to repeat
next train as good as lost

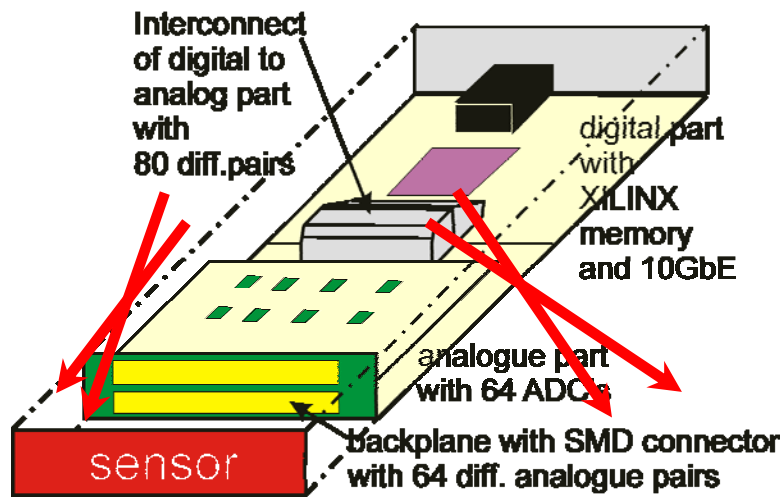


Evaluation test successful

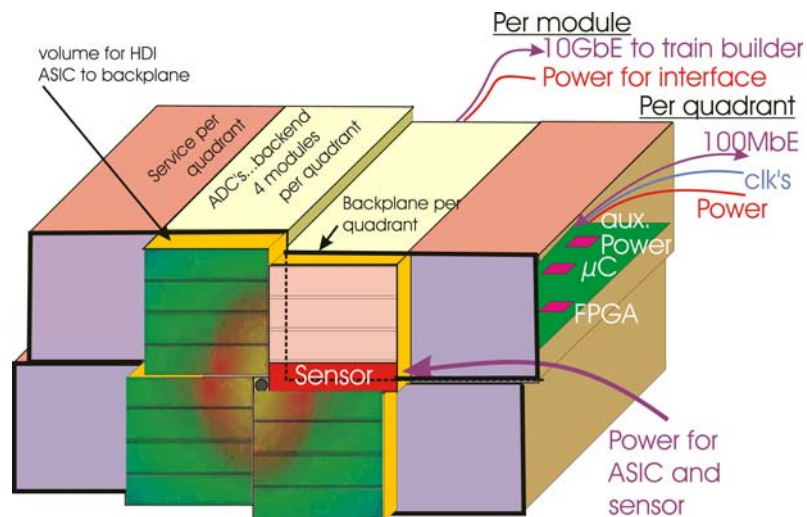
Now, converting to the
complex circuit and layout of full
module



Modular electronics of a module



Every part of a module fits behind sensor
 - stackable to 1MegaPixel and more
 Only common control/quadrant at the side

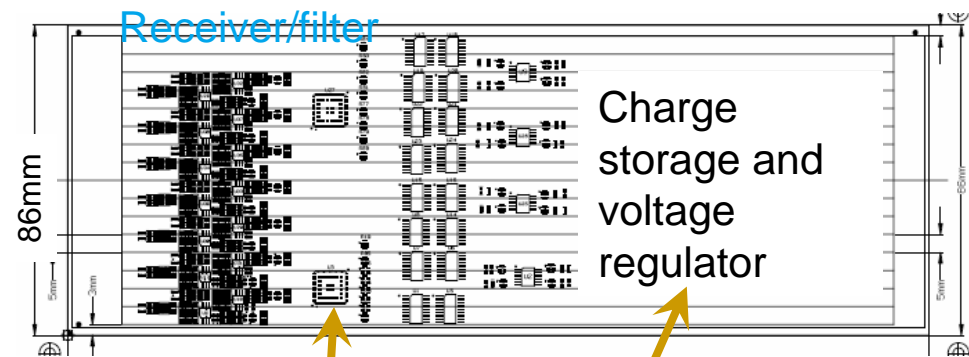


Using a **backplane** between sensors and Interface electronics as vacuum barrier and guiding common signals to the side

Separated digital and analog part

- performance has shown, that connector is no problem at 700Mbit/s
- Therefore possible
- Disentangled developments, versions

Compact analog part by two parallel PCB's, But still a dense layout of 16 filters/ADC's each side



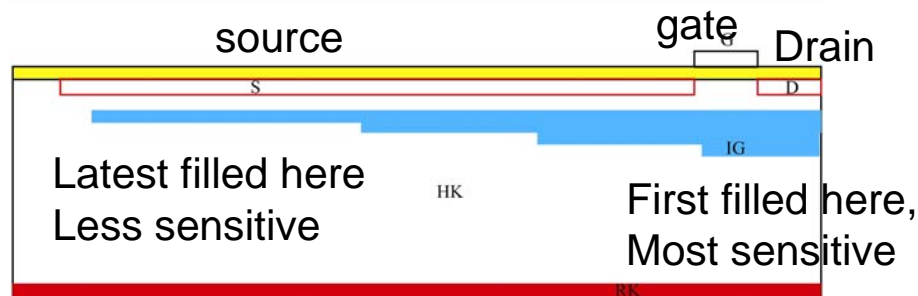
2x 8 channel ADC's

Trained operation requires stabilization of current and voltage



Allowed to tell?
What else?
What different?

Inside pixel a DEPFET with none-linear behavior



- Operation of 1 mega-clear gates
- ADC/pixel : 8 bits within 222ns for dynamics up to 10000 X-rays
- storage depth: 256 in DRAM behind pixel

LPD: Large Pixel Detector

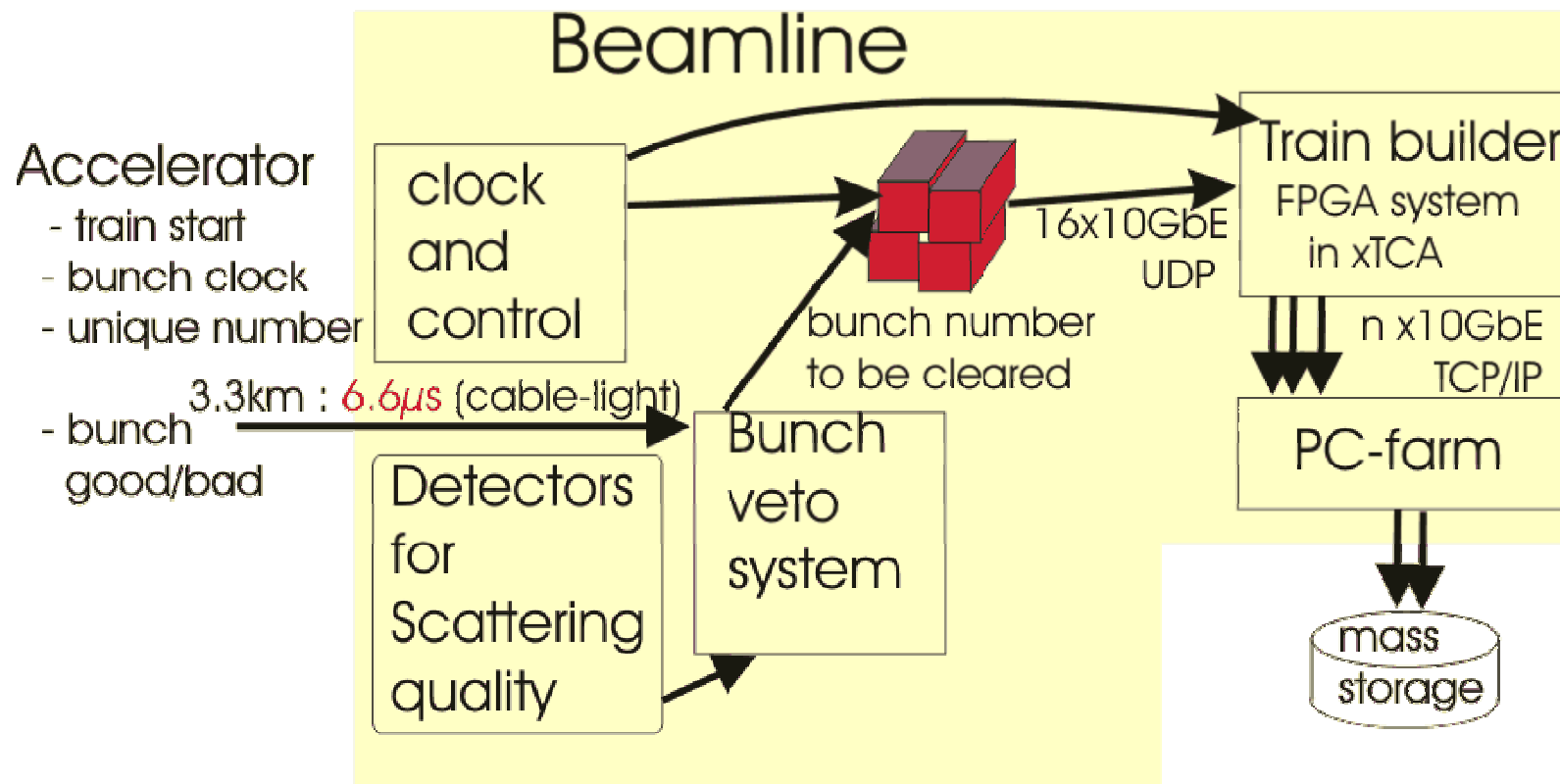
Larger pixel: more storage cells: 500

Challenges: Keeping noise low

Handling larger focal



Detector and control and backend



Beam line integration:

hard clocks

- synchronisation to beamline
- veto: none of the cameras can store each bunch: 200-512 out of 2700

Usage of best bunches by vetoing: delay from electron-source to beamline 6.6μs
anyway very late ⇒ random delay

TCP/IP from control: boot, monitoring, updates

High data stream to train builder



Concept for clock and control

Drawing from Chris



The veto system

I can do

Input from
Chris?



Concept of the backend

Drawing
from Chris



Status of the project

- > Civil engineering started begin 2009..... picture
- > XFEL-GmbH: Company founded November 2009
- > Plan operation 2015

