

Questions and Answers from 22-Jun-2010 meeting

23.6.2010 v1 CY

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1 Attendance

WP76: D.Wilson and C.Youngman

WP28: K.Rehlich and P.Gessler

UCL: E.Motuk, M.Wing, M.Postranecky and M.Warren

2 Questions and answers

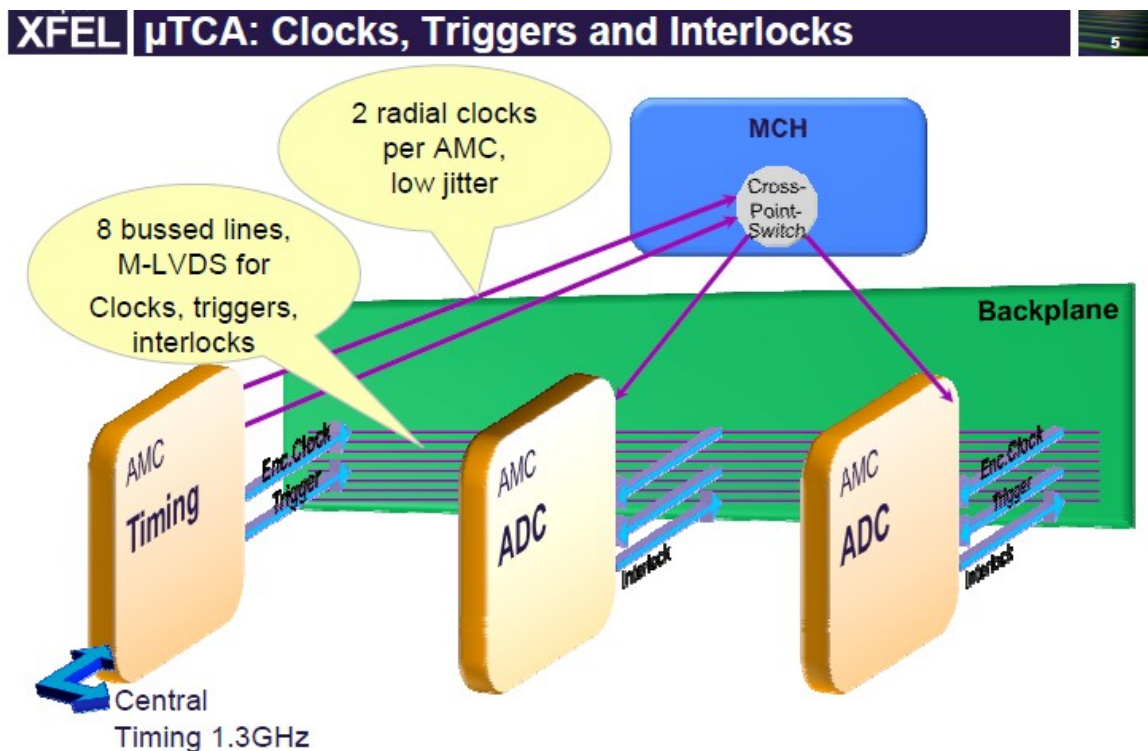
Your draft specification was a little thin

Well you can be happy that I did something at all!

Are users of the Timing Receiver (TR) board supposed to use the back plane to get access to the timing information?

The example crate sitting on the desk is an ELMA six slot xTCA crate. The backplane in the crate is very close to the final xTCA spec. This crate's backplane does not include a minor change/update which the final standard has. People buying a xTCA crate will get a standard xTCA backplane – it is not a custom backplane.

People who have ordered (e.g. WP76) the preliminary standard xTCA will get the pre-standard backplane, but the difference is on p2p lines used by specific users like LLRF and, at SLAC, interlock systems. This is not a problem – if it is order a new backplane (2k€) or entire crate.



Returning to the question: where should TR users get the timing information?

Look at slides 5 in KR_IEEE_xTCAtiming.ppt, see above, which shows how ADC slave cards receive timing information over the backplane. The ADCs shown receive low jitter clocks via p2p links and trigger and other information through bussed lines.

The xTCA standard foresees two radial p2p high precision clock lines with jitters ~few ps. These clocks are configurable and the CC master (user of TR like an ADC) can receive its 4.51 MHz bunch clock from the TR using one of the p2p links. The timing system ensures that the bunch clock is correctly synchronized. The TR board can be configured to deliver any clock frequency generated from the 1.3GHz input.

If the machine is running with 4.51MHz or 1MHz or any other bunch clock this will be configured at the TR, using information telegrams encoded on the 1.3GHz input to the TR, and is not a user configuration option.

Can you read out from TR memory the TR side configuration (configured via input fibre encoded data)?
Yes, but usually you use this to readout configuration information (pulse patterns, etc.) but not the frequency. The frequency is probably stored somewhere.

The central 1.3GHz is always the same?

Yes at XFEL, at FLASH the new timing system will be run in parallel at 1.3GHz – the choice of 4.51MHz bunch clock at XFEL is compatible with FLASH.

TCLKA and TCLKB described in the draft specification are the two p2p lines described?

Yes, TCLKA and TCLKB are the official xTCA standard names.

Are the frequencies of TCLKA and TCLKB fixed or configurable?

You can select in the TR via control software. The control software is part of the TR installation, but it must be interfaced to whatever control software is used by XFEL.

What are the eight non p2p lines shown on the slide?

These are eight bussed timing distribution lines with higher jitter, say ~100ps, and lower quality than the p2p lines due to multiple users connecting to them (typical bus line problems)

The bussed clocked lines used by the TR are configurable (can be disabled) allowing other usages of the lines?

Yes, the eight lines are free for other users – they are LVDS wired OR.

The TR can be configured to use bus lines to carry the encoded event messages (train #, start, bunch sequencing # (also known as bunch pattern index), etc.). User boards, like CC master, should take off the information they need by looking for the appropriate command opcode using a firmware decoder like Sam's LPD CC Manchester decoder.

No protocol has yet been specified for the bussed lines when used by the TR, users are encouraged to make proposals about what this should be: Manchester...

The p2p lines are LVDS clocks no data is encoded on them and they need no encoding.

The p2p lines are in the micro-TCA standard, the bussed lines not. Both are in the xTCA standard.

Does the CC system need the p2p clocks, or can just the bussed lines be used?

It is simply a question of what jitter is acceptable. The p2p connection is independent of other user boards – with the bussed lines there is some degradation of signal quality when extra boards are added.

What is the maximum TR p2p frequency, 1.3GHz?

LVDS cannot transport 1.3GHz, maybe 600MHz is possible.

One TR p2p can be specified as the bunch clock frequency and the other could be set to 108MHz?

Yes.

Does the xTCA standard specify the p2p and bussed lines as LVDS differential?

Yes.

Note that the front panel IO channels are not specified by the xTCA standard. The AMC form factor prototype TR (2009) had 1 SFP+ fibre for the 1.3GHz input signal and 4 copper (Harling) connectors. If no one requires front panel connections then they will be removed from the TR design – user feedback is required. Note that one output is required to daisy chain TR boards together, the number in the chain is not limited but the jitter worsens. The CC usage plans for the TR should be documented and given to the XFEL timing group.

We need TR boards for testing, can we get some and when? We asked for two?

Yes, a production run of 20 “final” TR boards is being prepared: components are there and the soldering is planned. The firmware is still to be worked on.

Yes, you can have a pair (meaning two they do not come in pairs).

How can the TR boards be tested without the 1.3GHz input, are there any configurable self drive features including event generation?

An external clock 1.3GHz signal must be generated – could use the crate PCIe 100MHz clock and PLLs to generate whatever is required. The TR has receiver and transmitter on board – this was stated twice but what does it really mean add new data to encode and send out on fibre or copper connections or bus lines??

To simulate XFEL operation we need a 1.3GHz clock with data encoded on it?

Yes, could create new firmware to generate the data message required.

Do not like the idea of running different firmware.

Then you need TR two boards (possibly in the same crate) one driving the other with different firmware.

Does a simple test driver system exist – it could be replicated?

We are at an early stage and the firmware currently allow configuration of most of the board chips. No test system exists.

Is there a specification of the timing (telegram) information and who will define it?

Not really because everything is programmable so this is not considered a priority item. The draft spec contains a list of telegrams which are expected to be implemented.

Does the CC have any additional “unexpected” requirements regarding timing telegrams?

Not at the moment, we need a start ≥ 15 ms before train arrival and train end telegrams.

At XFEL the start signal precedes the first bunch by ~ 30 ms which is required for the wire scanner which will be a problem for running at 30 Hz, so the CC ≥ 15 ms requirement is easily satisfied.

The p2p bunch clock configured is continuous?

Yes, but a flag can be set to make it a burst (during train delivery) rather than continuous if required. Delays can also be configured.

The Peter Goettlicher question comes up – is the p2p clock continuous?

Yes, this is the current understanding – please mention it again in the CC side specs.

How does the CC access the telegram information?

One way would be to read out the TR memory by the interrupted (PCIe TR generated) CPU and then send this to the CC. Another way, and probably the favoured way, would be for the CC master to pick off the telegram data payload for the command opcode of interest from one of the backplane bussed lines.

Are there any thoughts about using two bussed lines one for trigger and the other for data?
Yes, this as a configurable option is considered.

What telegrams are defined?
These are tabulated in the draft functional description.

What goes on the encoded bus line, is it the all telegrams?
Yes, all telegrams (command opcode and data payload) appear on the bussed line(s). The user boards just pick out what they need leaving the rest unprocessed.

How many bussed lines are free for user usage?
There are 8 lines. The TR needs 1 for the telegram distribution (assuming it is required/configured) and clock distribution (of worse jitter ~100ps), so the user might use up to 7 lines.
Note that no arbitration mechanism is defined to prevent two boards writing to the same bus line at the same time – maybe this should be further specified in the xTCA standard. The MCH does not know about the xTCA bussed timing lines.

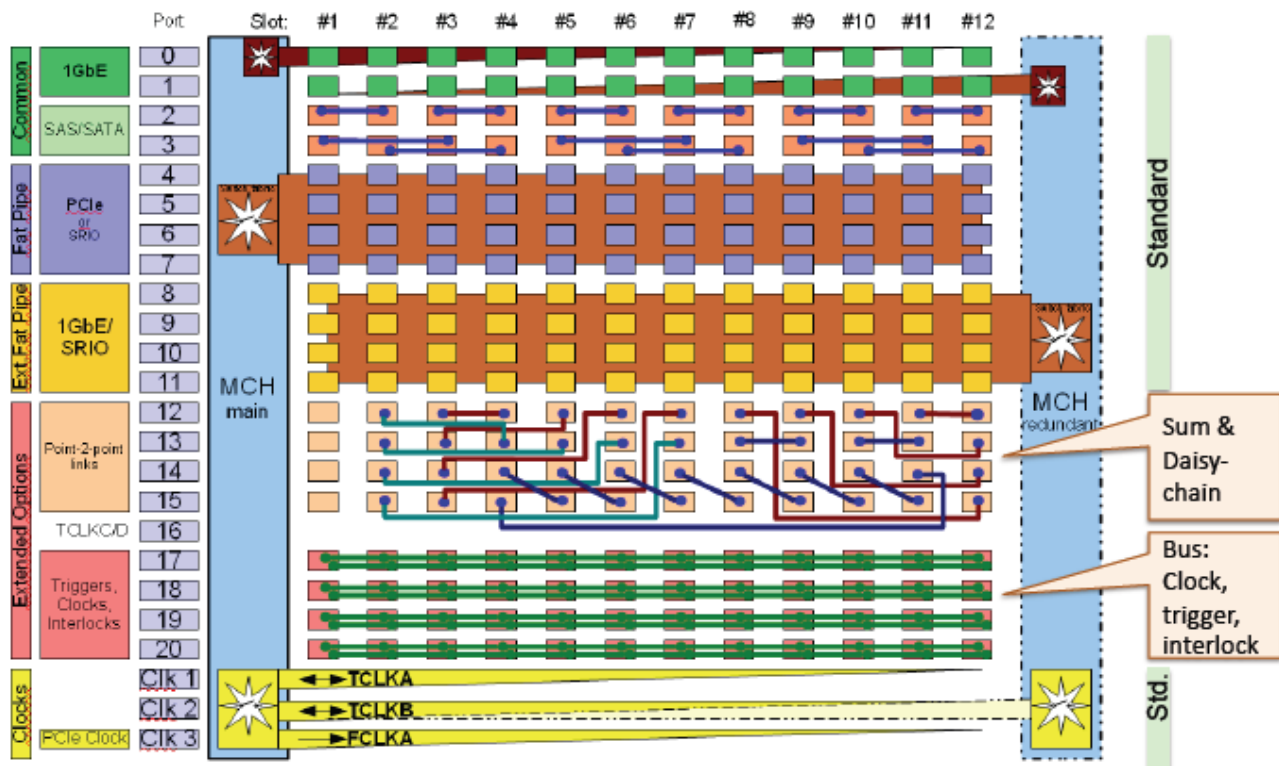
What will the CC use the non TR bussed lines for?
Known usages now are to distribute BUSY and similar signals. It is possible that other items will be added later. It would be possible to use one of the bussed lines for the status return from the slaves.

What happens if there are not enough slots in a crate, can you have crate extenders?
You need a solution, an extender board coupling the crate...

Does the xTCA standard foreseen additional p2p links beyond TCLKA and TCLKB?
Yes, additional bidirectional differential LVDS 3Gbps lines are available (cannot blow up the hardware). There is a free area which conforms to usage rules. Where are the additional p2p lines on the final 22.6.2010 xTCA schematic below (source: Backplane_discussion_22_6_2010.pdf)?

Backplane Status

Kay Rehlich (DESY), 22.6.2010



What protocol is used to access the datagram information for the current train in the TR board?
 PCIe accessing a given memory region within the boards address space. This data is available to the DOOCS control software or other software interfaced to DOOCS.

When the WP76 crate arrives we want to start running tests and this will need to interface our software to the DOOCS server software. Is this plan OK?
 Yes.

If firmware for decoding the datagram on the bussed lines is written we would like to use it.
 Yes, but why not write it and make it available for others – could Sam do this in Sept thru Dec at XFEL?

Is both the sequence # (index) identifying the bunch pattern and the pattern itself sent?
 Yes, probably both are sent as separate datagrams. Users exist for both.
CC should work out a prioritized list of datagrams required by ~Sept, i.e. the next TB and CC meeting, and give it to the timing group.
 It is not planned to have a global definition meeting, user groups should define what they need to the timing group.

The CC should use the backplane p2p and bussed timing lines, but how does one connect non XFEL timing systems requiring two inputs: bunch clock and bunch trigger? Can the TR be used to interface

other timing systems, e.g. Petra 3, which have a bunch clock and a trigger signal.? [CDR = clock and data recovery (chip)]

The important information is that the Petra 3 timing group are interested in joining the TR development effort – so the CC could use the TR interface similar sources and the small crate DAQ system could also use this solution.

To get it to work: “need to take a clock in and produce another clock” and “to take the trigger and delay it to produce another trigger”.

How to get the bunch and trigger signals from Petra 3 into the TR?

Use the copper inputs on the front panel – so there is a need for at least two front panel inputs from the CC.

Would control/configuration of input signal processing, like dividing, be part of the services provided by the TR developer group?

Yes. The firmware should allow selection of mode of operation – i.e. avoid have two different firmware versions. Maybe the CC could worry about generating events from bunch clock and trigger.

What is the time schedule for firmware development?

TR boards should be available in Sept. which broadly defines when firmware work can start.

Are the Petra 3 group capable of writing FPGA code?

Yes, at what level is uncertain and they used Altera FPGAs previously.

We should convince them to do it – ask them (J.Klute and Herr Huerdelbrink) tomorrow.

Are the design schematics of the TR available online?

No, external firms are interested so care is required. If special questions need to be asked then ask a developer.

How many timing lines are used by the STRUCK SIS 8300 ADC board?

Depends on the application. TCLKA and TCLKB are connected, clock from front and RTM, same interface to FPGA(?) can do interlocks.

Are people interested in a 12 slot xTCA crate – looking for people to join an initial order of five 12 slot crates?

Thank you for the offer, but we probably will not order a 12 slot crate in the near future – we will think about it.

The xTCA crate has a large area RTM, is this useful for the CC?

Really depends on what you want to do – more real estate is available especially on the RTM. The year old micro-TCA crate of UCL is not compatible with xTCA.

Extenders are available from NAT that allow single board running.