XFEL Timing System

Status 7.2008

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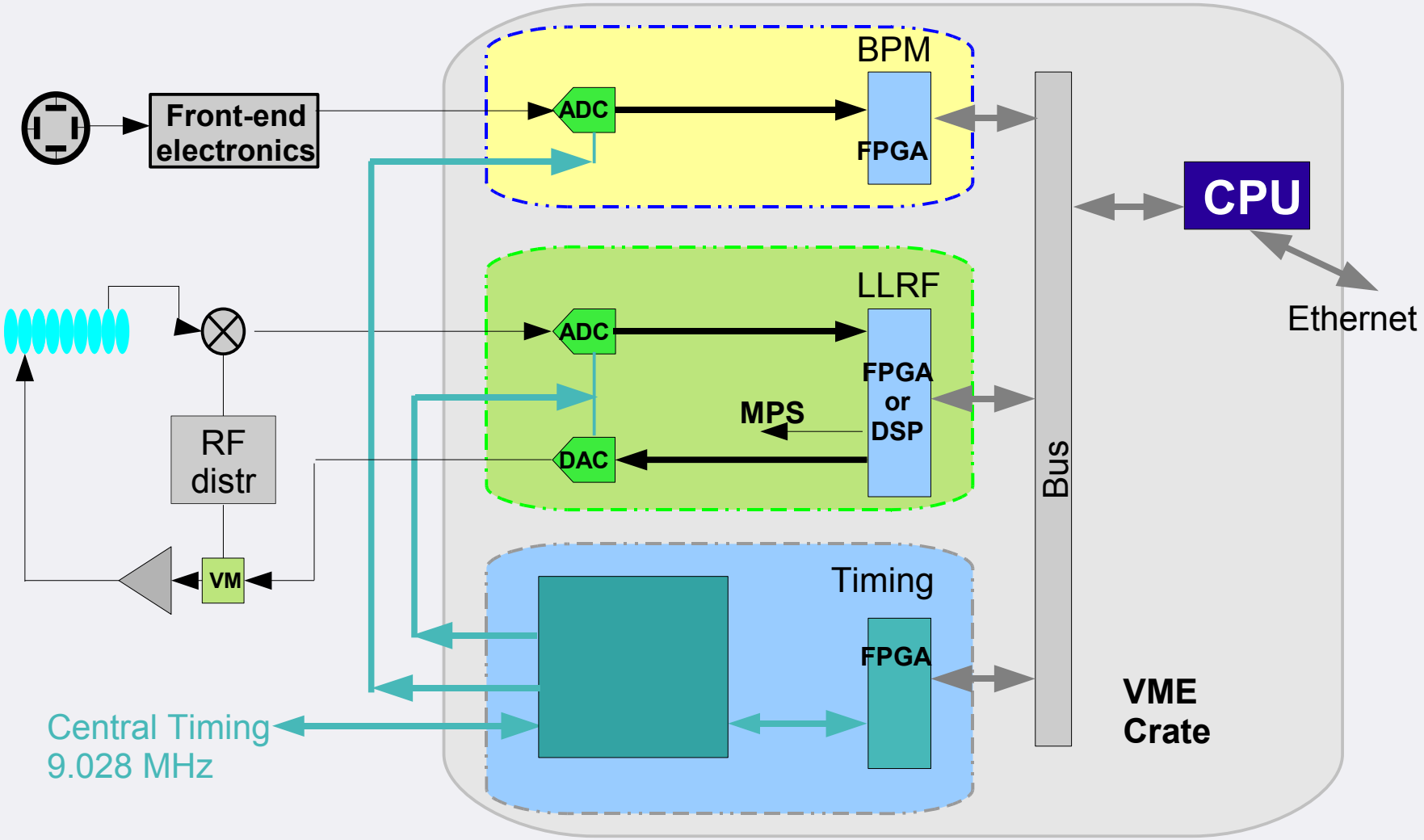
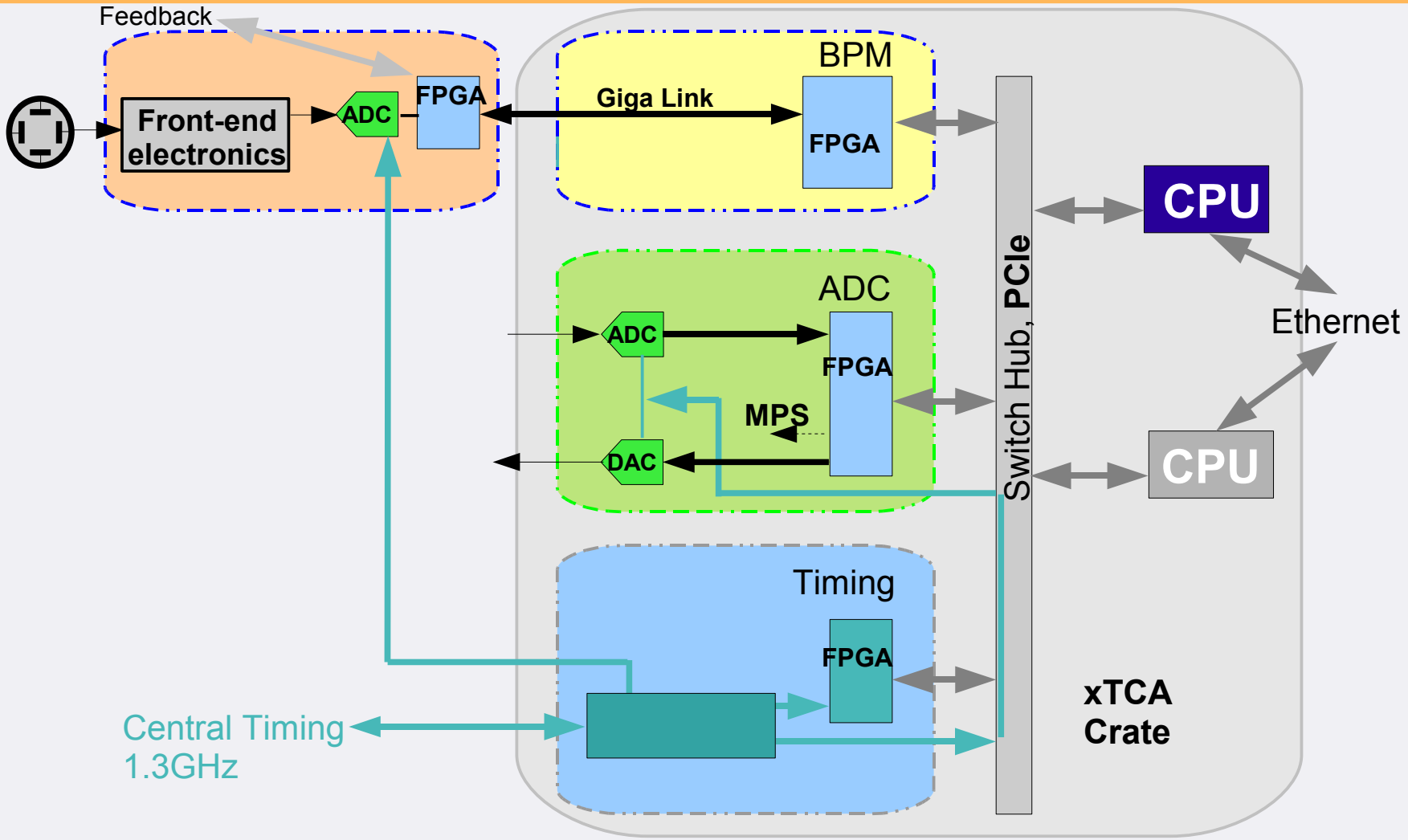
The Front-end: FLASH Example



The Front-end: XFEL Examples



Data Acquisition

Hardware:
receives clocks or patterns, triggers

to synchronize the bunches (ps stability)

RF/Diag
ADC
FPGA
clock
trigger
FPGA
Timing
PCIe
CPU
xTCA
Ethernet
Middle layer server
CPU
Tunnel

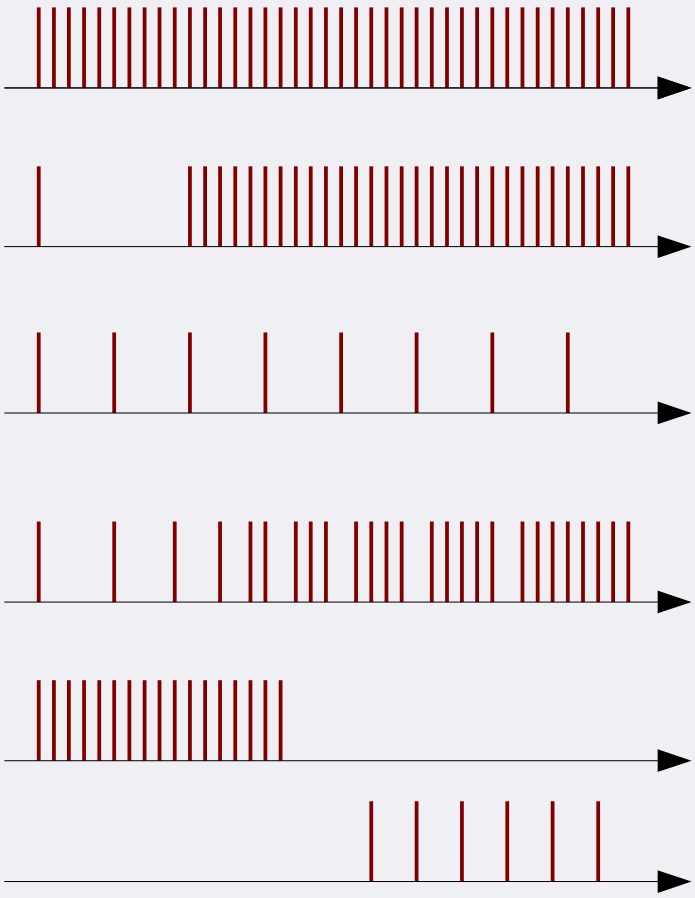
Data Acquisition

CPU:
receives event numbers, interrupts, modes

to synchronize the macro pulses for DAQ

RF/Diag
ADC
FPGA
clock
trigger
FPGA
Timing
xTCA
CPU
Ethernet
Middle layer server
CPU
Tunnel

Possible Bunch Patterns



Max: 5 Mhz, 3000 bunches

Pre bunch

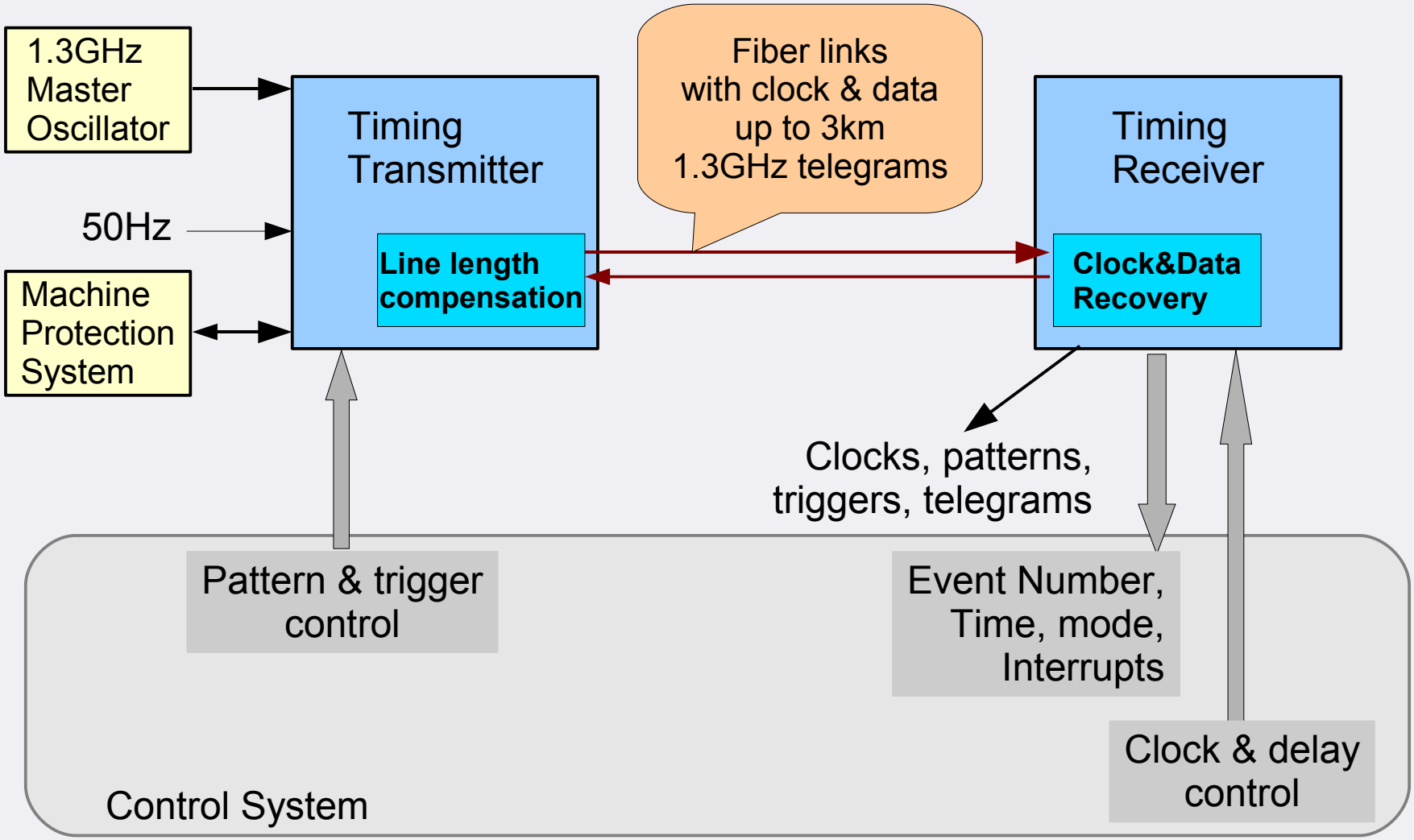
1 Mhz or lower frequencies

Arbitrary patterns

Different patterns @ different beamlines in one macro pulse

or varying patterns from shot to shot

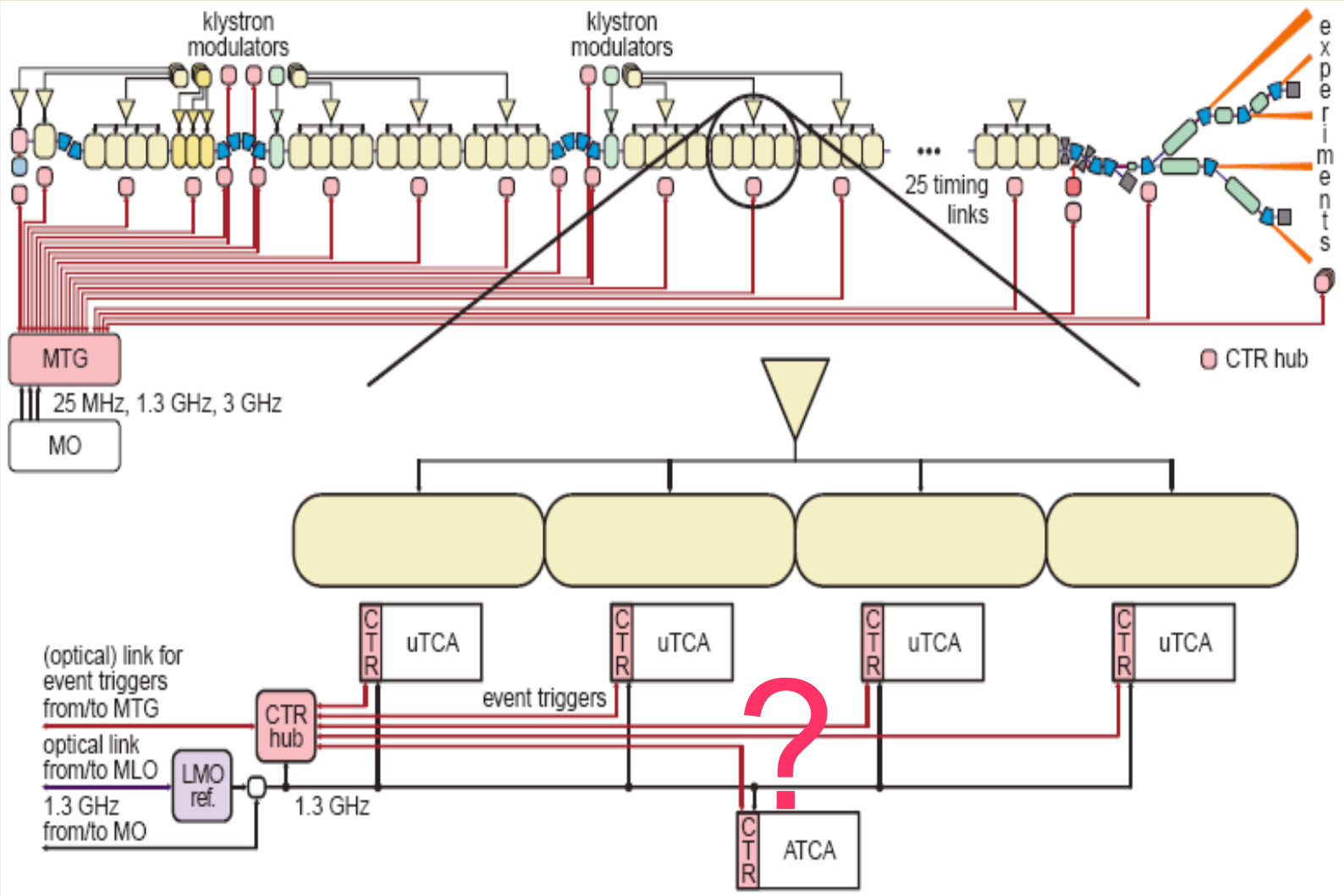
Timing System Blocks



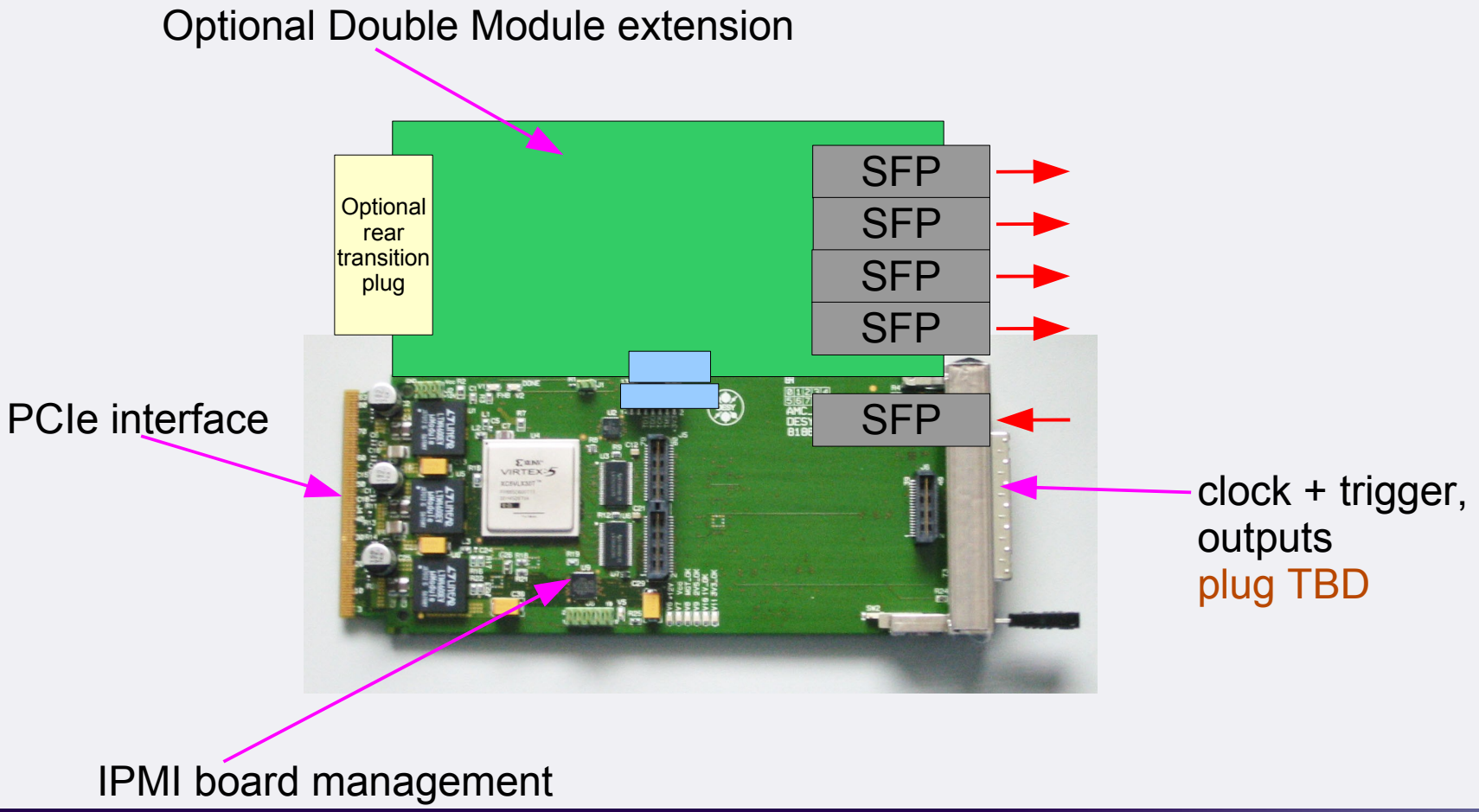
Timing System Requirements

- **1.3GHz telegrams**
  - With clock recovery, few ps jitter
  - Events and data for triggers, event number, modes, bunch pattern, (bunch charge?), ...
  - Sender compensates cable length, drifts and measures time delay from sender to receiver
- **Timing receiver outputs (hardware)**
  - Raw telegrams
  - Clock (and gated clocks) on front and backplane
  - triggers
  - Level (LVDS, LVPCL,..) to be defined
  - Connectors to be defined (e.g. infiniband)

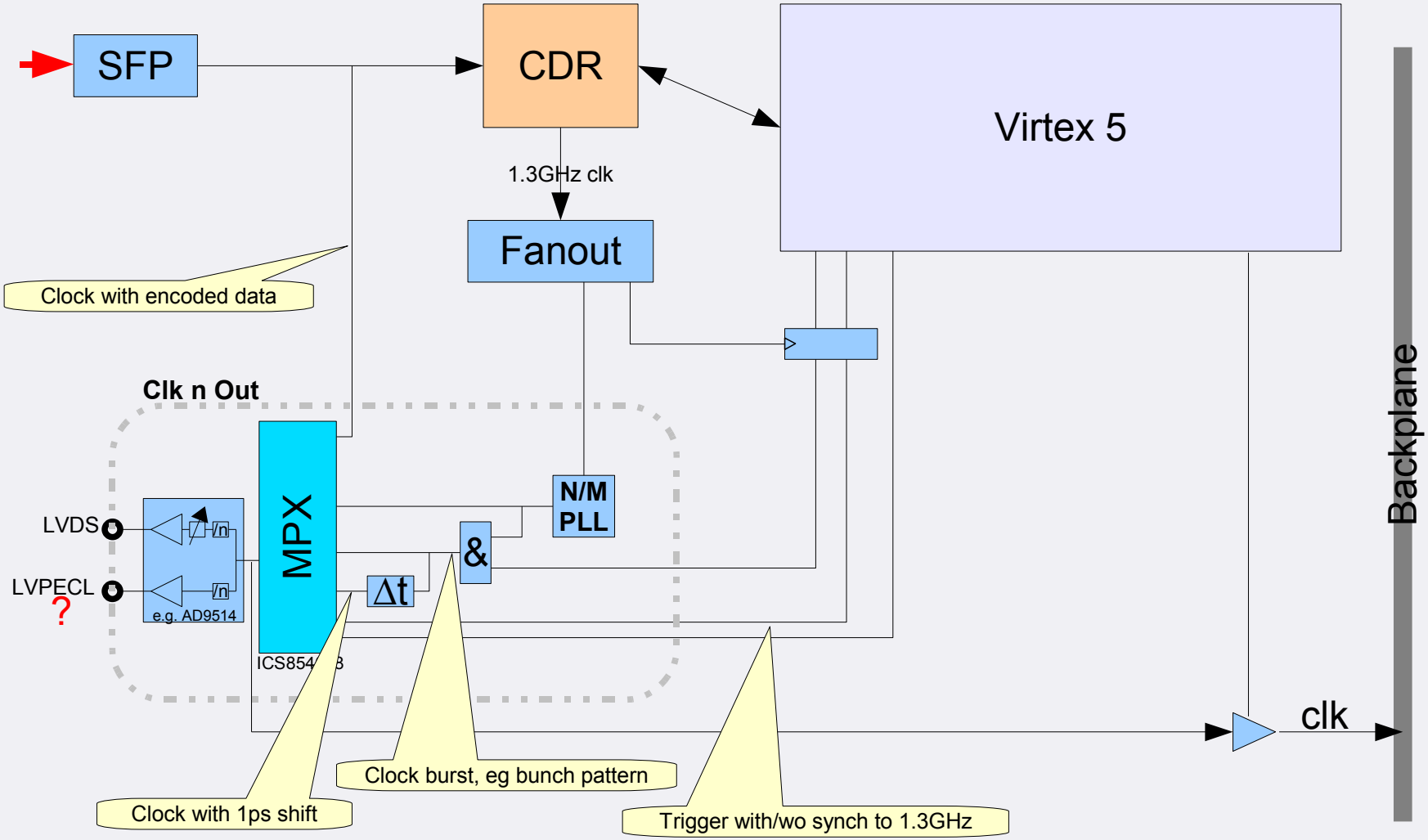
Timing Distribution



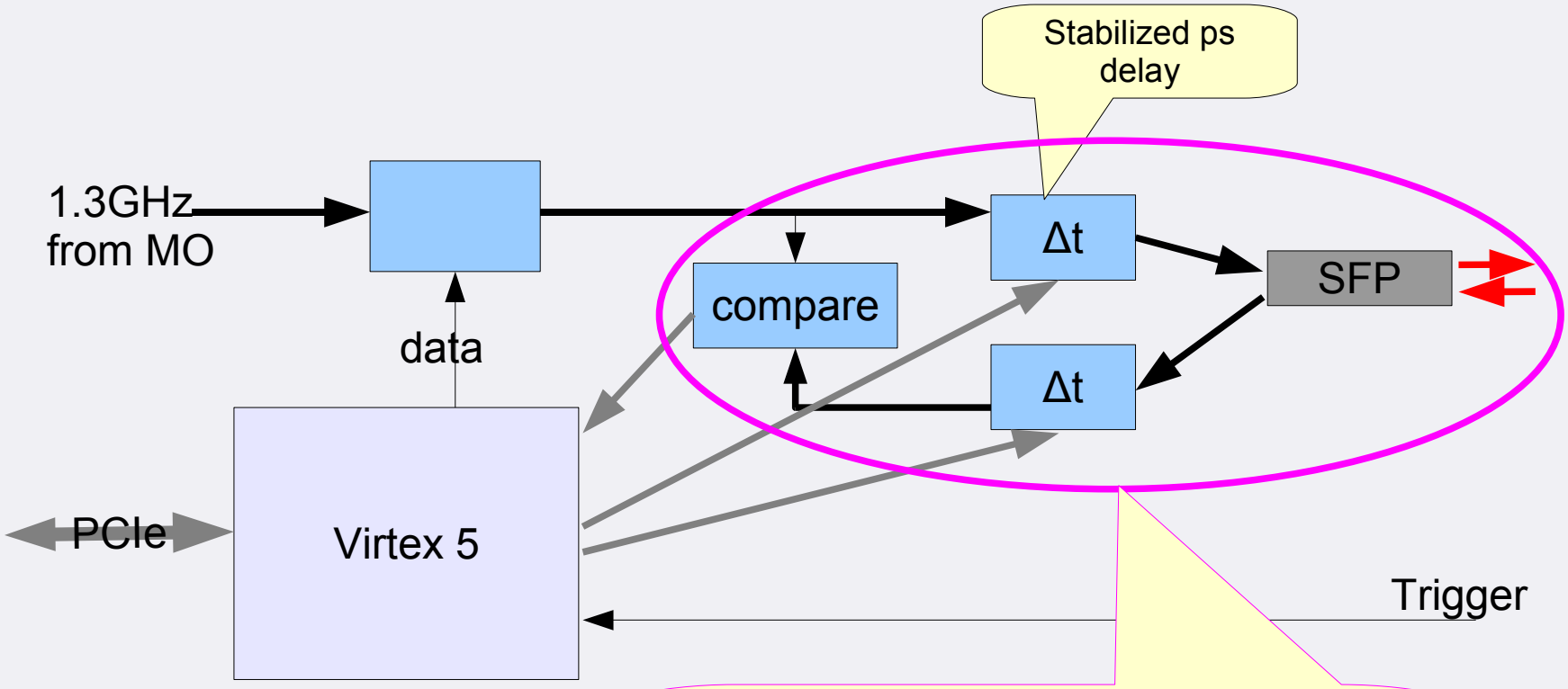
Possible AMC – Timing Receiver Module



Preliminary: output block



Preliminary: sender block

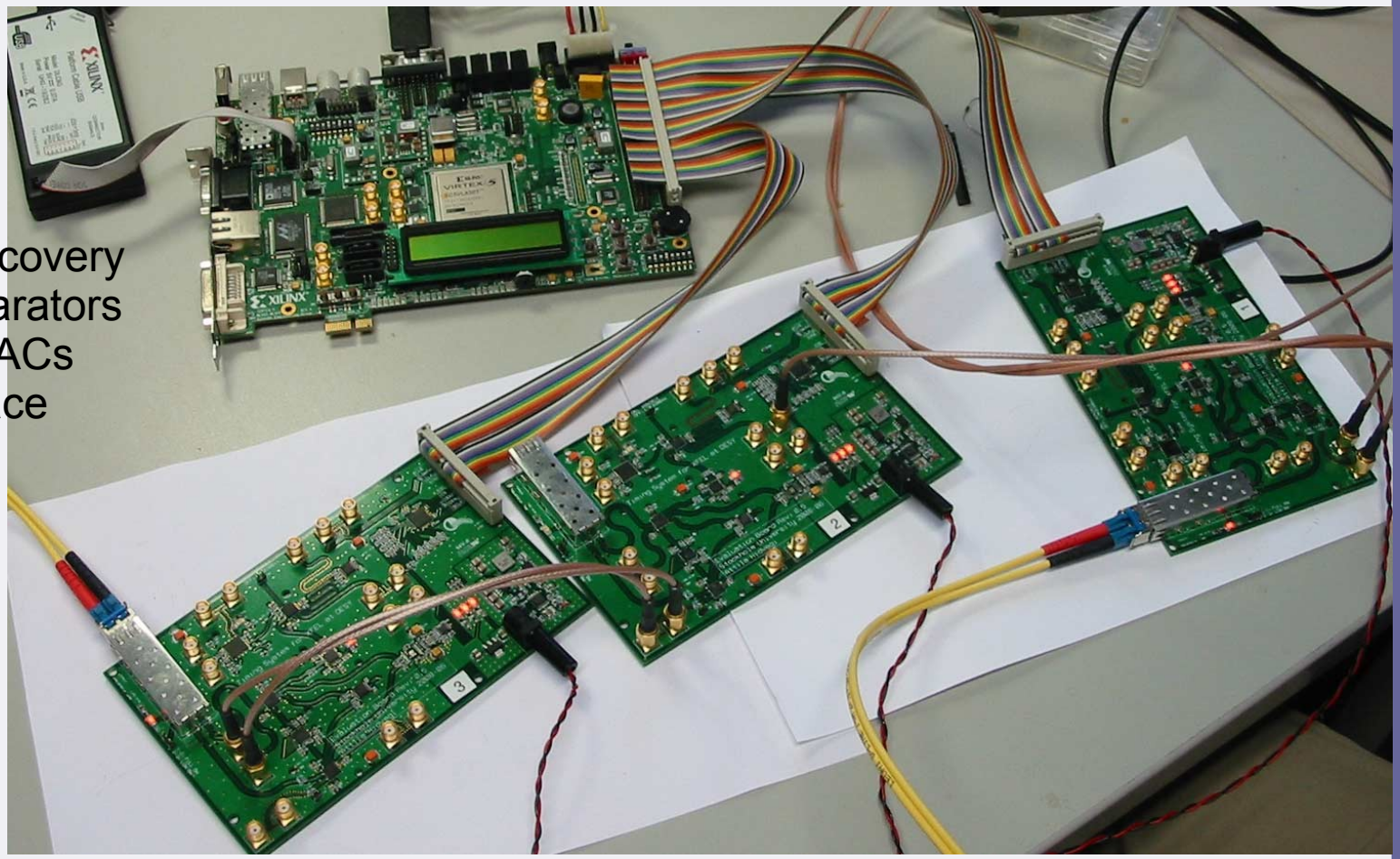


Evaluation board ready, tests started this week
Should demonstrate the achievable performance of the clock chips and FPGA

3 Test Boards connected to a Virtex 5

Contains:

fiber optic IO
delay chips
clock data recovery
phase comparators
ADCs and DACs
FPGA interface



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