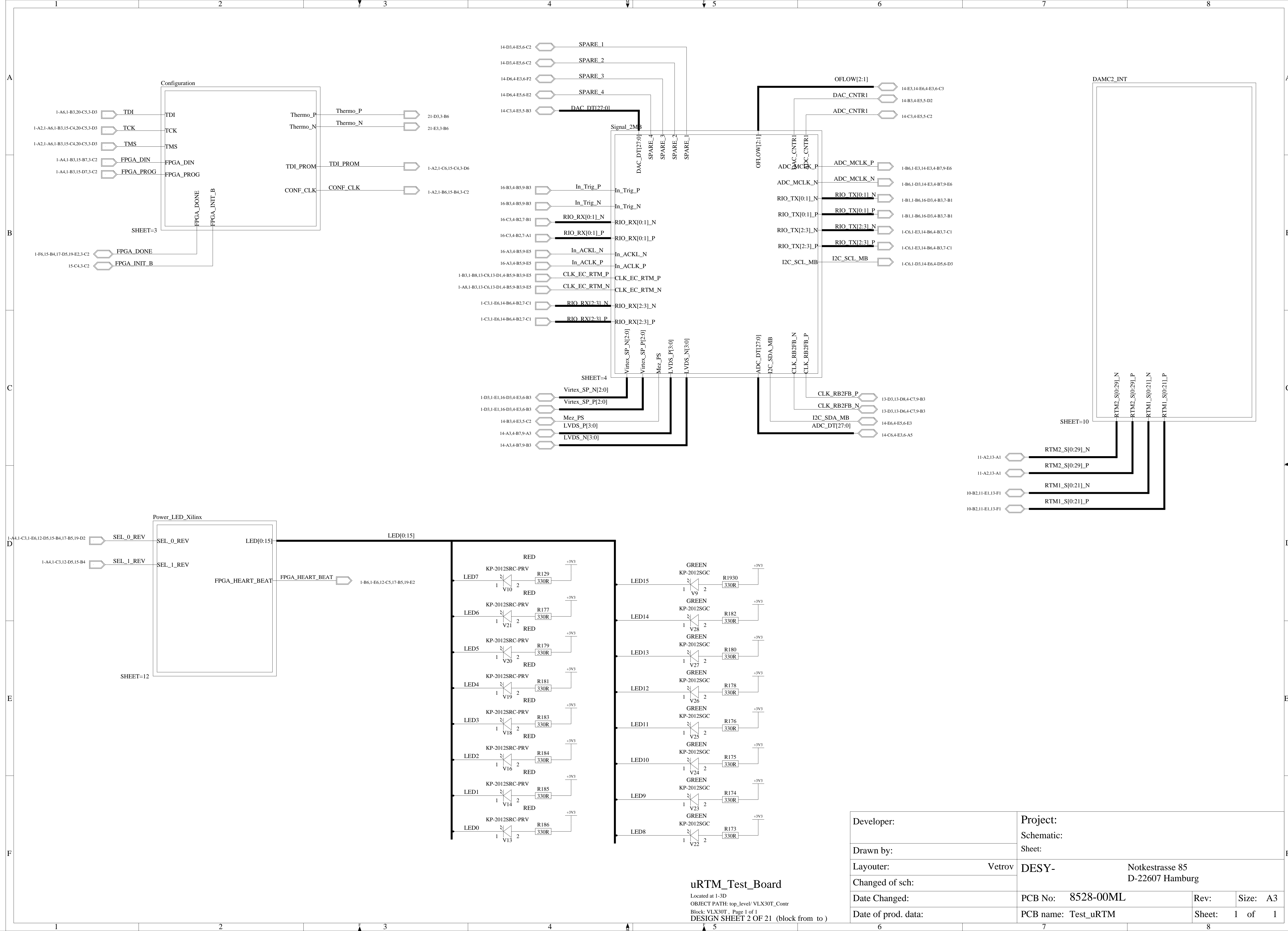


For copy schematics from other project one should open in File —>
Open —> Block —> Browse

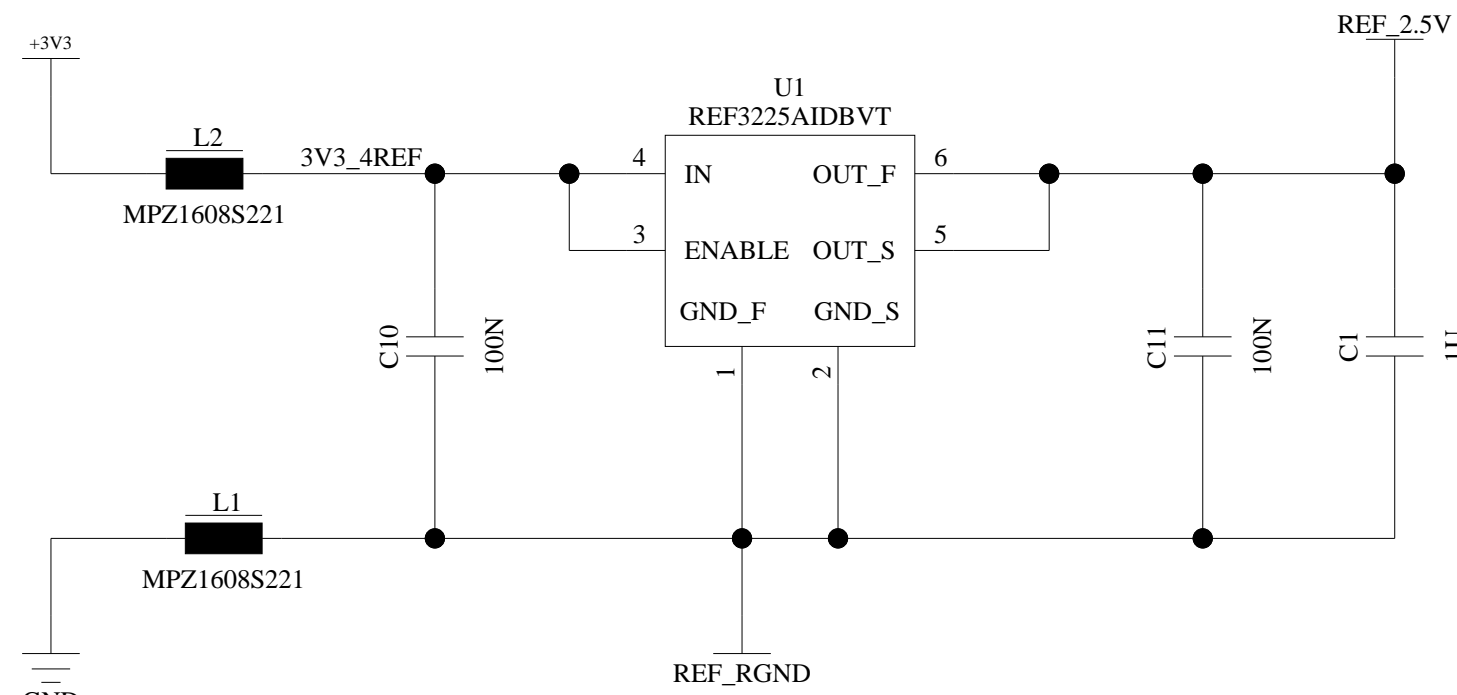
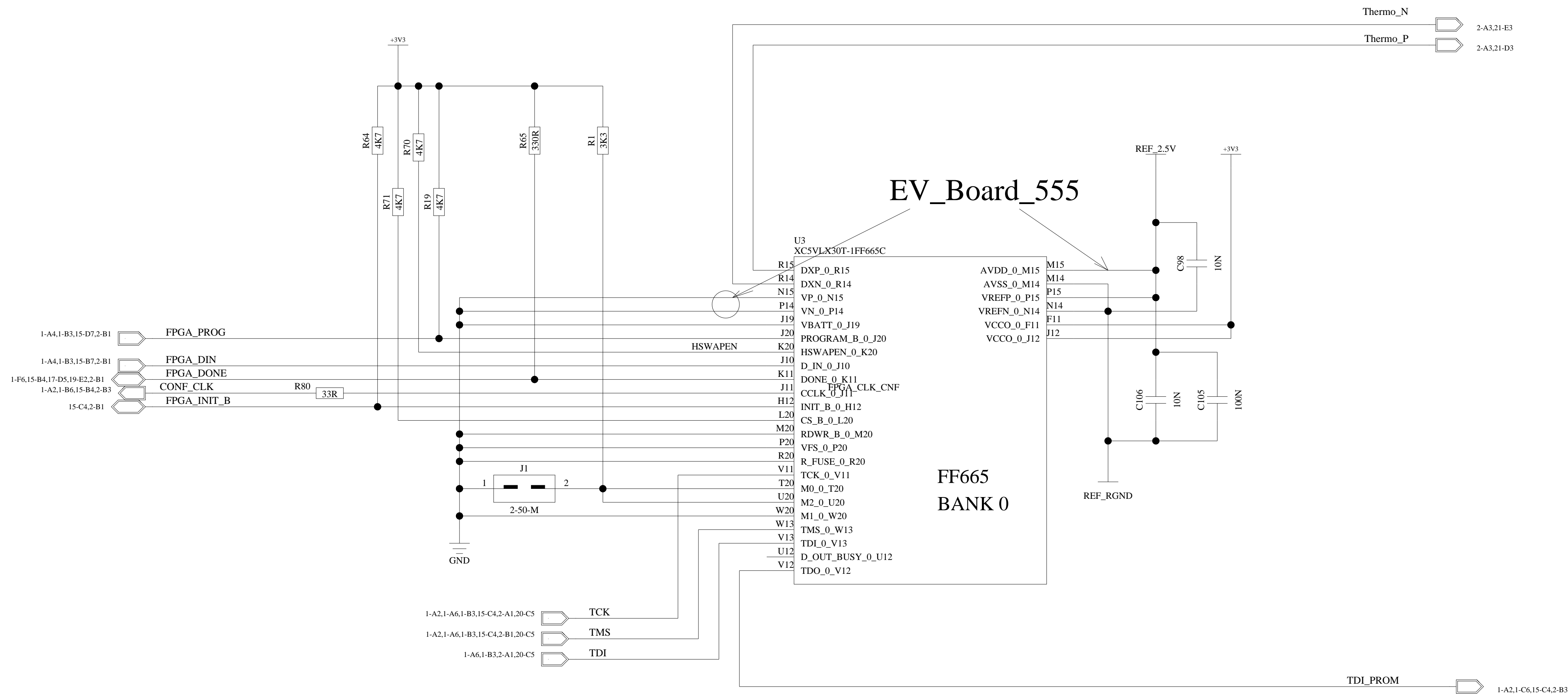
uRTM_Test_Board

Located at TOP-TopTop
OBJECT PATH: top_level/
Block: Schematic1 , Page 1 of 1
DESIGN SHEET 1 OF 21 (block from to)

Developer:	Project:			
	Schematic:			
Drawn by:	Sheet:			
Layouter:	Vetrov	DESY-Notkestrasse 85		
Changed of sch:		D-22607 Hamburg		
Date Changed:	PCB No:	8528-00ML	Rev:	Size: A3
Date of prod. data:	PCB name:	Test_uRTM	Sheet:	1 of 1



Configuration Bank and System Monitor

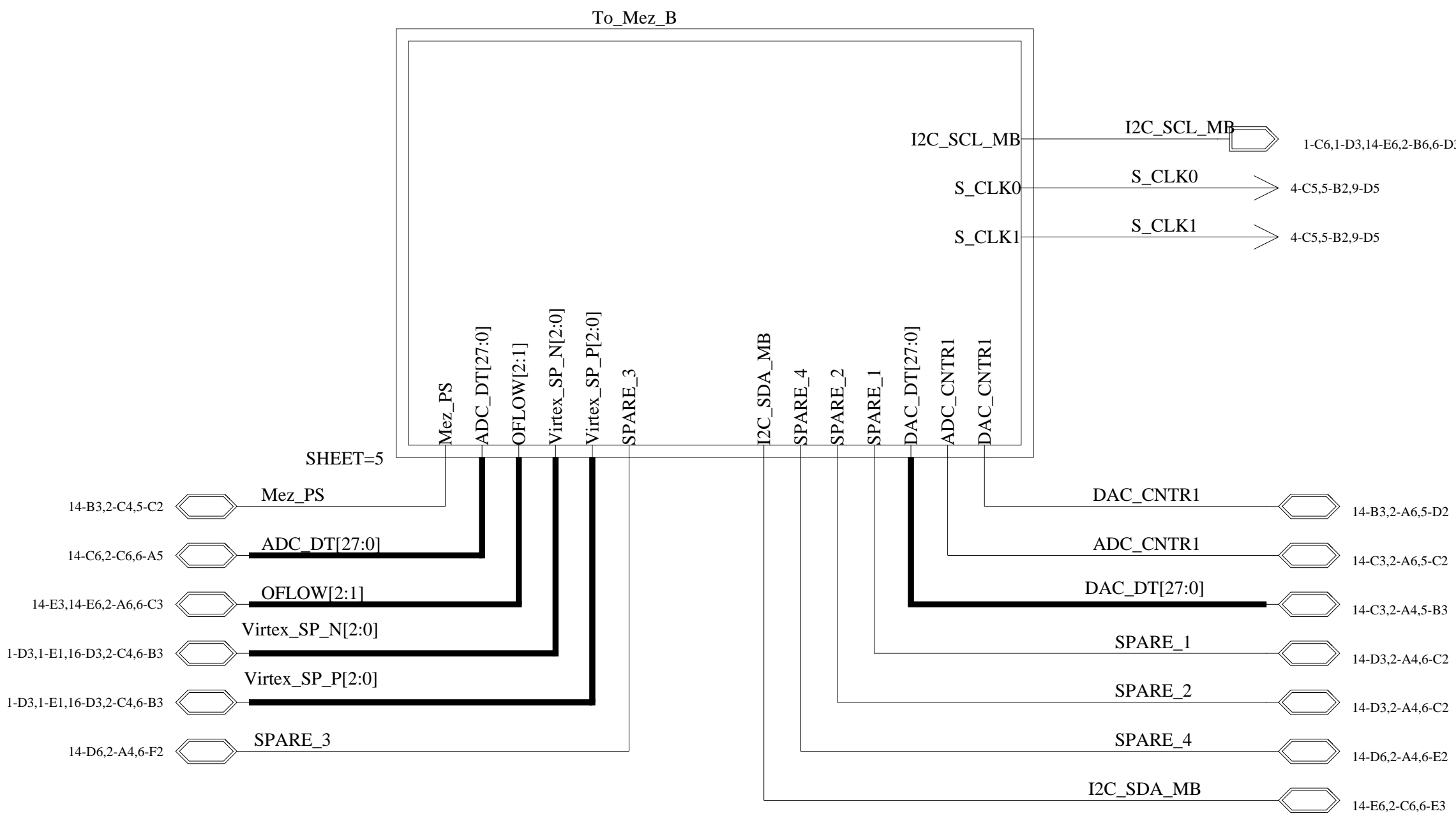
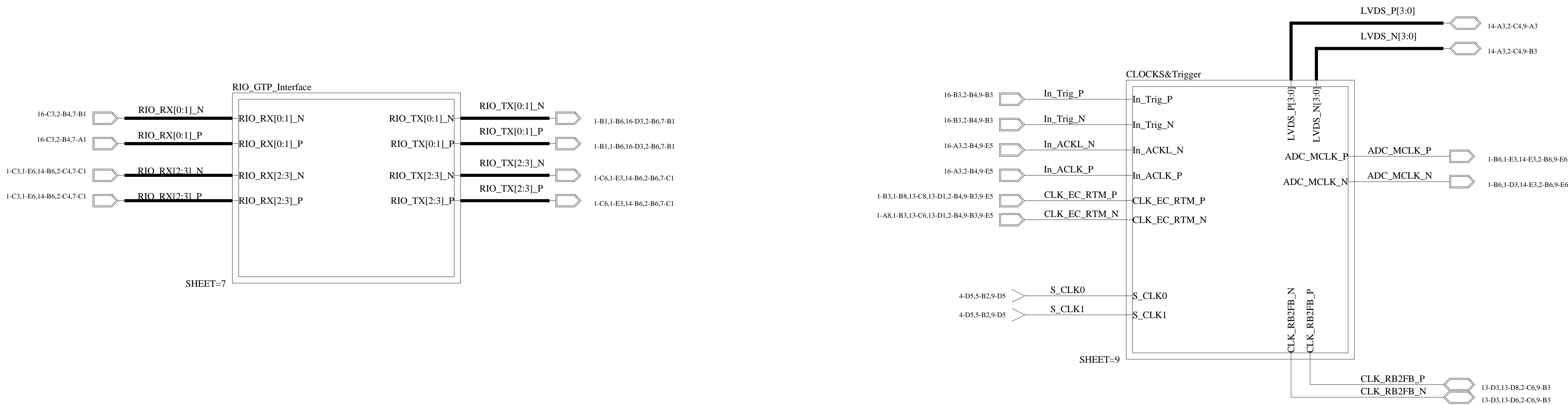


uRTM_Test_Board

Located at 1-2B
OBJECT PATH: top_level/ VLX30T_Contr/Configuration
Block: JTAG_ispPROM , Page 1 of 1
DESIGN SHEET 3 OF 21 (block from to)

Developer:		Project:			
		Schematic:			
Drawn by:		Sheet:			
Layouter:	Vetrov	DESY-Notkestrasse 85			
Changed of sch:		D-22607 Hamburg			
Date Changed:		PCB No: 8528-00ML		Rev:	Size: A3
Date of prod. data:		PCB name: Test_uRTM		Sheet: 1	of 1

Interface to 2ADC/2DAC Mezzanine Board and GTP Interfaces

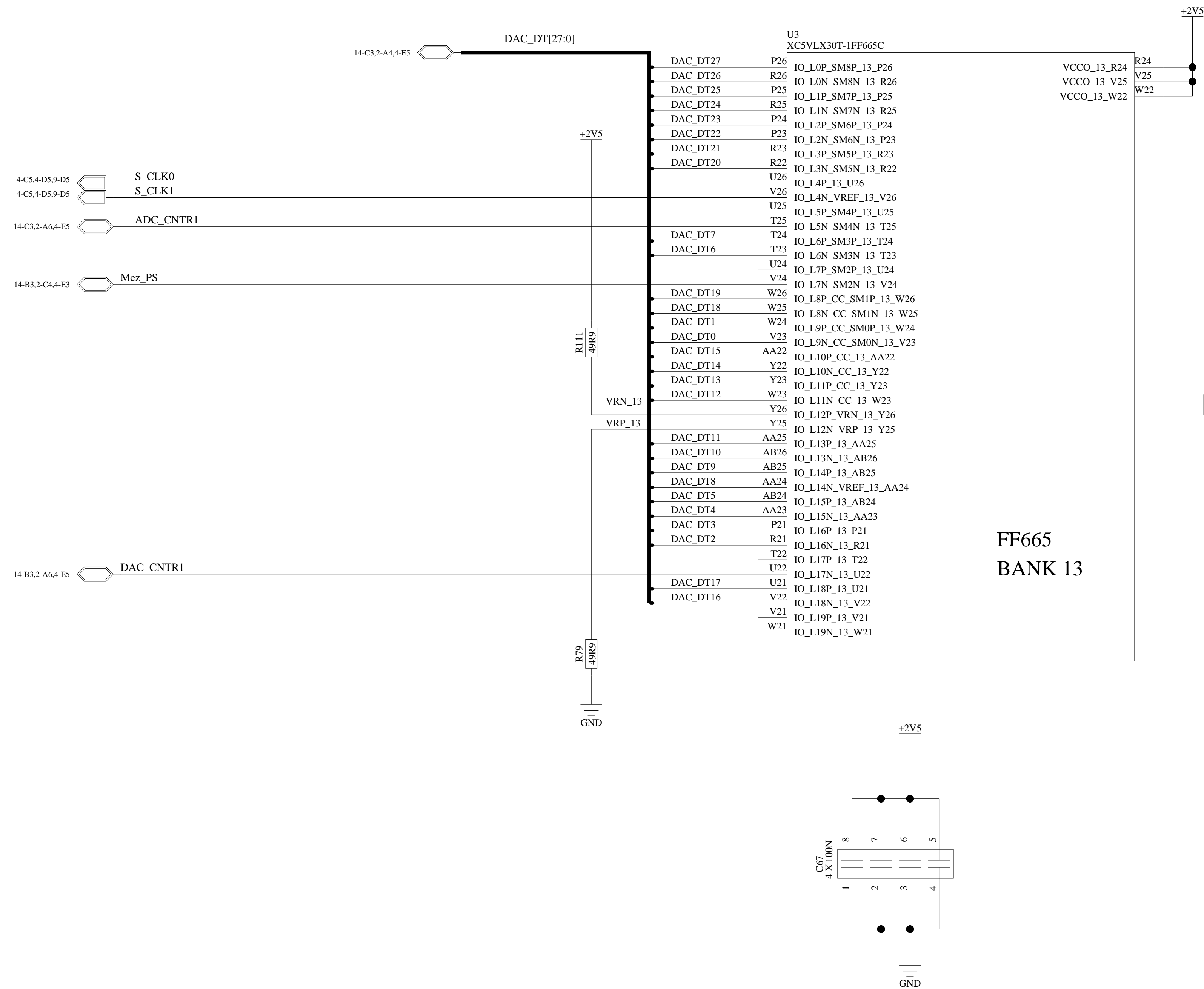


uRTM_Test_Board

Located at 1-4C
OBJECT PATH: top_level/ VLX30T_Contr/Signal_2MB
Block: Mez_INT , Page 1 of 1
DESIGN SHEET 4 OF 21 (block from to)

Developer:	Project:			
	Schematic:			
Drawn by:	Sheet:			
Layouter:	DESY-			
Changed of sch:	Notkestrasse 85			
Date Changed:	D-22607 Hamburg			
Date of prod. data:	PCB No: 8528-00ML	Rev:	Size: A3	
	PCB name: Test_uRTM	Sheet: 1 of 1		

Differential or single ended Interface to Mezzanine Board – 1



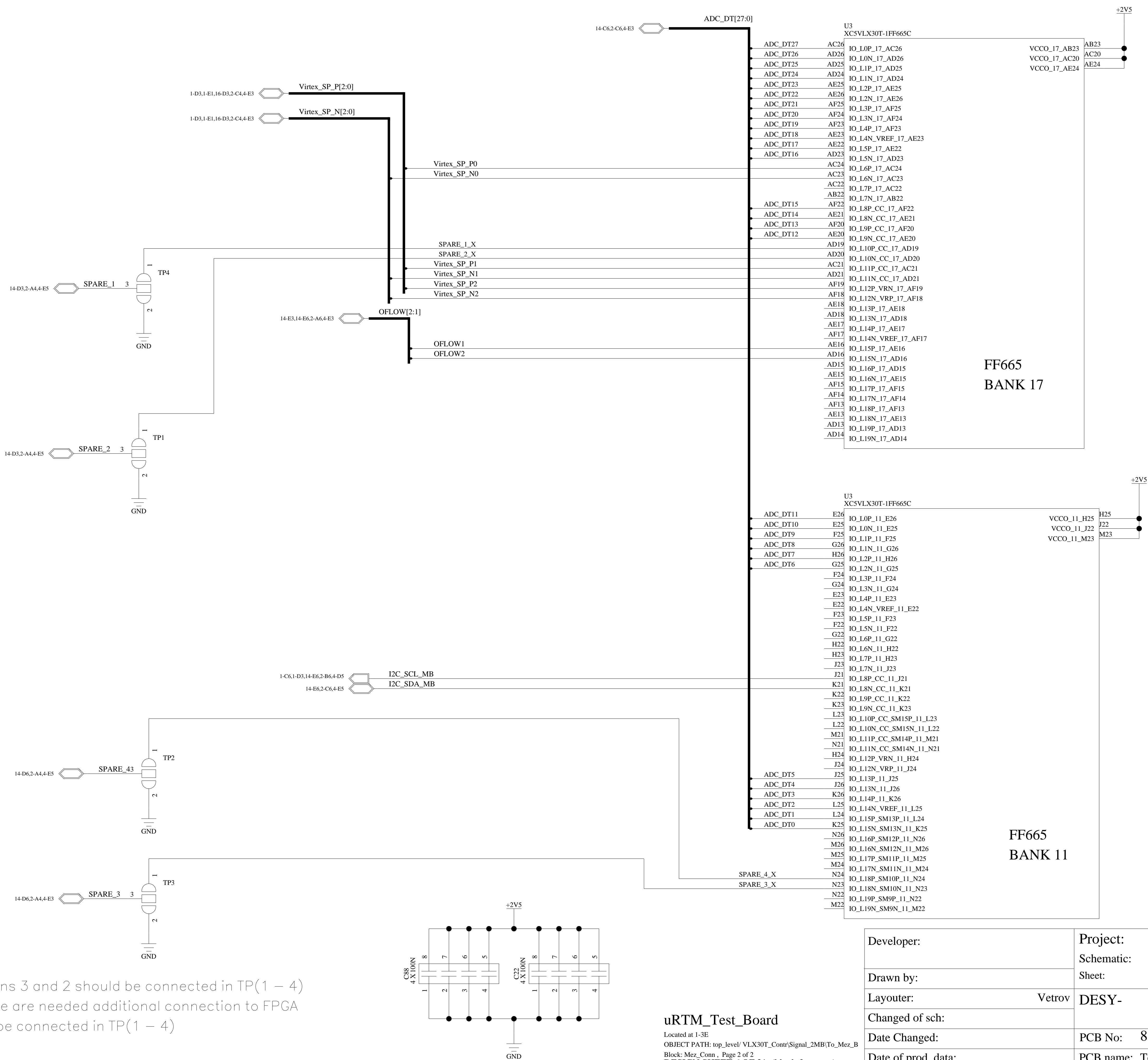
I/O buffer in this bank should be LVDCI_25 or LVDS_25

uRTM_Test_Board

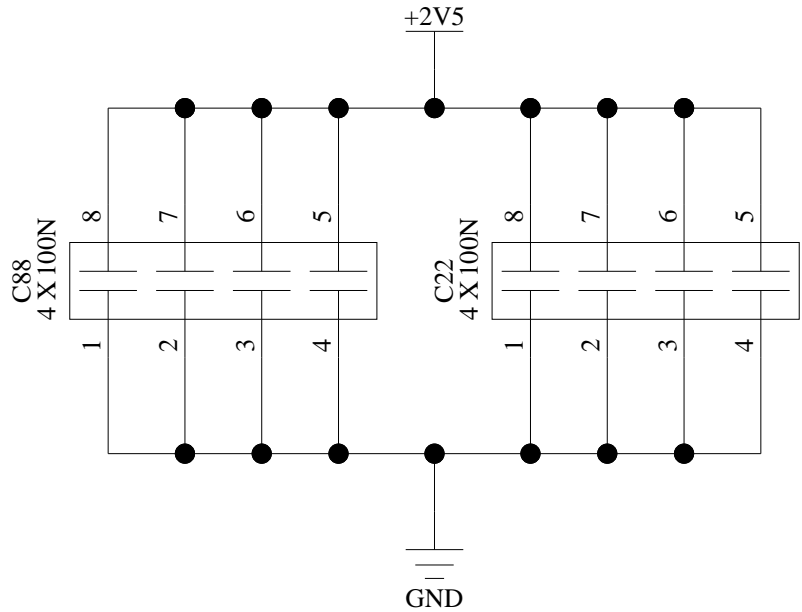
Located at 1-3E
OBJECT PATH: top_level/VLX30T_Contr/Signal_2MB/To_Mez_B
Block: Mez_Conn , Page 1 of 2
DESIGN SHEET 5 OF 21 (block from to)

Developer:	Project:			
Drawn by:	Schematic:			
Layouter:	Vetrov	DESY- Notkestrasse 85		
Changed of sch:		D-22607 Hamburg		
Date Changed:	PCB No:	8528-00ML	Rev:	Size: A3
Date of prod. data:	PCB name:	Test_uRTM	Sheet:	1 of 1

Differential or single ended Interface to Mezzanine Board – II



1. For 2xDAC, 2xADC pins 3 and 2 should be connected in TP(1 – 4)
2. For application where are needed additional connection to FPGA pins 3 and 1 should be connected in TP(1 – 4)

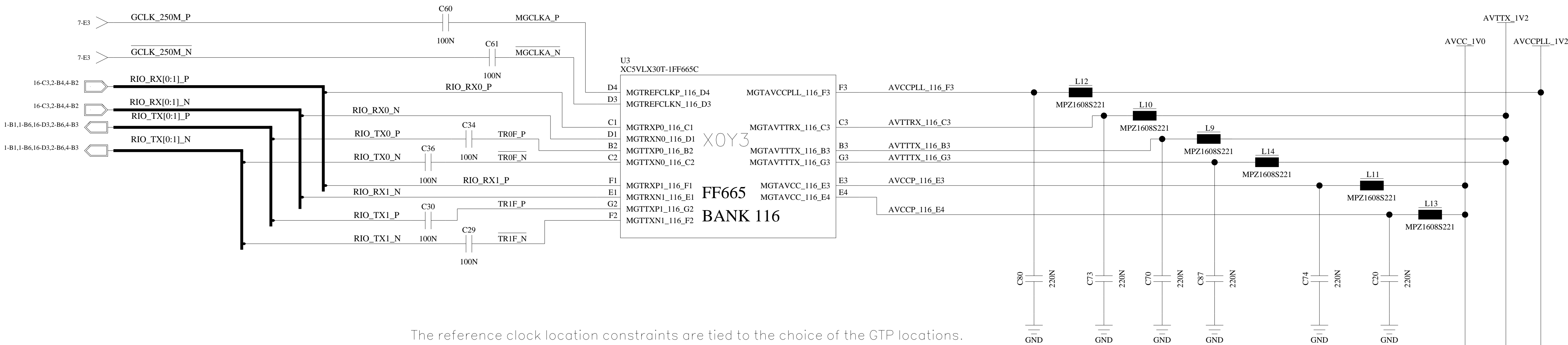


uRTM_Test_Board

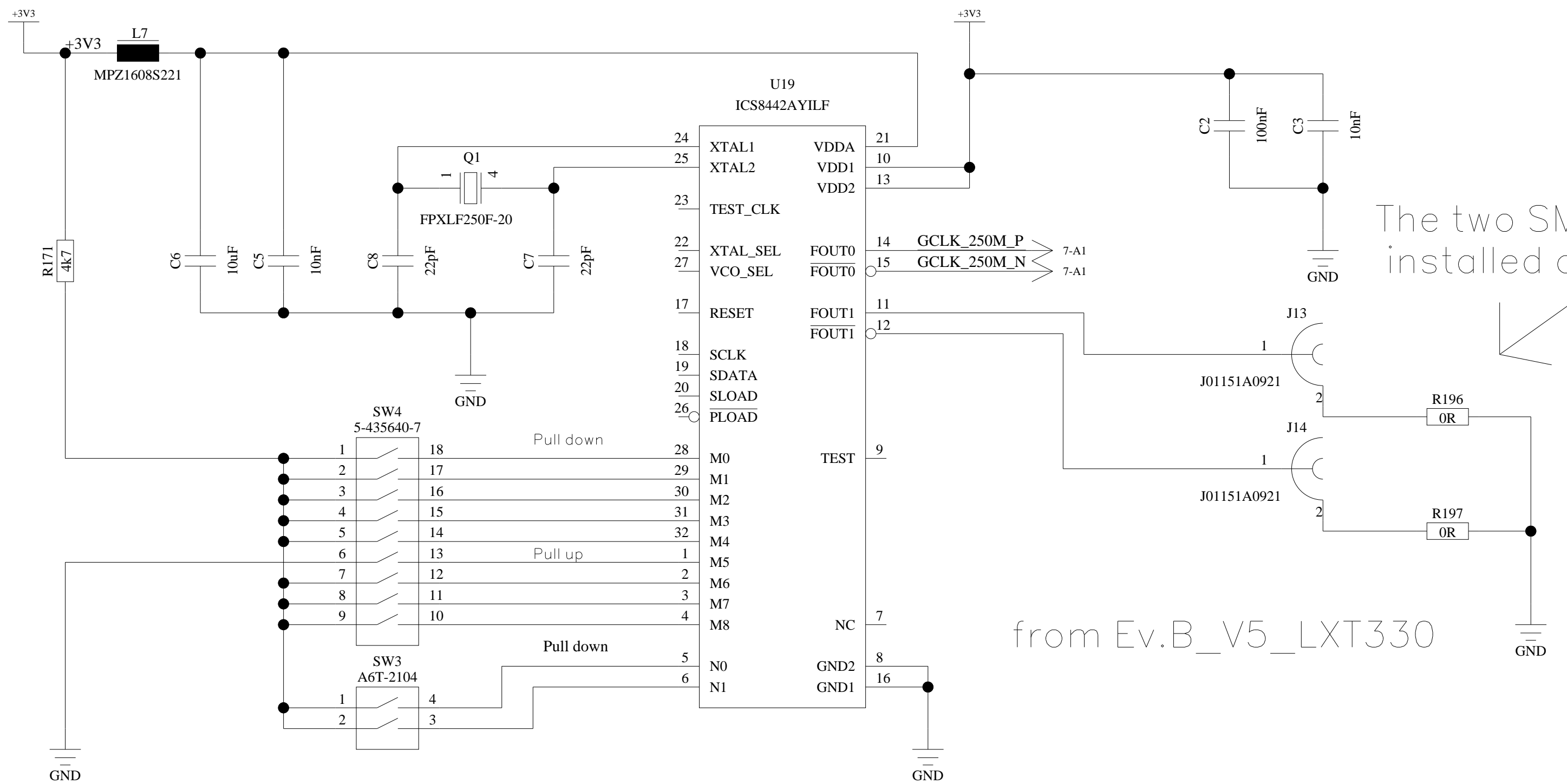
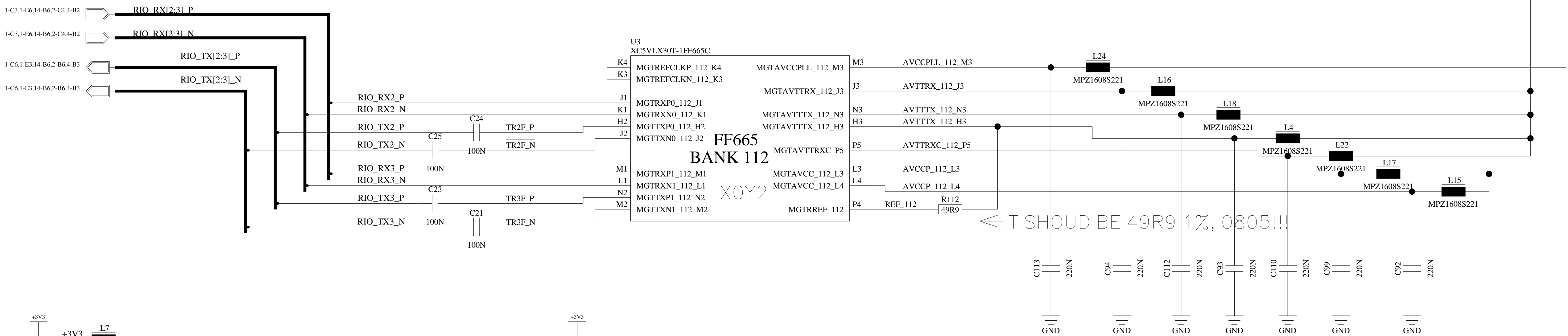
Located at 1-3E
OBJECT PATH: top_level/ VLX30T_Contr/Signal_2MB/To_Mez_B
Block: Mez_Conn , Page 2 of 2
DESIGN SHEET 6 OF 21 (block from to)

Developer:	Project:			
	Schematic:			
Drawn by:	Sheet:			
Layouter:	DESY-			
Changed of sch:	Notkestrasse 85 D-22607 Hamburg			
Date Changed:	PCB No:	8528-00ML	Rev:	Size: A3
Date of prod. data:	PCB name:	Test_uRTM	Sheet:	2 of 2

GTP_Interfaces



The reference clock location constraints are tied to the choice of the GTP locations. Reference clock needs to arrive at one of the GTP tiles chosen in the design and routed to the other GTP tiles. The reference clock arriving at one GTP tile can be routed to any other GTP tile that is up to three GTP tiles away in either the north or south direction. The GTP tile used for Lane 0 is chosen to receive the reference clock.



The two SMA right angle connectors installed on front pane

from Ev.B_V5_LXT330

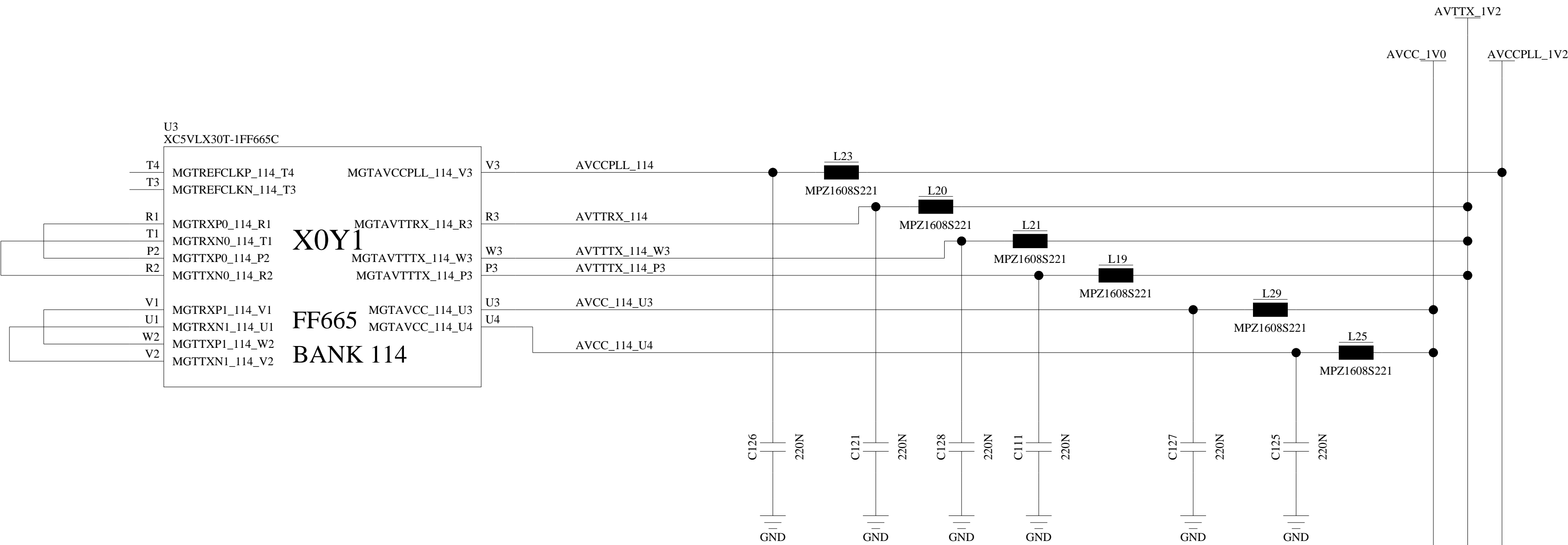
uRTM_Test_Board

Located at 1-2C
OBJECT PATH: top_level/ VLX30T_Contr/Signal_2MB/RIO_GTP_Interface
Block: GTP_Interface , Page 1 of 2
DESIGN SHEET 7 OF 21 (block from to)

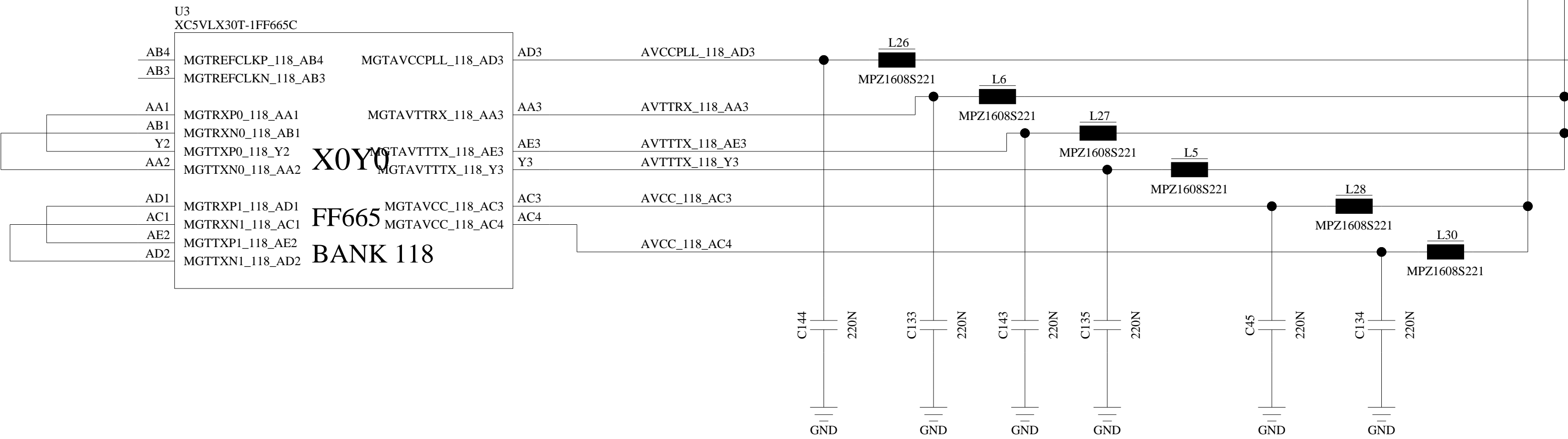
Interconnect Technology	FOUT0 and FOUT1 (MHz)	ICS8442 M and N Settings										
		M8	M7	M6	M5	M4	M3	M2	M1	M0	N1	N0
Gigabit Ethernet	125	0	0	0	0	0	1	0	1	0	0	1
Fiber Channel	106.25	0	0	0	0	1	0	0	0	1	1	0
	212.5	0	0	0	0	1	0	0	0	1	0	1
Infiniband	250	0	0	0	0	0	1	0	1	0	0	0
XAUI	312.5	0	0	0	0	1	1	0	0	1	0	1

Developer:	Project:		
Drawn by:	Schematic:		
Layer:	Sheet:		
Changed of sch:	DESY-		
Date Changed:	Notkestrasse 85		
Date of prod. data:	D-22607 Hamburg		
PCB No:	8528-00ML	Rev:	Size: A3
PCB name:	Test_uRTM	Sheet:	1 of 1

Unused GTP



The total number of GTP_DUAL tiles sourced by the external clock pin pair(MGTREFCLKN/MGTREFCLKP) must not exceed seven.



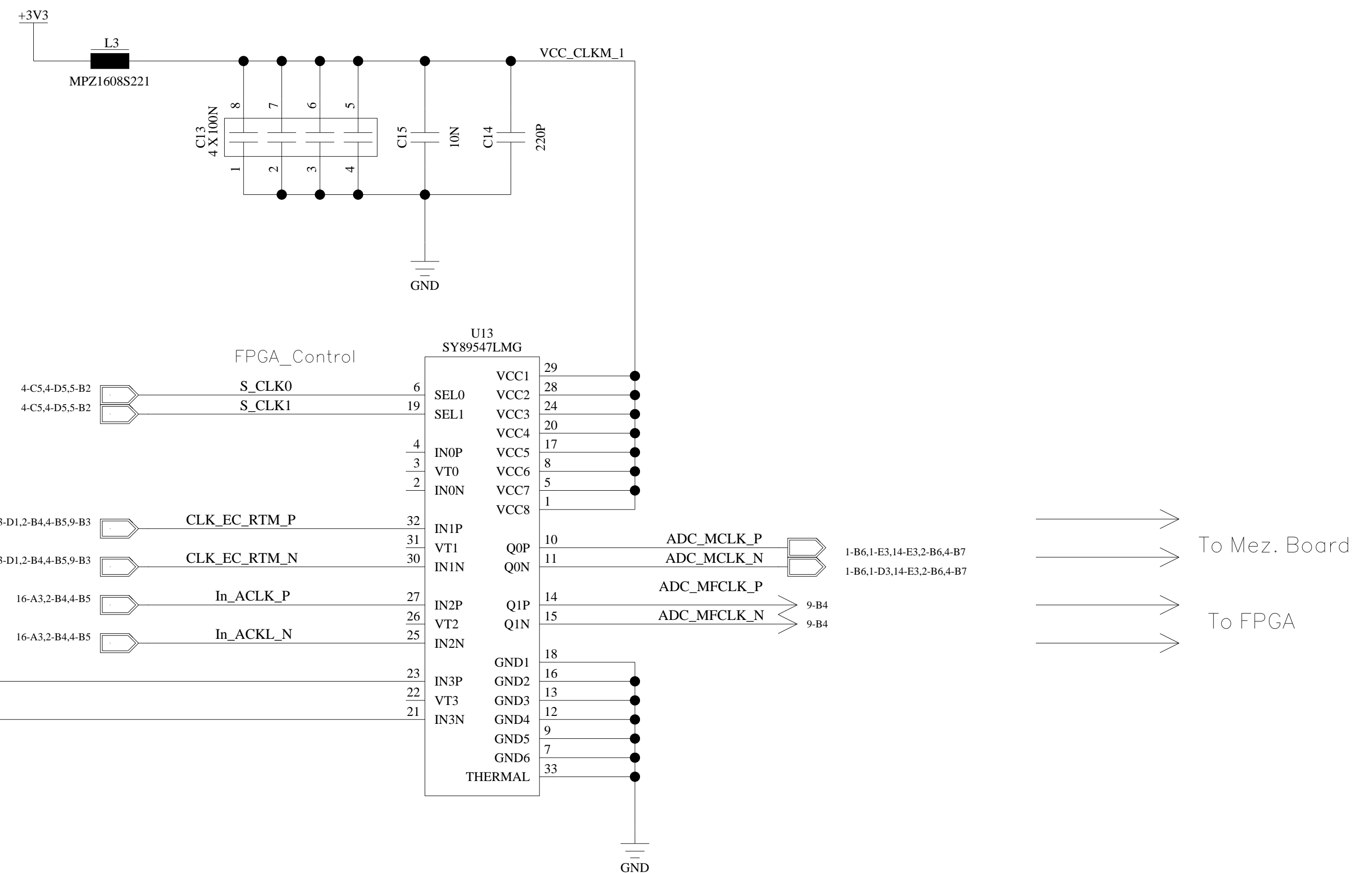
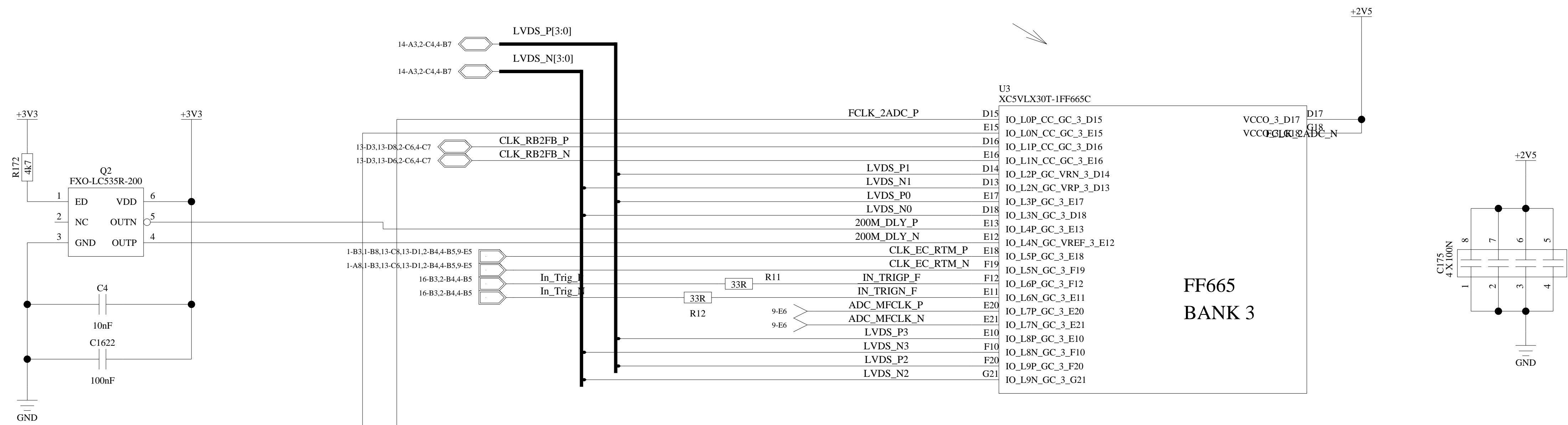
uRTM_Test_Board

Located at 1-2C
OBJECT PATH: top_level/ VLX30T_Contr/Signal_2MB/RIO_GTP_Interface
Block: GTP_Interface , Page 2 of 2
DESIGN SHEET 8 OF 21 (block from to)

Developer:	Project:			
	Schematic:			
Drawn by:	Sheet:			
Layouter:	DESY-Notkestrasse 85 D-22607 Hamburg			
Changed of sch:				
Date Changed:	PCB No: 8528-00ML	Rev:	Size:	A3
Date of prod. data:	PCB name: Test_uRTM	Sheet:	2 of	2

Clocks, LVDS and Trigger

DIFF_TERM + TRUE!!! → receivers will have internal 100 Ohm termination



True Table

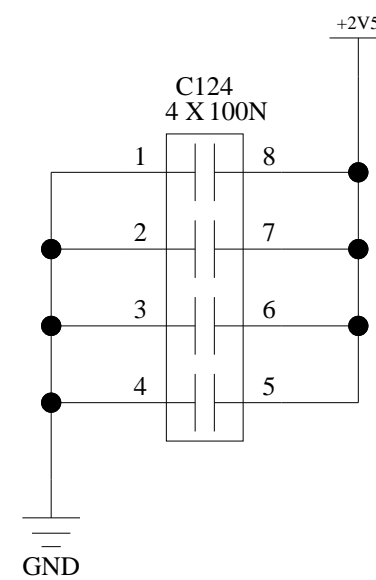
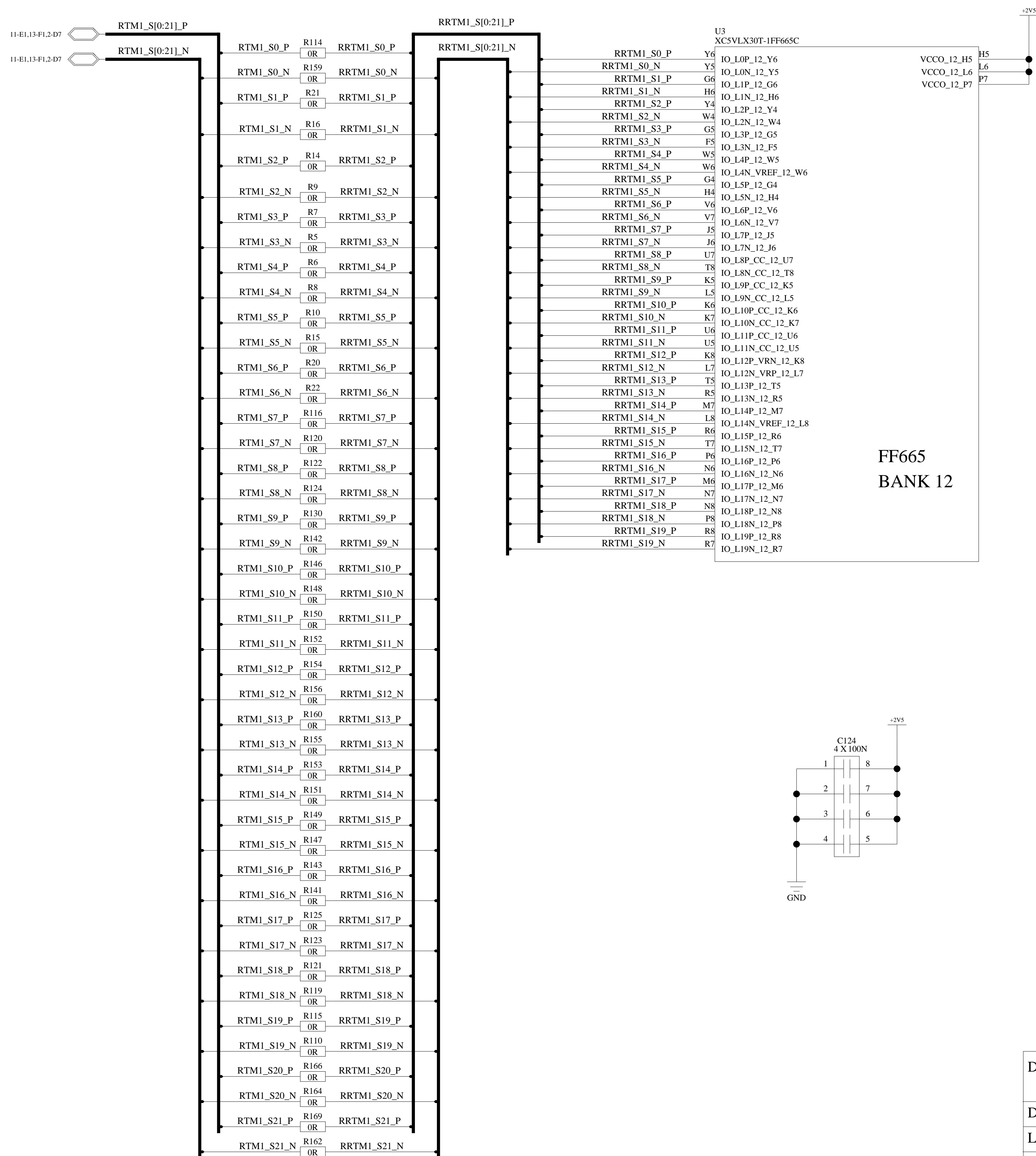
INO	IN1	IN2	IN3	SEL0	SEL1	Q	Q#
0	X	X	X	0	0	0	1
1	X	X	X	0	0	1	0
X	0	X	X	1	0	0	1
X	1	X	X	1	0	1	0
X	X	0	X	0	1	0	1
X	X	1	X	0	1	1	0
X	X	X	0	1	1	0	1
X	X	X	1	1	1	1	0

uRTM_Test_Board

Located at 1-6C
 OBJECT PATH: top_level\VLX30T_Contr\Signal_2MB\CLOCKS&Trigger
 Block: LVDS_TO_MB, Page 1 of 1
DESIGN SHEET 9 OF 21 (block from to)

Developer:	Project:			
Drawn by:	Schematic:			
Layouter:	Vetrov	DESY- Notkestrasse 85		
Changed of sch:		D-22607 Hamburg		
Date Changed:	PCB No:	8528-00ML	Rev:	Size: A3
Date of prod. data:	PCB name:	Test_uRTM	Sheet:	1 of 1

uRTM Interface with Jumpers Zero Ohm Resistors_1

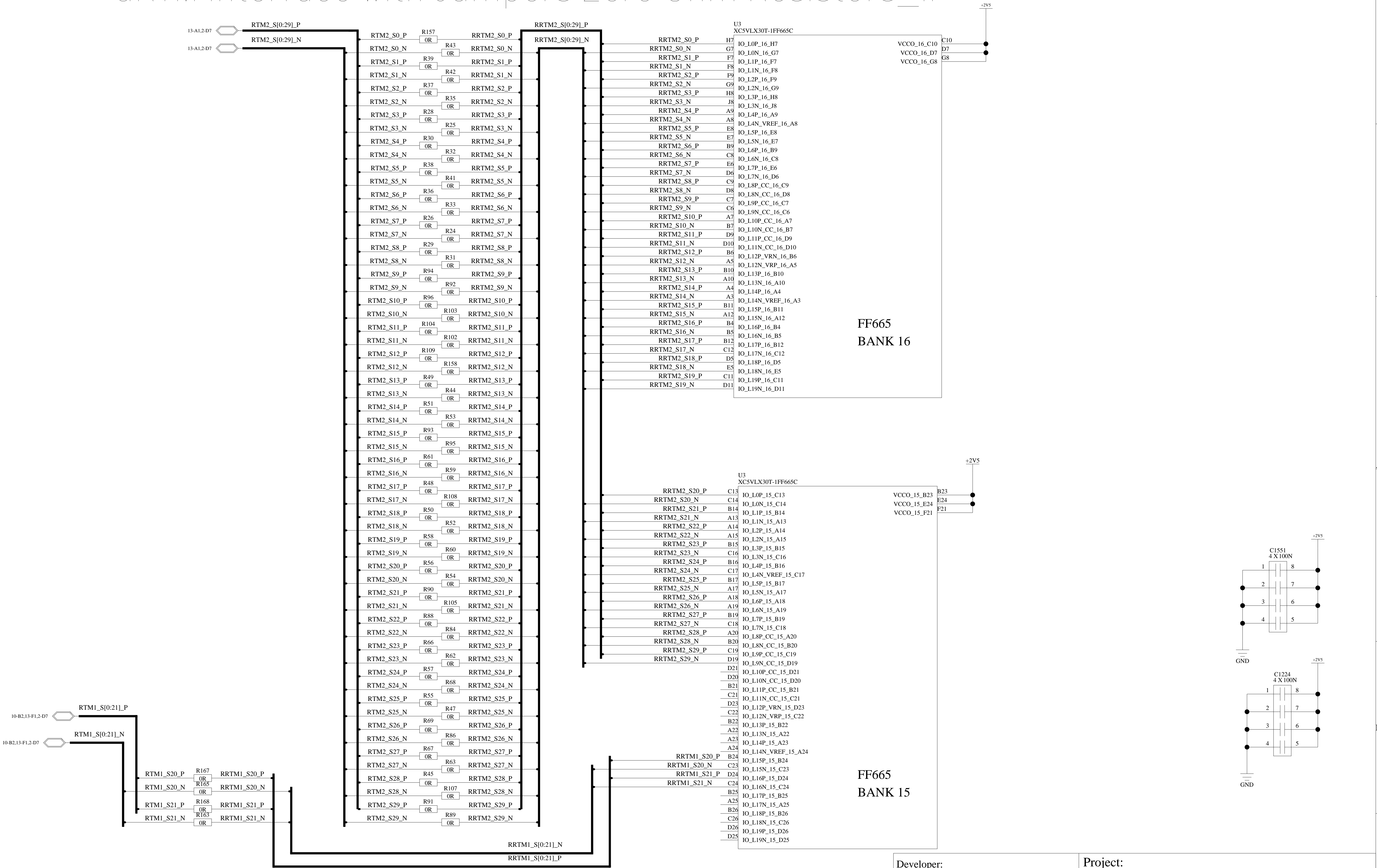


uRTM_Test_Board

Located at 1-7C
OBJECT PATH: top_level\ VLX30T_Contr\ DAMC2_INT
Block: DAMC2_INT , Page 1 of 2
DESIGN SHEET 10 OF 21 (block from to)

Developer:	Project:		
Drawn by:	Schematic:		
	Sheet:		
Layouter: Vetrov	DESY- Notkestrasse 85		
Changed of sch:	D-22607 Hamburg		
Date Changed:	PCB No: 8528-00ML	Rev:	Size: A3
Date of prod. data:	PCB name: Test_uRTM	Sheet: 1	of 1

uRTM Interface with Jumpers Zero Ohm Resistors_II

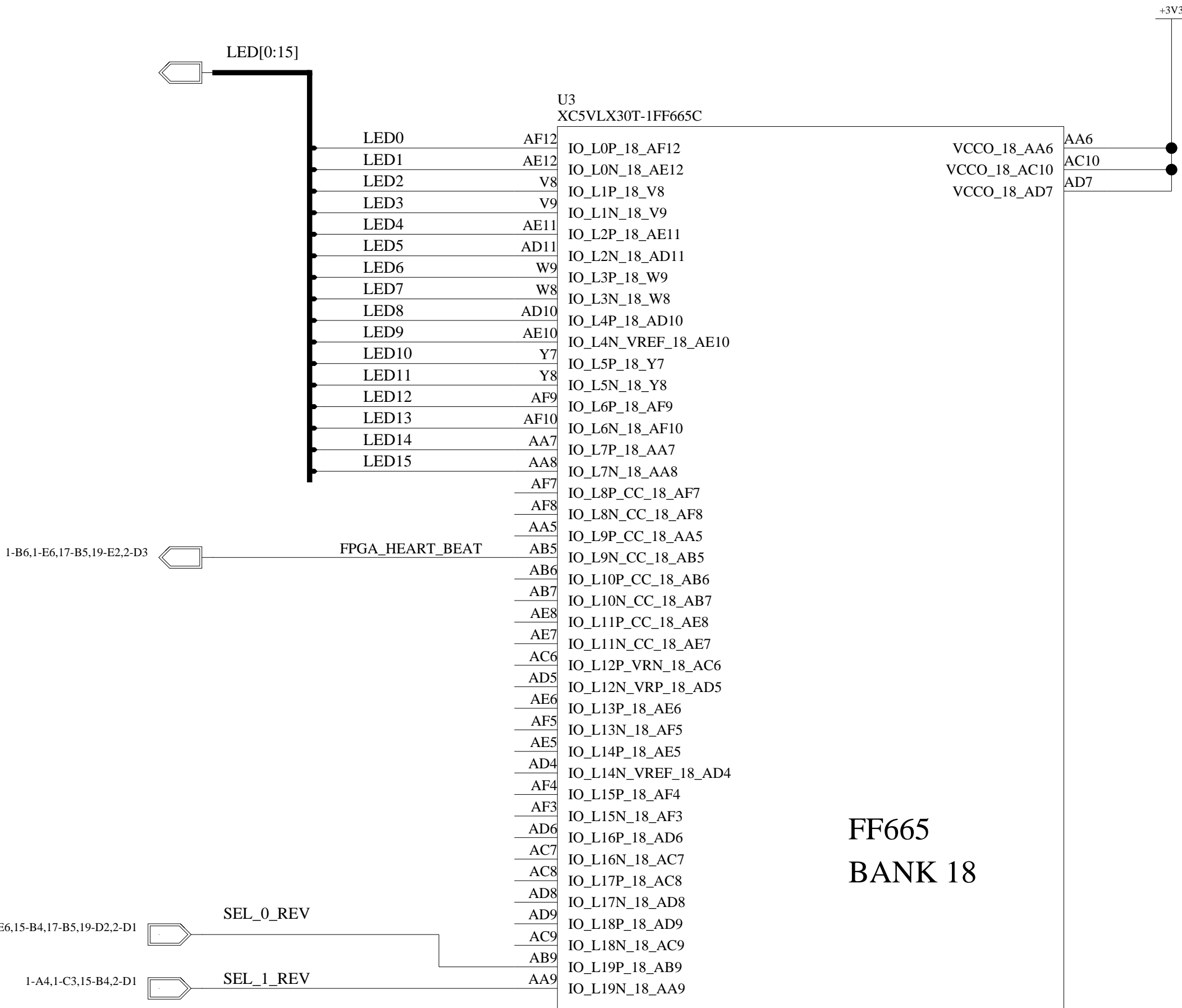
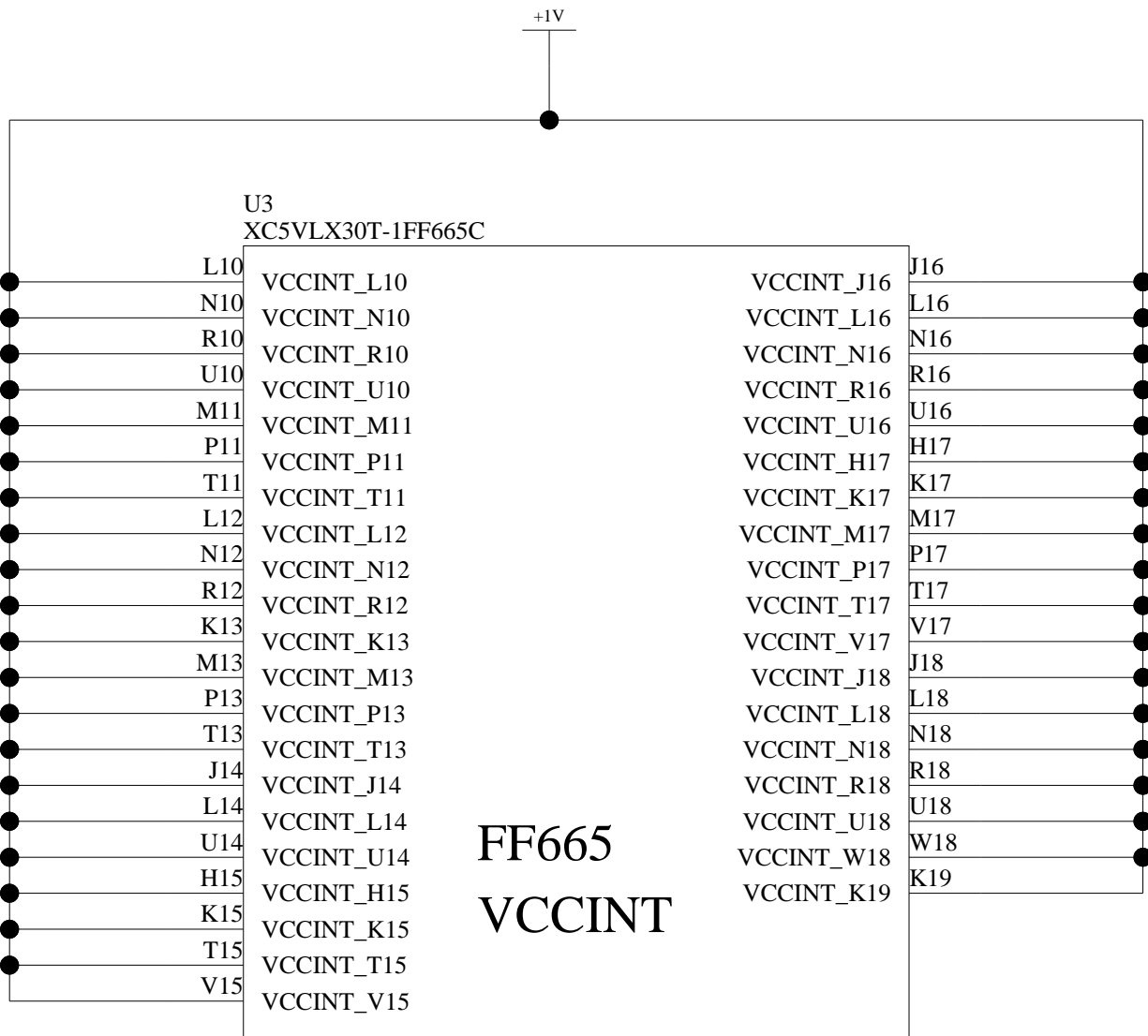
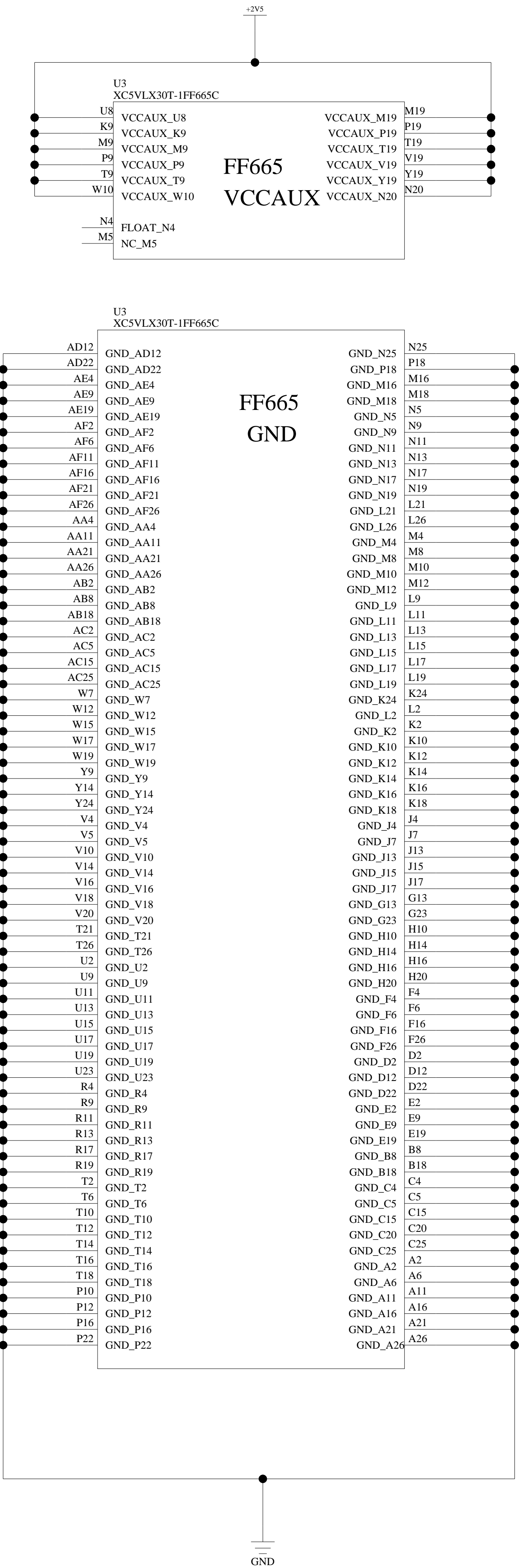


uRTM_Test_Board

Located at 1-7C
OBJECT PATH: top_level/ VLX30T_ContriDAMC2_INT
Block: DAMC2_INT , Page 2 of 2
DESIGN SHEET 11 OF 21 (block from to)

Developer:	Project: Schematic: Sheet:		
Drawn by:			
Layer:	DESY-		
Changed of sch:	Notkestrasse 85 D-22607 Hamburg		
Date Changed:	PCB No: 8528-00ML	Rev:	Size: A3
Date of prod. data:	PCB name: Test_uRTM	Sheet:	2 of 2

Xilinx Powers and LEDs control

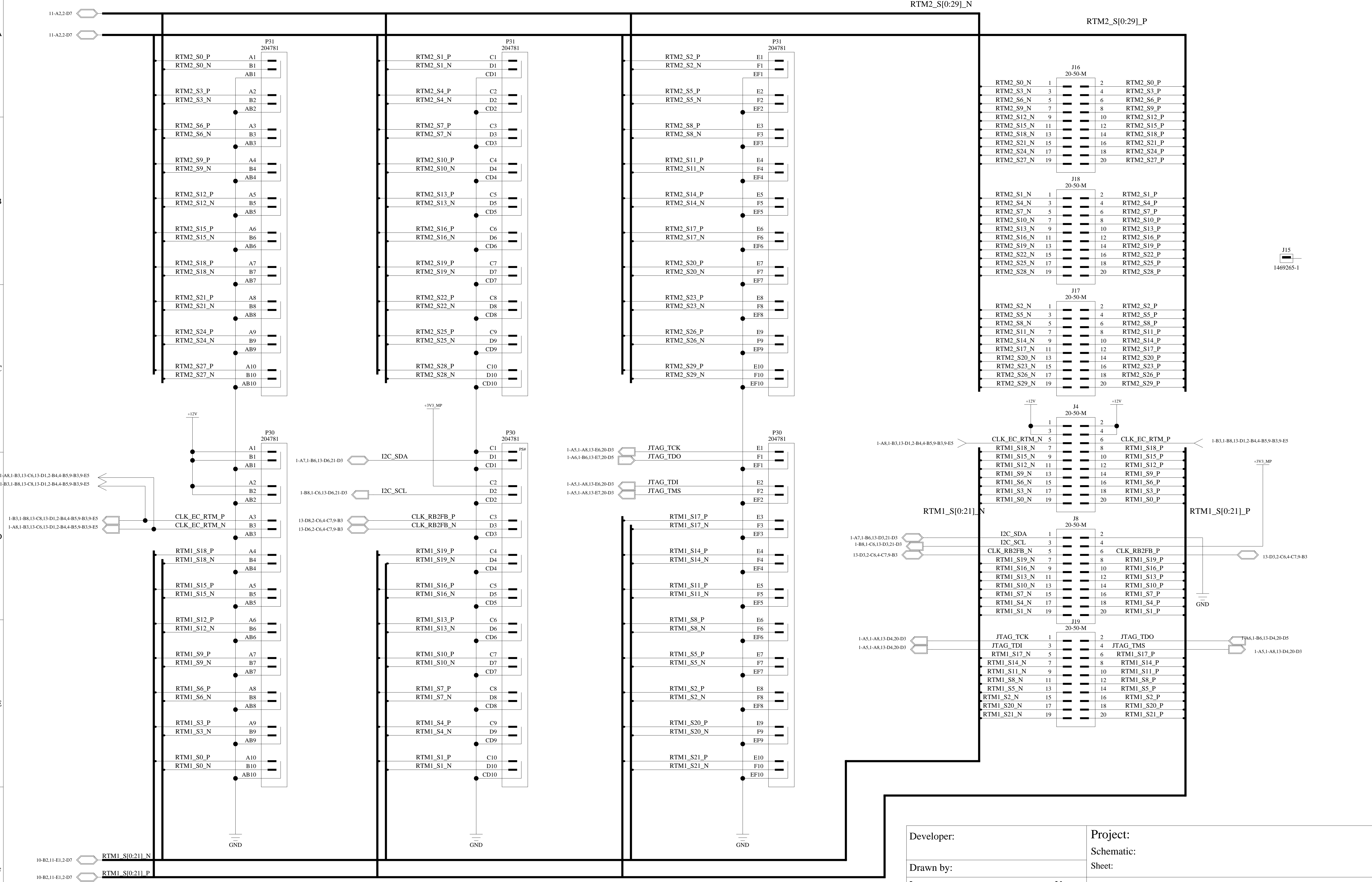


uRTM_Test_Board

Located at 1-2E
OBJECT PATH: top_level/ VLX30T_ContriPower_LED_Xilinx
Block: Power_Xilinx , Page 1 of 1
DESIGN SHEET 12 OF 21 (block from to)

Developer:	Project:			
	Schematic:			
Drawn by:	Sheet:			
Layer:	DESY-			
Changed of sch:	Notkestrasse 85 D-22607 Hamburg			
Date Changed:	PCB No: 8528-00ML	Rev:	Size:	A3
Date of prod. data:	PCB name: Test_uRTM	Sheet:	1 of	1

Block connectors P30 and P31, Test Pin–Headers and Guide

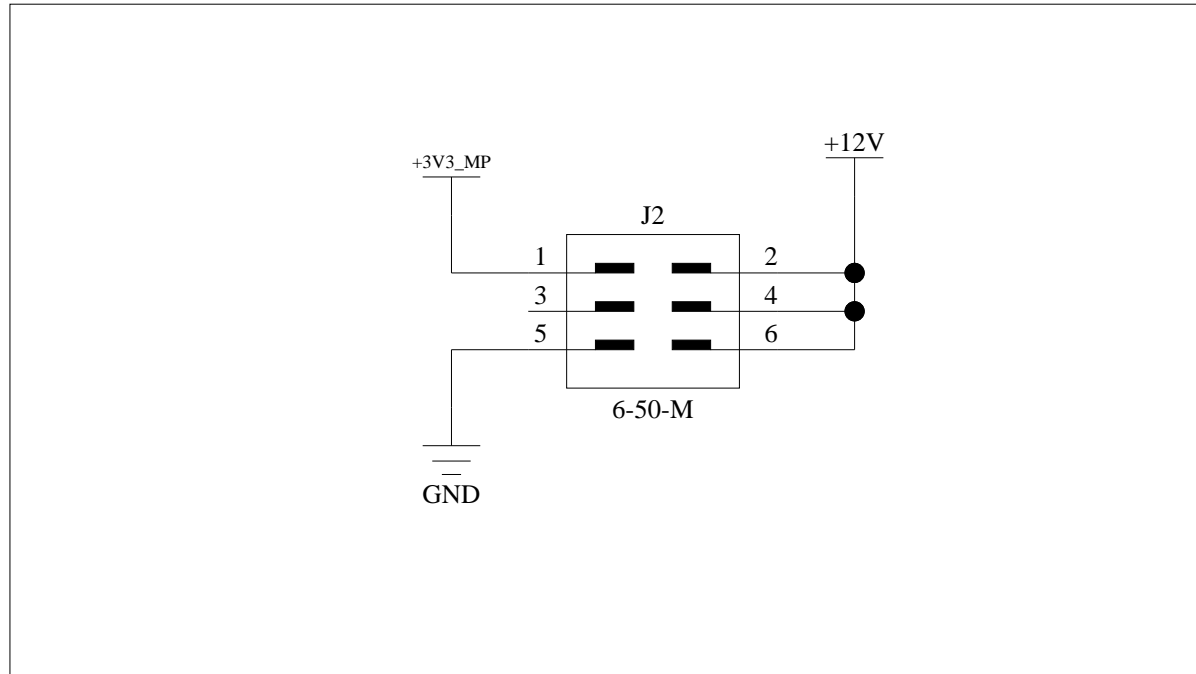
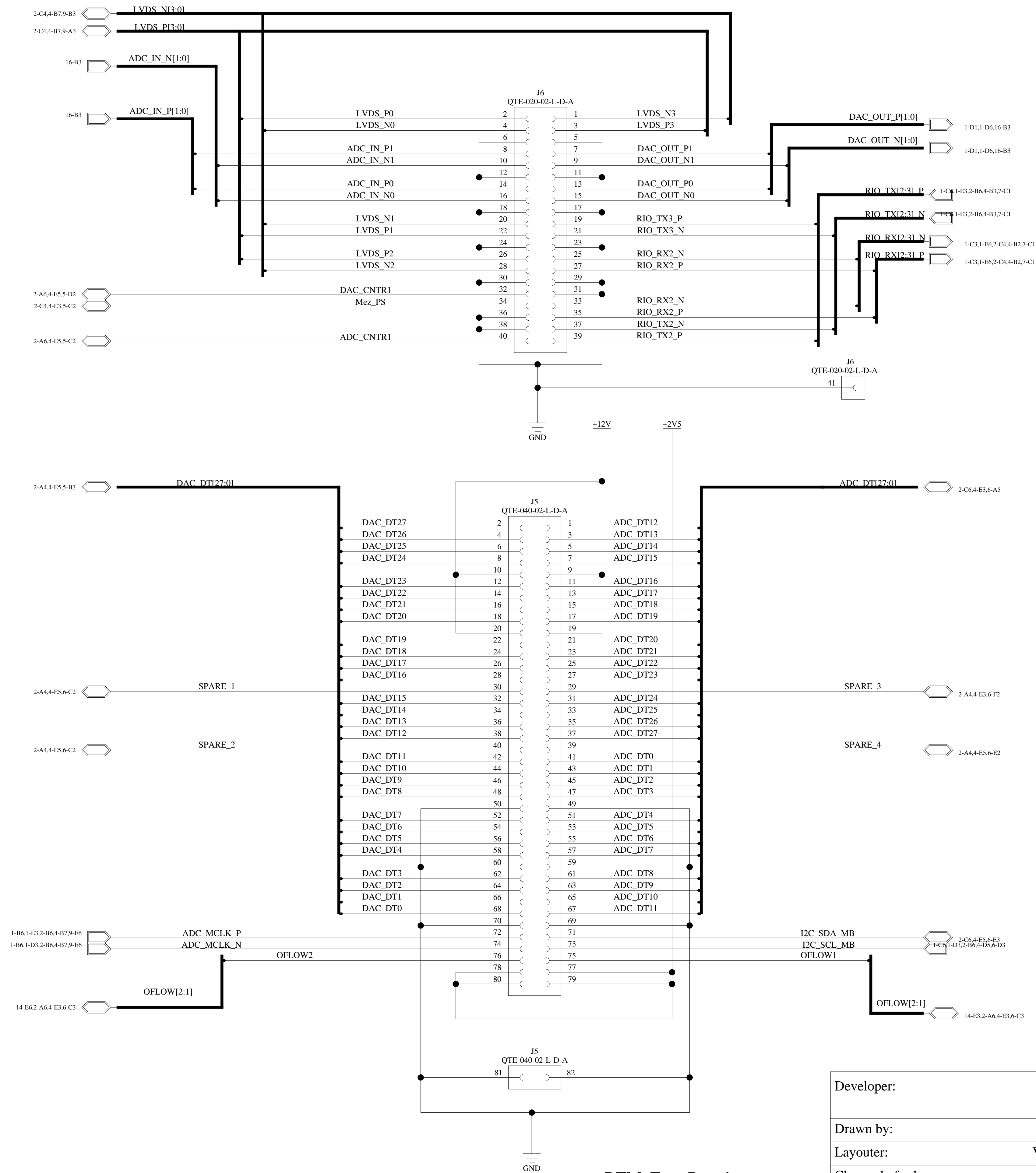


uRTM_Test_Board

Located at 1-7D
OBJECT PATH: top_level/ P30_P31_Header
Block: P30_P31 , Page 1 of 1
DESIGN SHEET 13 OF 21 (block from to)

Developer:	Project:			
	Schematic:			
Drawn by:	Sheet:			
Layouter:	DESY-			
Changed of sch:	Notkestrasse 85			
Date Changed:	D-22607 Hamburg			
Date of prod. data:	PCB No: 8528-00ML			
	Rev: Size: A3			
	PCB name: Test_uRTM			
	Sheet: 1 of 1			

Two connectors for Mezzanine Board
Only for Mezzanine Board with +2V5 compatible interface!!!



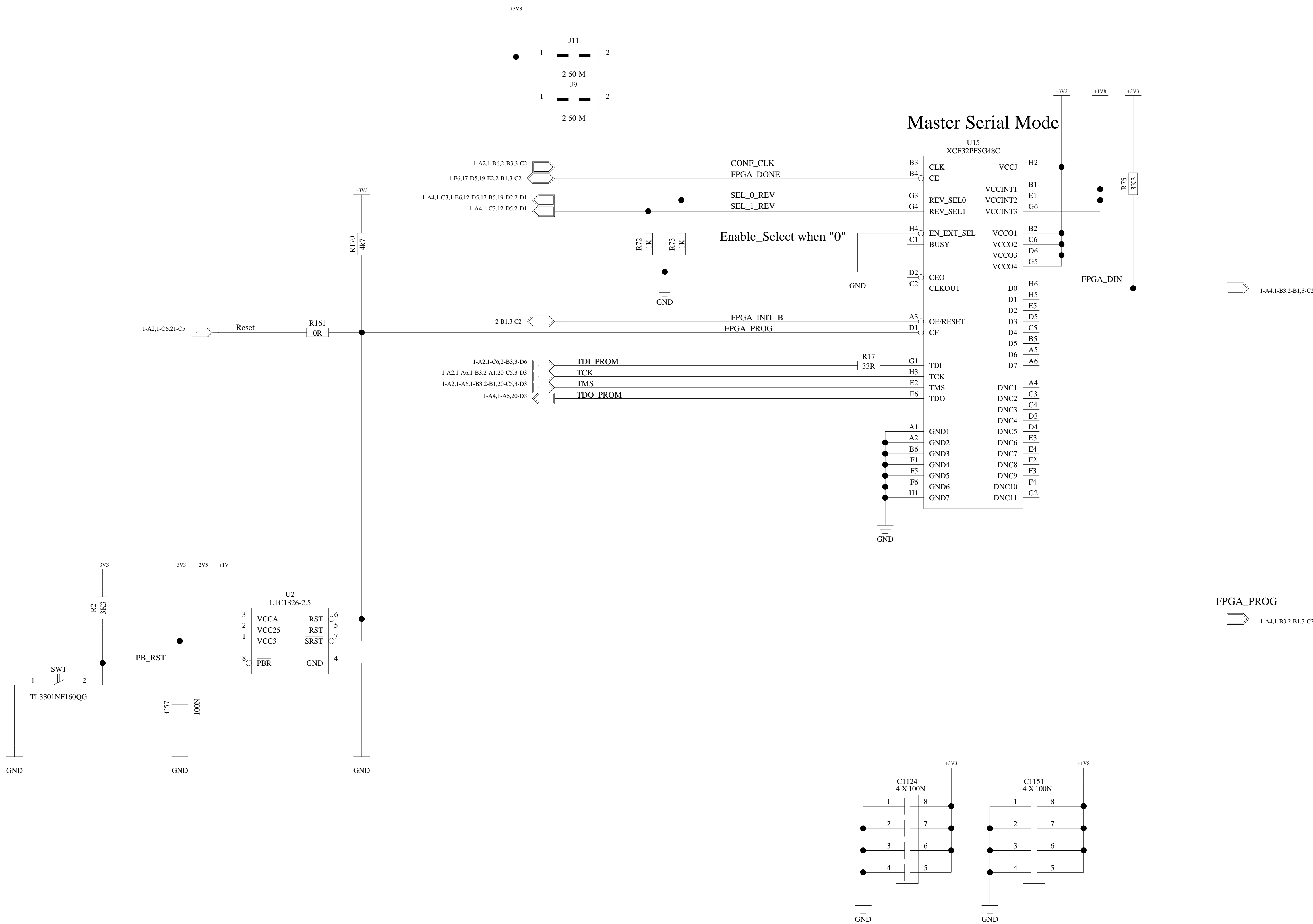
AUX_Power_Connector

uRTM_Test_Board

Located at 1-3E
OBJECT PATH: top_level/ Mez_Con
Block: Mez , Page 1 of 1
DESIGN SHEET 14 OF 21 (block from to)

Developer:	Project:			
	Schematic:			
Drawn by:	Sheet:			
Layouter:	DESY-			
Changed of sch:	Notkestrasse 85			
Date Changed:	D-22607 Hamburg			
Date of prod. data:	PCB No: 8528-00ML	Rev:	Size: A3	
	PCB name: Test_uRTM	Sheet: 1 of 1		

ispFlash and Reset FPGA

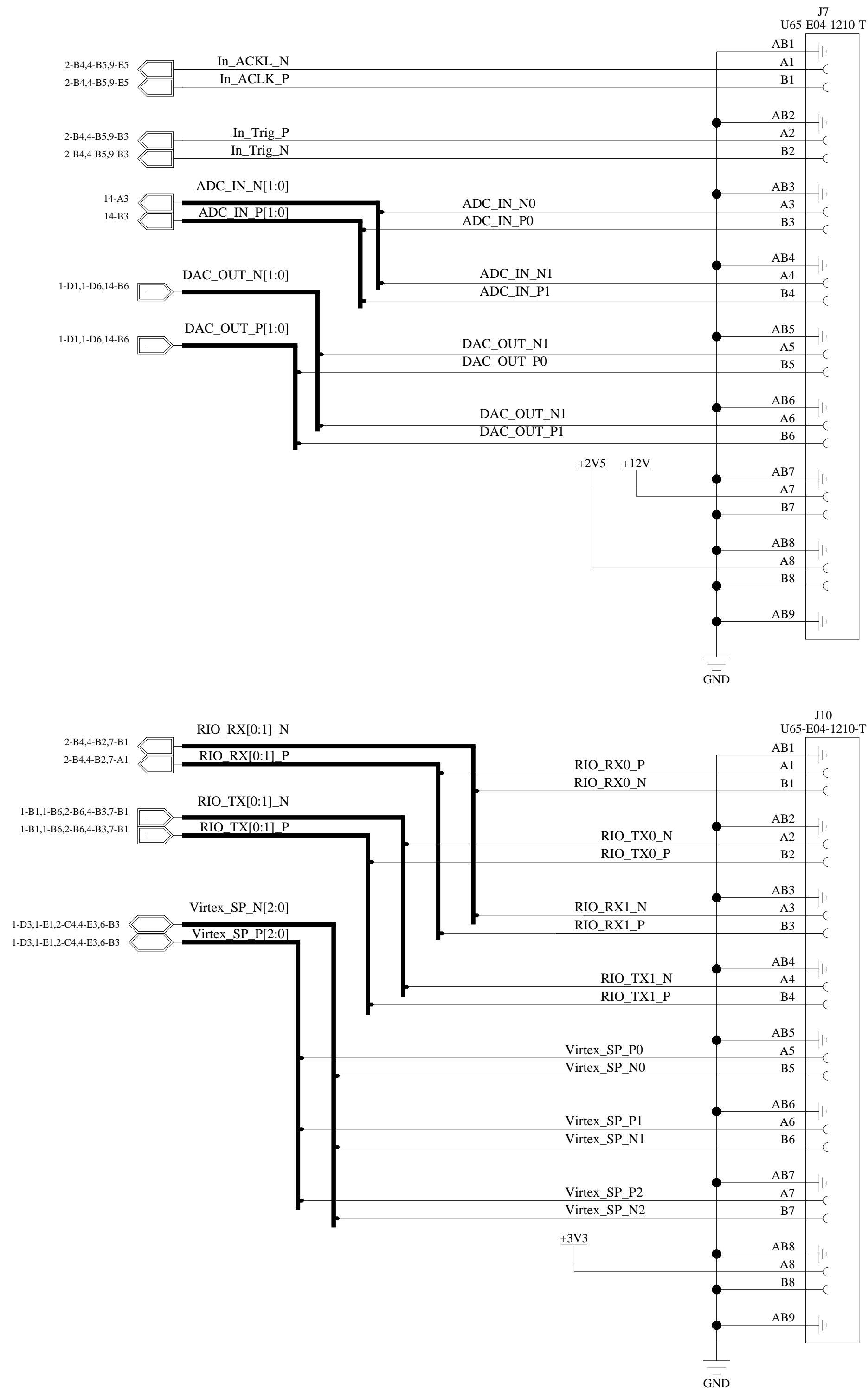


uRTM_Test_Board

Located at 1-3A
OBJECT PATH: top_level/ ispPROM
Block: ispPROM , Page 1 of 1
DESIGN SHEET 15 OF 21 (block from to)

Developer:		Project:			
		Schematic:			
Drawn by:		Sheet:			
Layouter: Vetrov		DESY-Notkestrasse 85 D-22607 Hamburg			
Changed of sch:					
Date Changed:		PCB No: 8528-00ML		Rev:	Size: A3
Date of prod. data:		PCB name: Test_uRTM		Sheet: 1	of 1

Two Front Panel Analog/Digital Interfaces Connectors

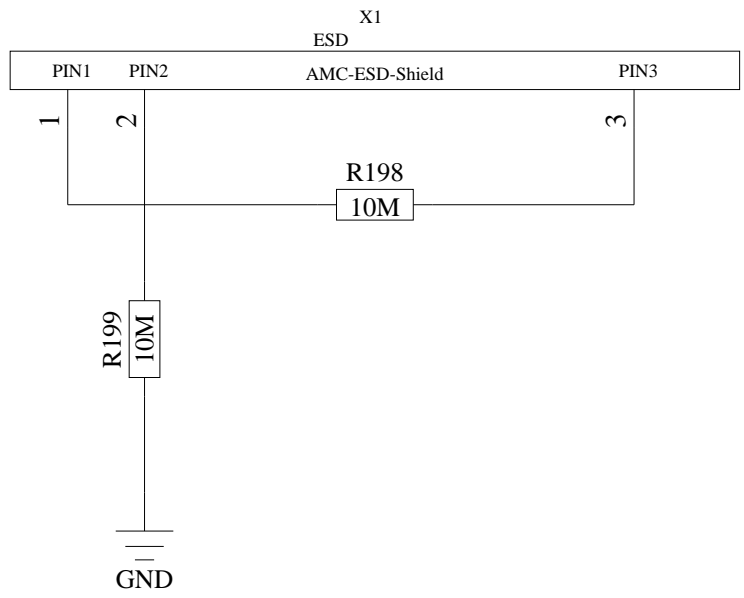
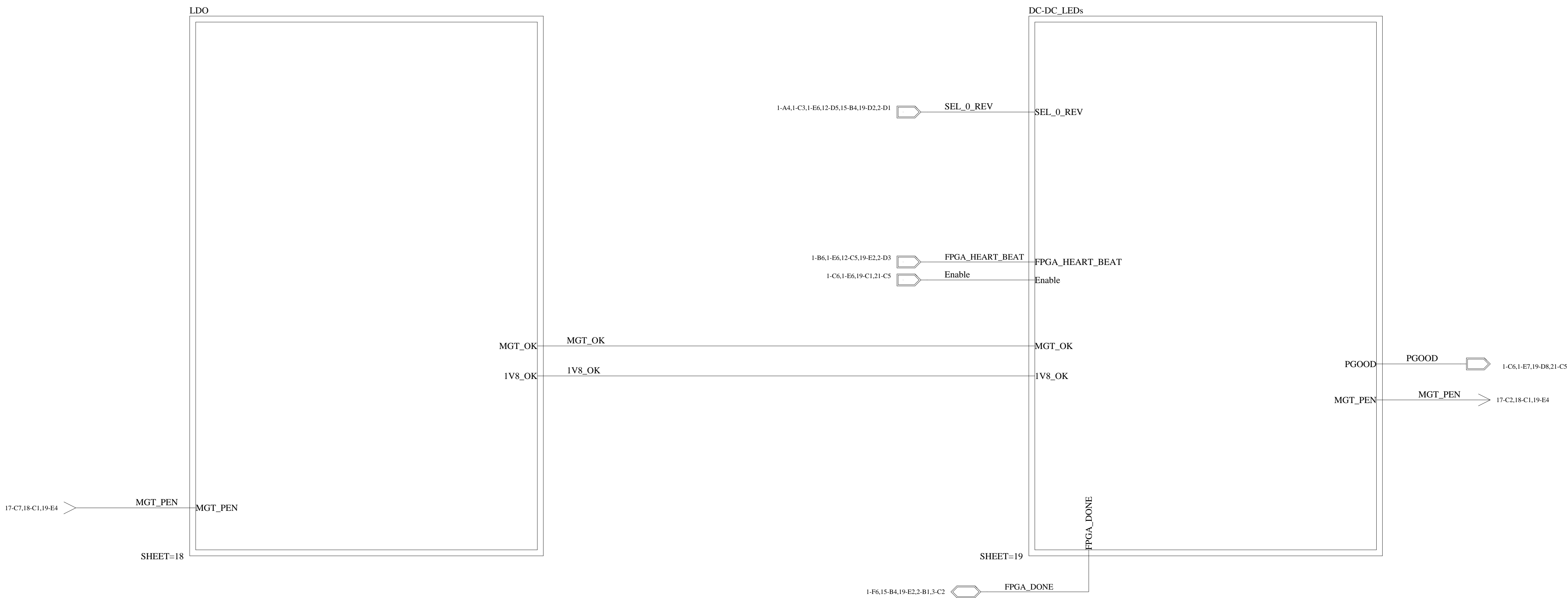


uRTM_Test_Board

Located at 1-1E
OBJECT PATH: top_level/ Digital_Analog_IO
Block: Digital_IO , Page 1 of 1
DESIGN SHEET 16 OF 21 (block from to)

Developer:	Project:			
	Schematic:			
Drawn by:	Sheet:			
Layouter:	DESY-Notkestrasse 85 D-22607 Hamburg			
Changed of sch:				
Date Changed:	PCB No: 8528-00ML	Rev:	Size:	A3
Date of prod. data:	PCB name: Test_uRTM	Sheet:	1 of	1

Power Converters and ESD Streep

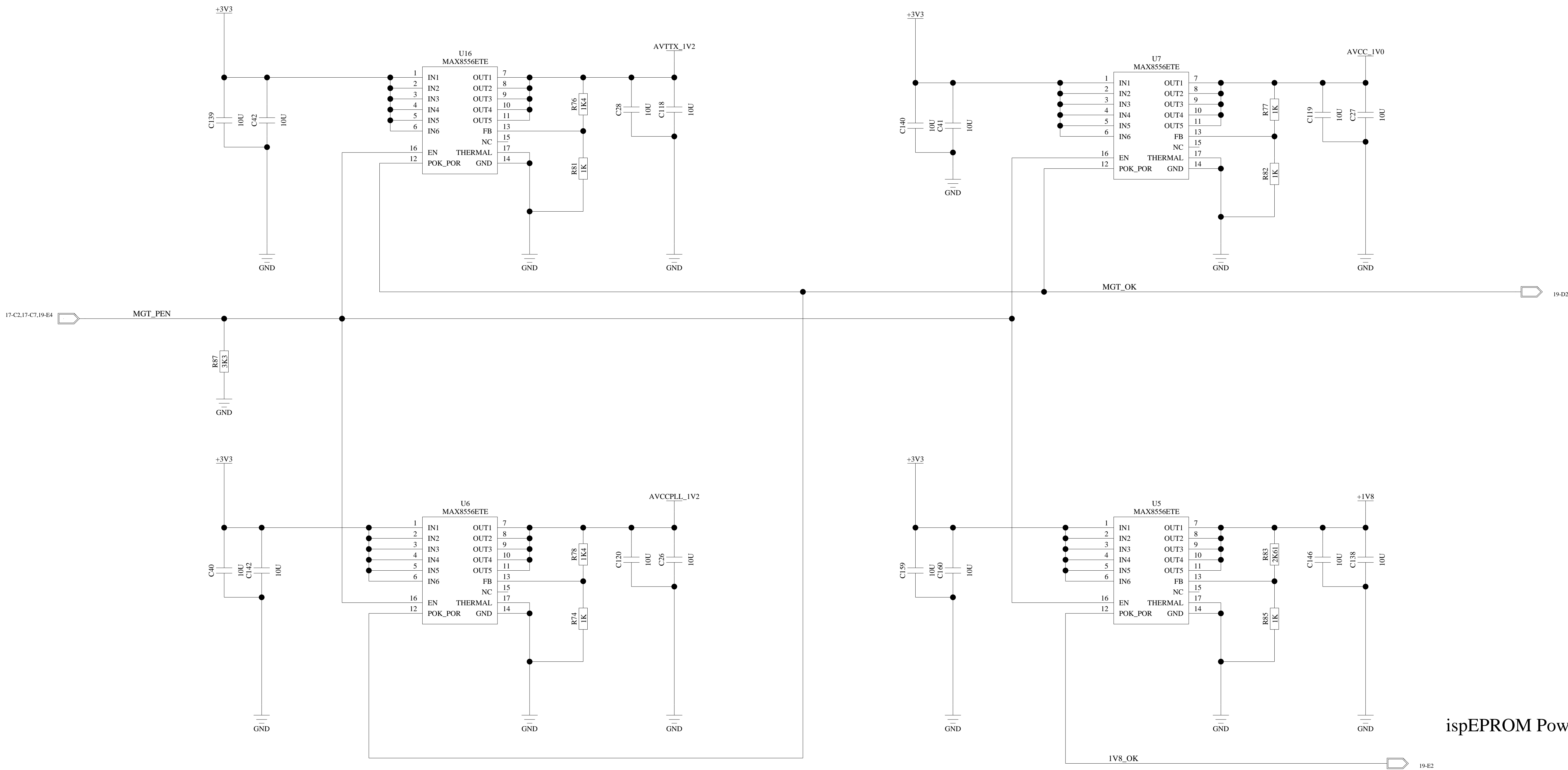


uRTM_Test_Board

Located at 1-6E
OBJECT PATH: top_level/ DC_LDO
Block: DC_LDO , Page 1 of 1
DESIGN SHEET 17 OF 21 (block from to)

Developer:	Project:			
	Schematic:			
Drawn by:	Sheet:			
Layouter:	DESY-Notkestrasse 85 D-22607 Hamburg			
Changed of sch:				
Date Changed:	PCB No: 8528-00ML	Rev:	Size:	A3
Date of prod. data:	PCB name: Test_uRTM	Sheet:	1 of	1

MGT and 1V8 Powers



ispEPROM Power

MAXIMUM Dropout Voltage is 0.1V if current is 4Ampers
Sturt-up voltage rampe to VDD no longer than 500us

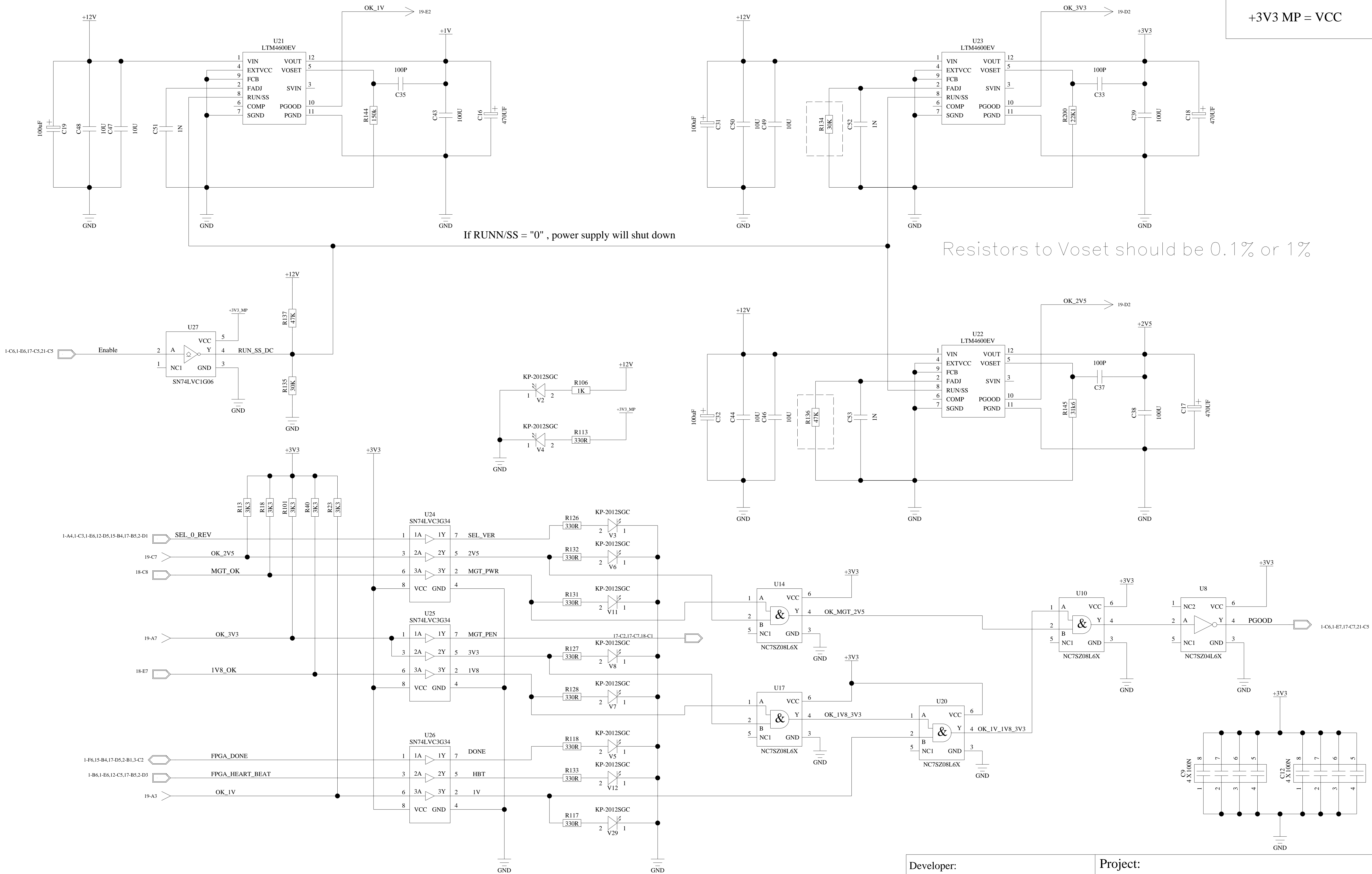
uRTM_Test_Board

Located at 1-2D
OBJECT PATH: top_level/ DC_LDO/LDO
Block: LDO , Page 1 of 1
DESIGN SHEET 18 OF 21 (block from to)

Developer:	Project:			
	Schematic:			
Drawn by:	Sheet:			
Layer:	DESY-			
Changed of sch:	Notkestrasse 85			
Date Changed:	D-22607 Hamburg			
Date of prod. data:	PCB No: 8528-00ML			
	Rev: Size: A3			
	PCB name: Test_uRTM			
	Sheet: 1 of 1			

Payload DC-DC convertors and Leds

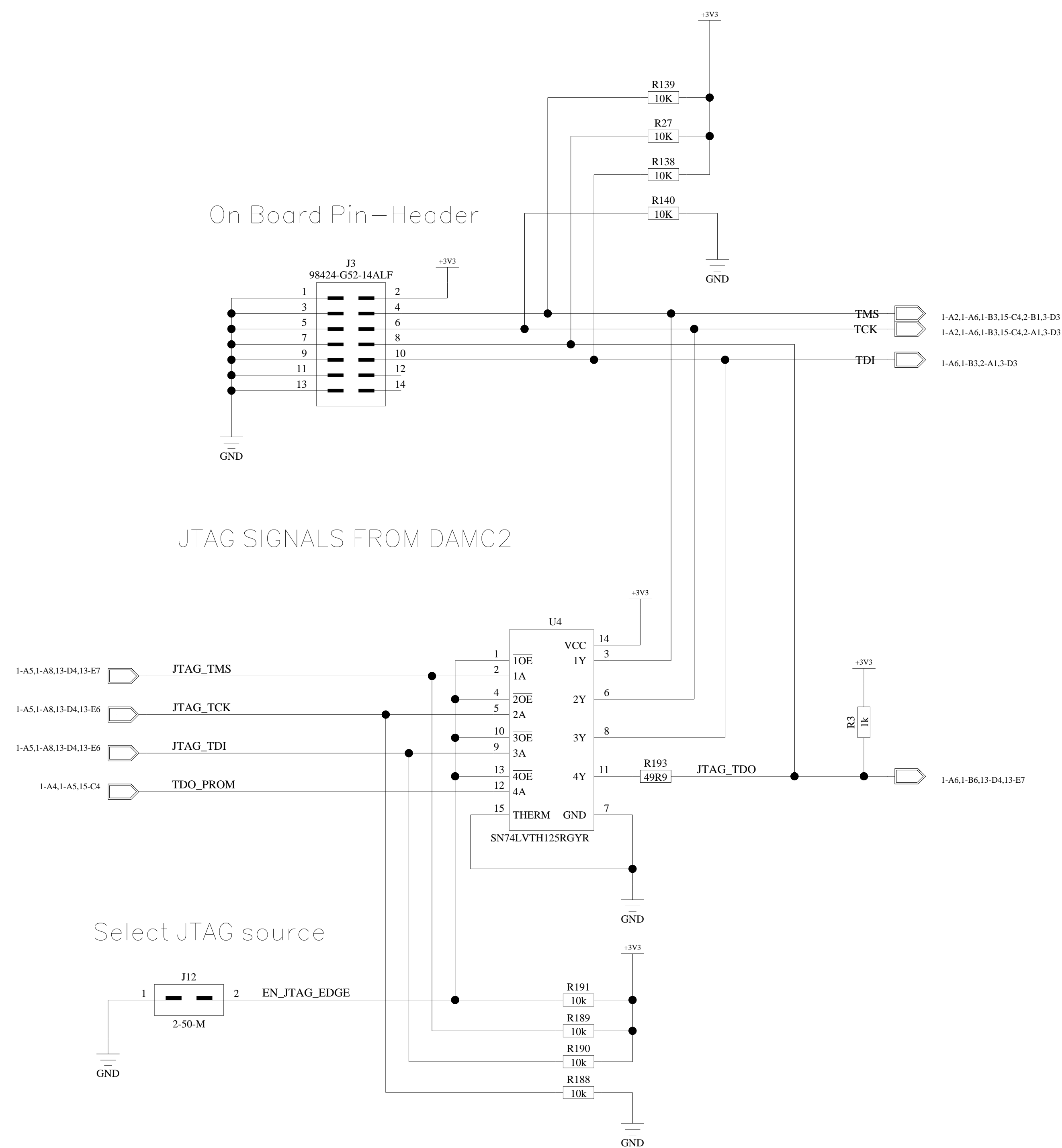
+3V3_Payload = +3V3
+3V3 MP = VCC



uRTM_Test_Board

Located at 1-5D
OBJECT PATH: top_level/ DC_LDO/DC-DC_LEDs
Block: DC-DC_LEDs , Page 1 of 1
DESIGN SHEET 19 OF 21 (block from to)

Developer:	Project:			
	Schematic:			
Drawn by:	Sheet:			
Layouter:	DESY-			
Changed of sch:	Notkestrasse 85			
Date Changed:	D-22607 Hamburg			
Date of prod. data:	PCB No: 8528-00ML	Rev:	Size: A3	
	PCB name: Test_uRTM	Sheet: 1 of 1		

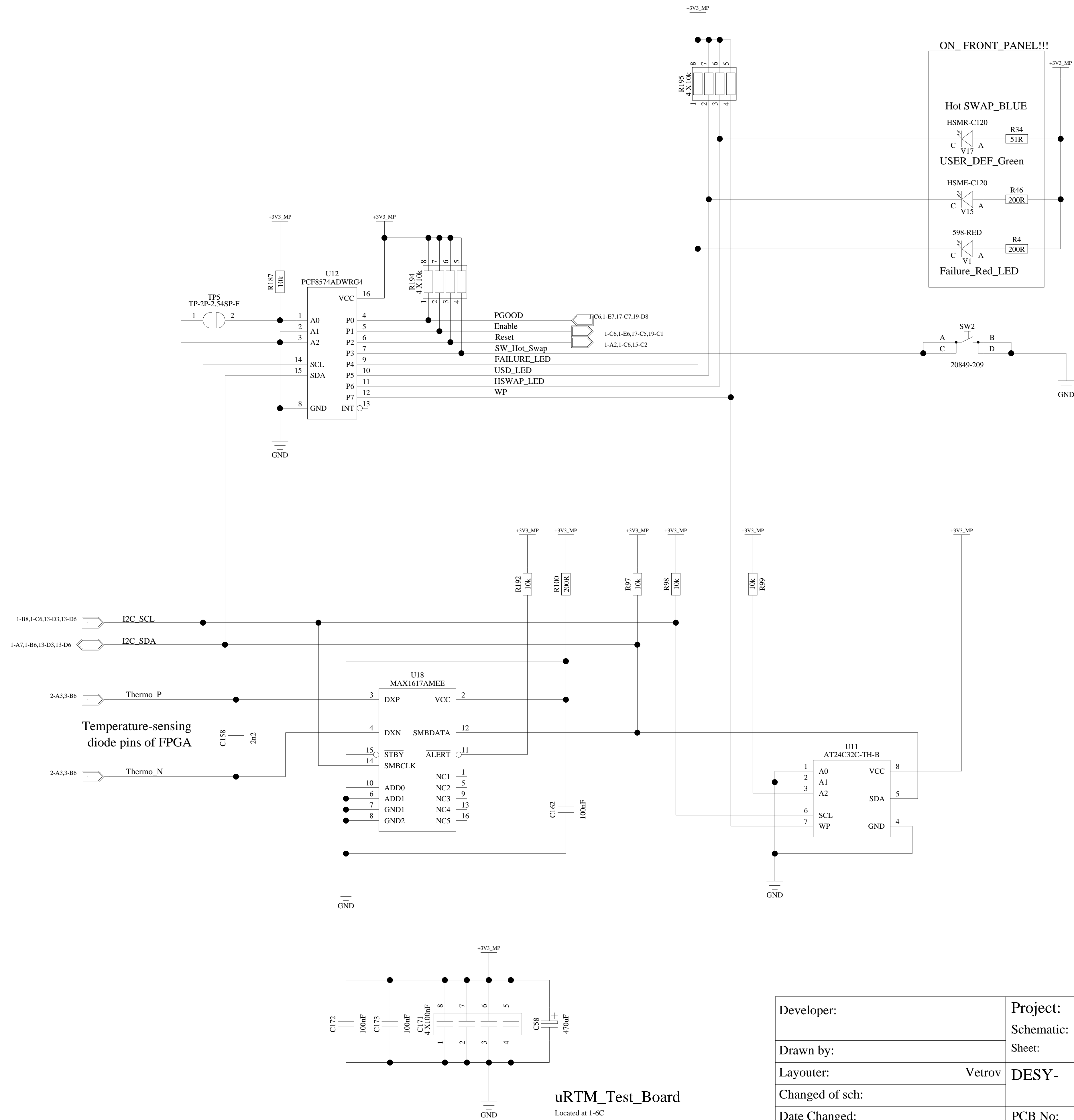


uRTM_Test_Board

Located at 1-5A
OBJECT PATH: top_level/ JTAG
Block: JTAG , Page 1 of 1
DESIGN SHEET 20 OF 21 (block from to)

Developer:	Project:			
Drawn by:	Schematic:			
	Sheet:			
Layouter: Vetrov	DESY-		Notkestrasse 85	
Changed of sch:			D-22607 Hamburg	
Date Changed:	PCB No:	8528-00ML	Rev:	Size: A3
Date of prod. data:	PCB name:	Test_uRTM	Sheet:	1 of 1

IPMI, Hot-Swap Switch, SEEPROM and Temp. Sensor



Developer:	Project:		
	Schematic:		
Drawn by:	Sheet:		
Layouter: Vetrov	DESY- Notkestrasse 85 D-22607 Hamburg		
Changed of sch:			
Date Changed:	PCB No: 8528-00ML	Rev:	Size: A3
Date of prod. data:	PCB name: Test_uRTM	Sheet: 1 of 1	