XFEL Timing System Specifications

Version 0, 31.5.2010

PRELIMINARY

Table of Contents

1 Introduction

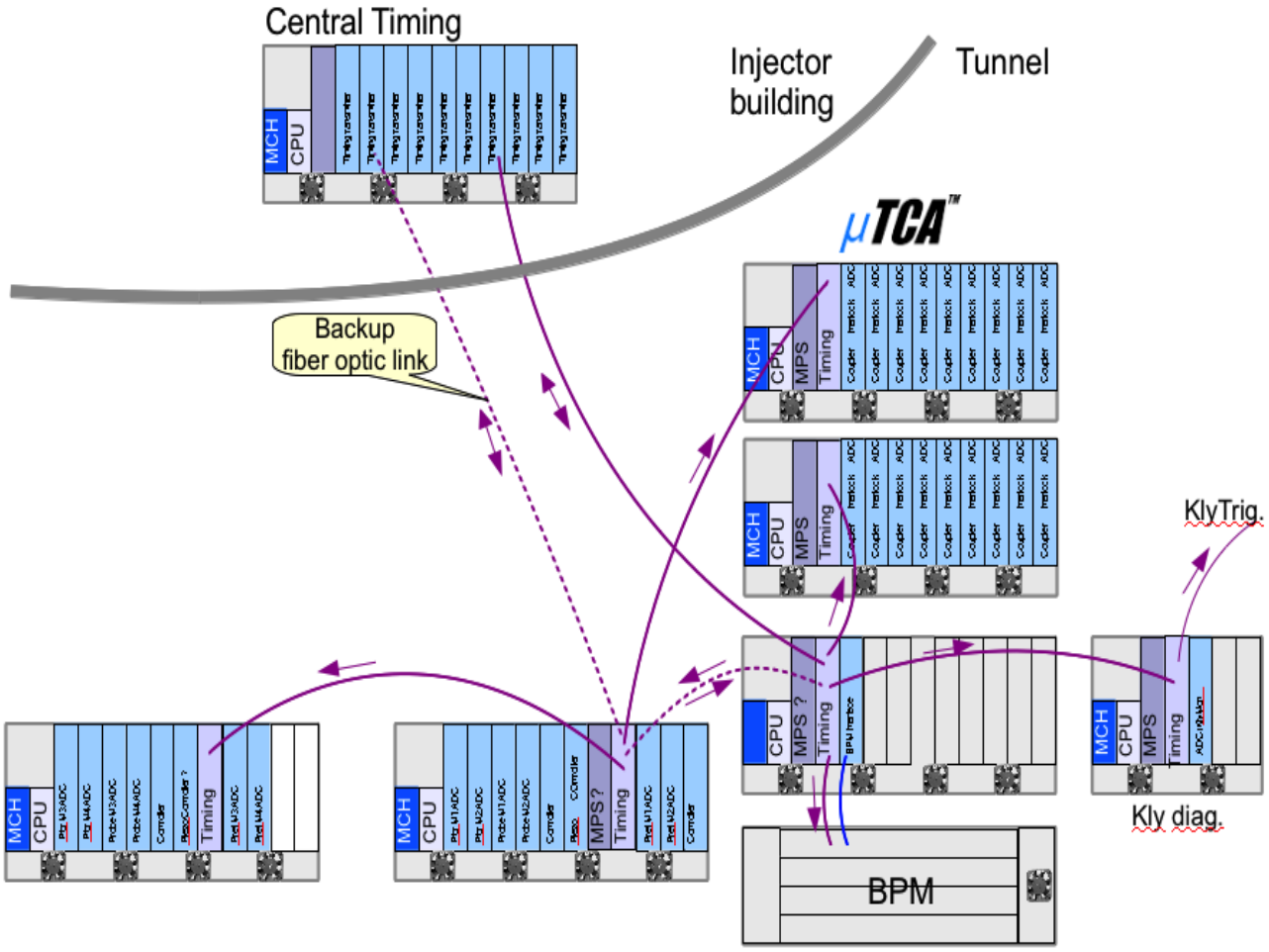
An introduction of the XFEL timing concept can be found under:
http://flash.desy.de/sites/site_vuvfel/content/e403/e1644/e1136/e1137/infoboxContent1838/TESLA-2006-12.pdf

2 Applications

2.1 XFEL

The XFEL timing will be distributed from a central place in the injector building close to the Master Oscillator (MO). It will receive a stable 1.3GHz clock from the MO. A further input will be a 50Hz signal from the mains.

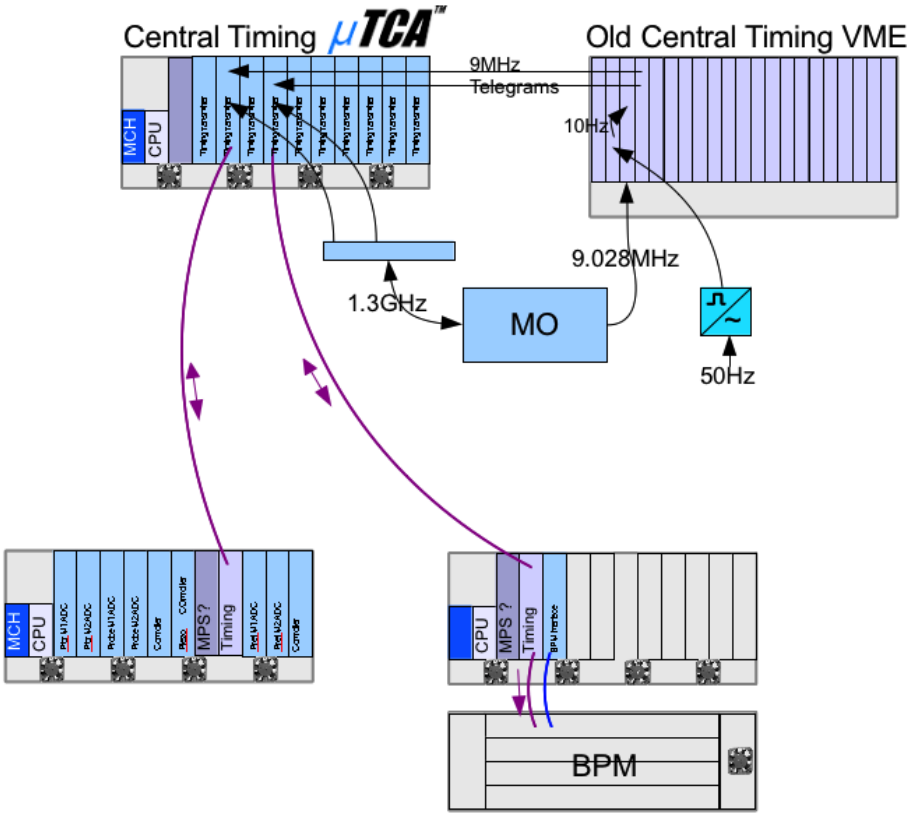
For the receivers a redundant option is foreseen. Two timing receivers can receive the 1.3GHz telegrams from the central station via separate fiber optic cables. A link between the two receiver AMC's is used as an update channel. If one link to the central timing transmitter fails the receiver detects this and switches to the update link from the second receiver. This update link is bidirectional and directly transmits the incoming telegrams to the second AMC.



Drawing 1: Timing links of one RF section in XFEL

2.2 FLASH and FLASH2

The FLASH timing system is based on a event distribution system from Fermilab. It is TTL based and works with 9.028MHz as the main clock frequency. Triggers are derived from the 50Hz mains by an AC/DC converter. 50Hz is the input for a rep-rate generator that has programmable divider to generate e.g. the 10 Hz macro pulse frequency for FLASH. The incoming 50Hz is synchronized with the 9MHz from the master oscillator (MO). The output triggers a clock generator which then generates events. Events are manchester encoded on the 9.028MHz and send as telegrams to all timing receiver boards. A receiver extracts the 9MHz clock and the events from the telegram stream.



Drawing 2: Communication of the old FLASH timing with the new XFEL timing to be operated in FLASH

To be able to run the old timing and the new XFEL timing system in parallel in FLASH, is is required to receive the 9MHz telegrams from the old timing and to extract the events from it as the basis for the events distributed in the new timing.

Description	Module Type	Number	Date
Central event generator	Transmitter	6	01.06.10
Kicker	Receiver	3	01.06.10
BPM test Geb 49	Receiver	1	
3.9GHz system	Receiver	1	
LLRF ACC1	Receiver	1	01.06.10

Table 1: Timing modules required for FLASH

Required number of timing modules for FLASH2 have to be defined. FLASH2 will be equipped with the new timing system only. Since FLASH2 has a similar bunch distribution as XFEL, with two or more users of a bunch train, the new timing system is required. Furthermore, it is planned to use the same hardware of XFEL for FLASH too which is based on µTCA.

Description	Module Type	Number	Date
Toroid protection system	Receiver	2	01.06.12
BPM	Receiver	4	01.06.12
Machine Protection System	Receiver	3	01.06.12
Diagnostics, Photon Diag.	Receiver	3	01.06.12
Central event generator	Transmitter	6	01.06.12

Table 2: Very preliminary list of timing modules required for FLASH2

2.3 REGEA

The REGEA accelerator should be equipped with the new timing only.

Description	Module Type	Number	Date
Event generator	Transmitter	1	01.06.10
LLRF controller	Receiver	1	01.06.10
Laser	Receiver	1	?
Monitoring (optional)	Receiver		

Table 3: Timing modules required for REGEA

2.4 PITZ

PITZ requires a new timing system for the test of the Transverse Deflecting Cavity System and the modulator tests. For the TDS a connection to the old PITZ timing system is required. This is the same connection as in FLASH (9.028MHz telegrams to be decoded and inserted as events in the new timing).

Description	Module Type	Number	Date
Event/trigger generator	Transmitter	1	
Modulator tests	Receiver	1	
Event/trigger generator	Transmitter	1	01.07.10
LLRF controller	Receiver	1	01.07.10

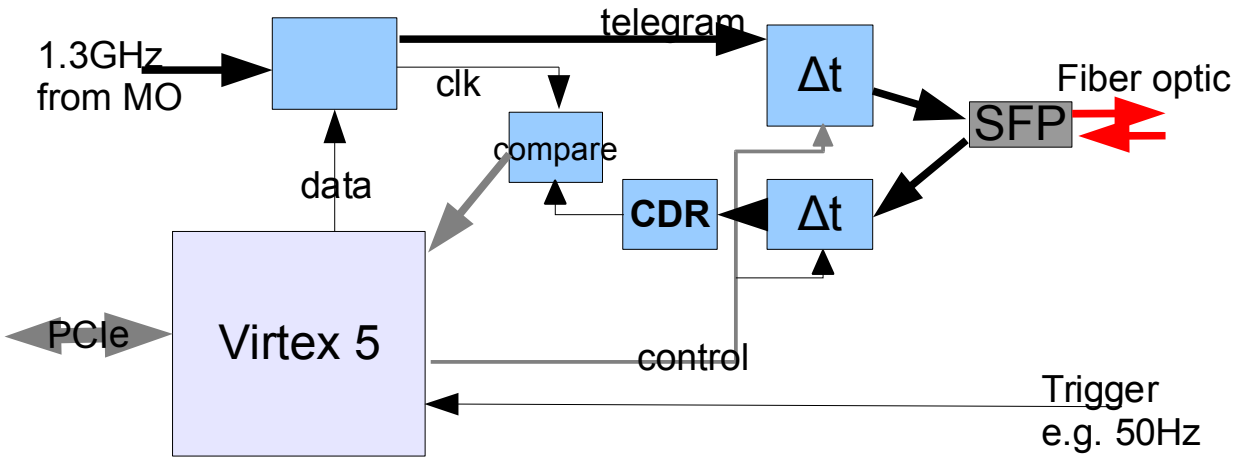
Table 4: Timing modules required for PITZ (TDS)

2.5 Labs

Description	Module Type	Number	Date
LLRF Event generator	Transmitter	1	01.06.10
LLRF controller	Receiver	1	01.06.10
Timing tests/programming HH	Transmitter	1	available
Timing tests/programming HH	Receiver	1	available
Exp DAQ group	Transmitter	1	01.07.10
Exp DAQ group	Receiver	1	01.07.10
Timing tests/programming Stockholm	Transmitter	1	available
Timing tests/programming Stockholm	Receiver	1	available

Table 5: Timing modules required for the labs (test setups)

3 *Timing Transmitter*



Drawing 3: Transmitter block diagram

Two versions are planned:

1. Single size AMC as a combined receiver and transmitter
2. Double size AMC with more fiber optic links (TBD)

Central timing transmitter inputs:

- 1.3GHz from master oscillator (level to be defined)
- 50 Hz from a line filter, level: LVDS
- Synchronization of the transmitters via μTCA backplane (TBD)

Transmitter outputs:

- 10 (up to 16) fiber optic (SFP) outputs with telegrams, bidirectional
- sync on backplane (TBD)

The link between a central station and receiver boards is accomplished by a bidirectional fiber optic cable. The return line of this connection is used to compensate drifts and to measure the round trip time. On this link a stable clock is modulated with encoded 8b/10b data. This combined clock and data is decoded at the receiver and the clock and data is separated.

A telegram starts with a START comma character followed by a command (CMD) followed by optional data bytes and ends with correction bytes and an END comma character:

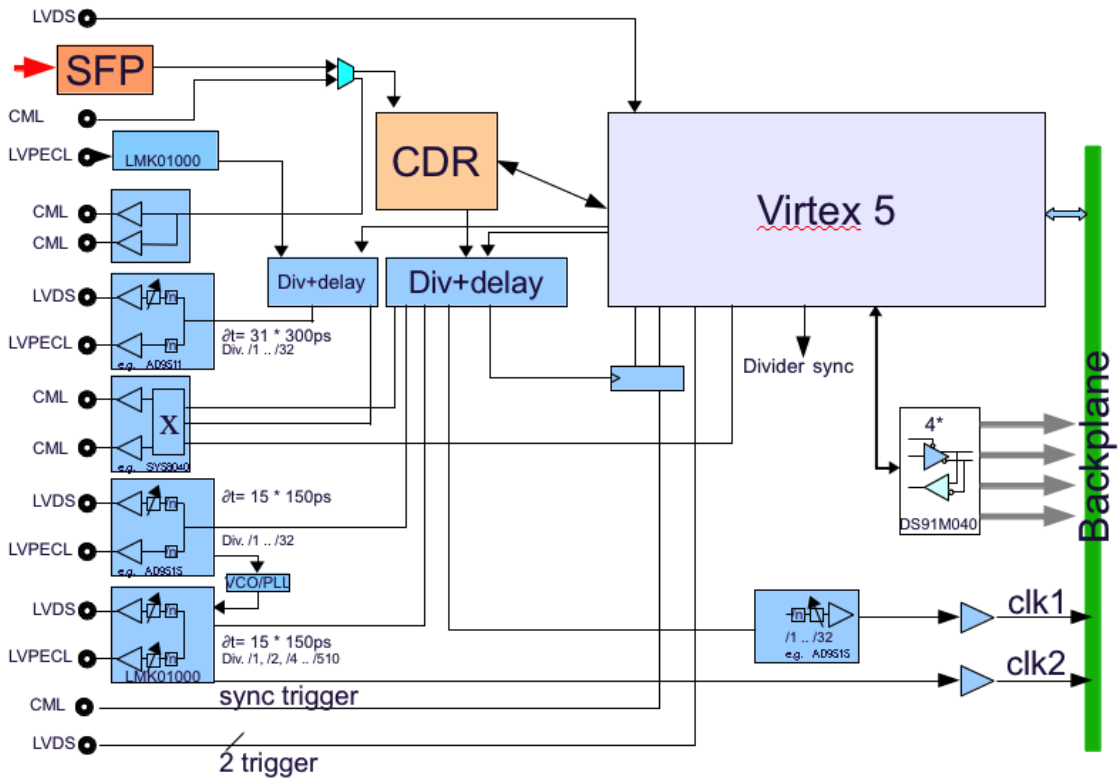
<START><CMD><DataByte1><DataByte1><CORR><END>

In case that the stability of the clock recovery is not good enough it could be improved by adding 11 “Filler” bytes between all bytes. The fillers are composed of regular bit changes to allow a clean phase comparison between incoming and outgoing data streams. THIS IS AN OPTION ONLY and probably not required. To be able to distribute the incoming 1.3GHz bit rate on a slower 108MHz clock a 1/12 data buffering on the receiver is required. The sender has to provide enough space between telegrams to not overrun the receiver.

Name	Function	Data byte
Filler	used for phase comparison to compensate drifts (D10.2)	0x4A
Sync	Synchronization of the receivers, before each macro pulse	0x10
Probe	Measure total link delay	<1>
Event	Trigger event	<2>
	Event number (0..255)	EEEEEEEE
	Relative time to Sync (high byte)	TTTTTTTT
	Relative time to Sync	TTTTTTTT
	Relative time to Sync	TTTTTTTT
	Relative time to Sync (low byte)	TTTTTTTT
Mode	Linac operation mode	<3>
	Mode, byte	MMMMMMMM
EventNumber	Unique number for each macro pulse	<4>
	4 bytes with event number	4 * byte
Sequence #	The sequence number of the actual macro pulse	<7>
	Sequence number in the range of 0..3 (max 255)	SSSSSSSS
Pattern	Byte array to describe the e.g. bunch fill pattern as a function of location	<5>
	Type of table (e.g. bunch pattern)	PPPPPPPP
	Location description (valid on a certain beam line)	LLLLLLLL
	Sequence number (valid for a certain linac cycle or sequence)	SSSSSSSS
	High byte of length	NNNNNNNN
	Low byte of length	NNNNNNNN
	Byte array with fill pattern	N * byte
Time	Abs. time, 64 bit	<6>
		8 * byte
MPS	Interlock from MPS was detected	<7>
	Time of interlock event (high byte)	TTTTTTTT
	Time of interlock event	TTTTTTTT
	Time of interlock event	TTTTTTTT
	Time of interlock event (low byte)	TTTTTTTT
Trigger1	Direct trigger 1	<10>
Trigger2	Direct trigger 2	<11>
Trigger3	Direct trigger 3	<12>
Trigger4	Direct trigger 4	<13>
LinkDelay	Delay time from sender to receiver ??????	

Table 6: Data telegrams, the <x> fields needs to be replaced with hex numbers (TBD)

4 Timing Receiver



Drawing 4: Timing receiver block diagram of the first prototype, to be corrected

Timing receiver:

- receives clock + events on fiber optics
- loop-back the clock + events to sender
- decodes events
- generates programmable timing signals out of the events (~ 1ns .. 100ms)
- delay and output pulse width are individually programmable
- generates programmable clocks (100kHz .. 1.3GHz)
- generates local interrupts within a crate (programmable)
- provides data registers for macro pulse type and event number
- data register for permissions
- general purpose registers or tables
- has a readable counter for precise time measurements, set by an abs. time event

- receives time delay of the link form transmitter to correct delays
- sender for event broadcasts on Ethernet (implemented in software, timing server)

Inputs:

- SPF plug with fiber optic receiver for incoming telegrams
- Harlink connector for incoming telegrams, copper and twisted pair (level: LVPECL?)

Outputs:

- on AMC plug: TCLKA (Clk1), TCLKB (Clk2)
- on front plugs
- variable frequency and var. ps/ns delay
- optional gated with pattern and/or start/stop event
- trigger outputs on front, harLink plug, level: LVDS, PECL, CML???
- trigger outputs on AMC plug
- encoded clock output with 108MHz bit rate on AMC plug
- variable pulse width and var delay in the range of >=100ms, ns resolution (front)
- one output with ps delay in addition (front)

Mechanics (receiver):

AMC boards: single and double wide boards, mid size form factor.

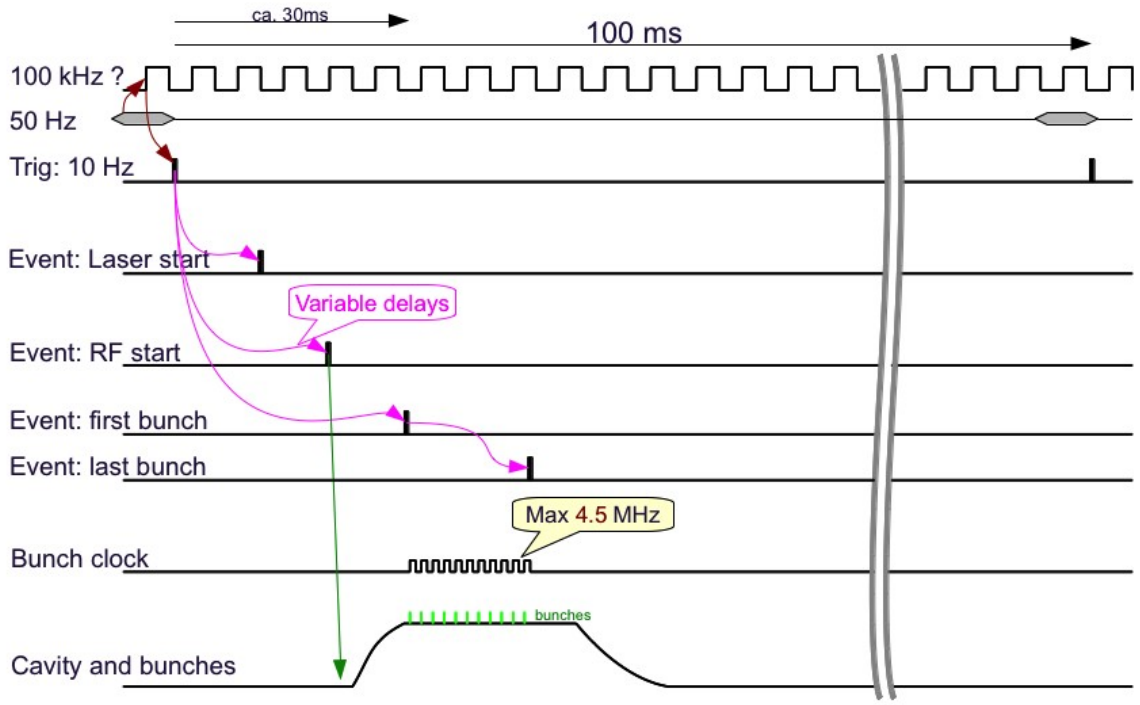
5 Events in XFEL

Events are used to synchronize all subsystems in XFEL.

Event #	Function	Users
	Early trigger	WireScanner, cameras
	Laser start	
	Modulator start	RF
	LLRF start	RF, LLRF
	1. bunch	
	Readout trigger	CPU interrupt
	ADC trigger	Data acquisition hardware

Relations between events have to be defined:

- Definition of subsystems with a fixed timing relation
- Event numbers and the meaning and relation of events
- Definition of subsystem event groups that can be shifted together



Drawing 5: Preliminary event sequence principle of the XFEL

Event sequence in XFEL (TBD).

Grouping of events in XFEL (very preliminary):

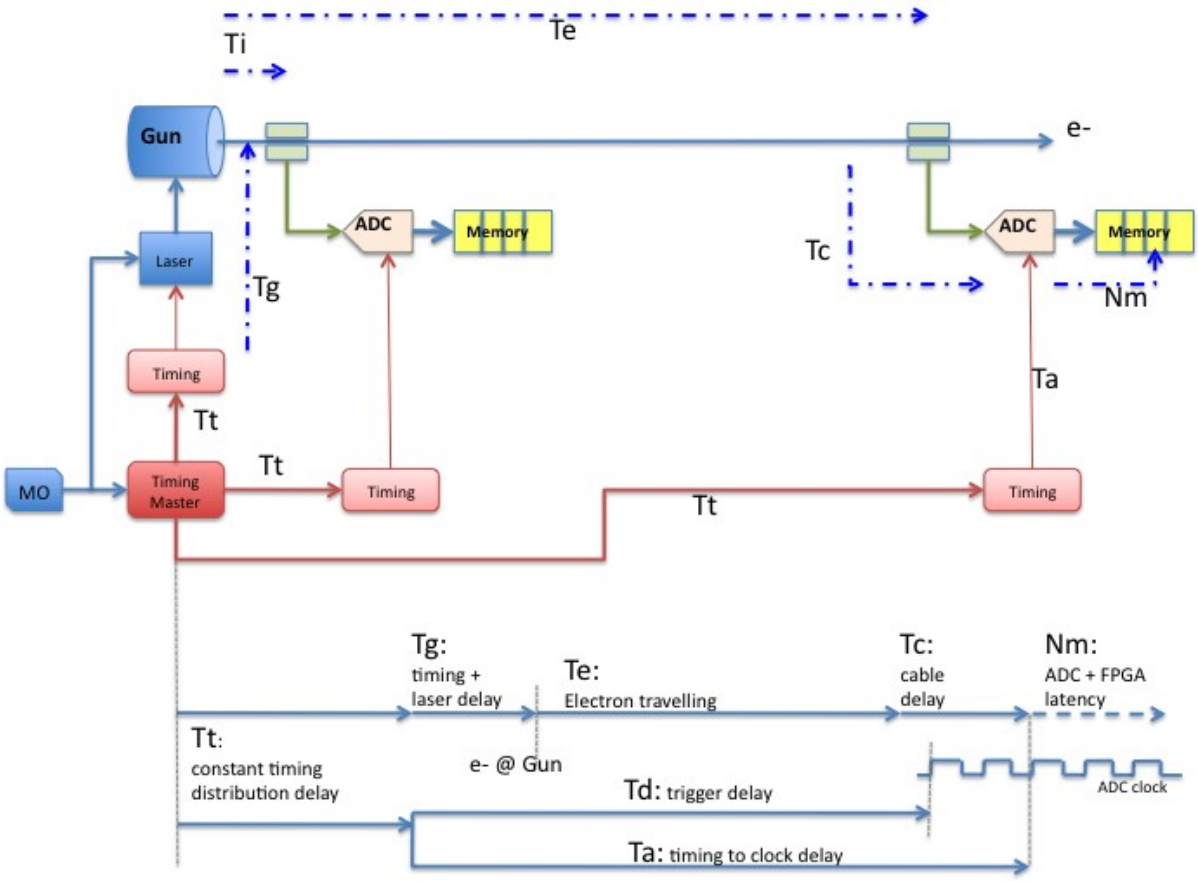
Event group	Description
Bunch position	Injector laser and relative first bunch position
Gun RF	Temporal position of the Gun relative to the bunches
ACC RF	Main RF (all acceleration modules without gun) rel. to bunches
...	

To be able to shift e.g. the gun RF in relation to the beam all timing of the gun (the klystron and LLRF) must derive the timing from the same event group number. One parameter will be defined in the control system to shift the whole gun RF without influencing the other timings. Special care has to be taken that the recorded data is in a correct position to the overall diagnostics shown in the control system.

6 Calculation of the timing relations

Explanation of the drawing:

	Description	Derived from
Tt	Constant delay between the master timing sender and all receivers	Constant
Tg	Delay timing receiver to electron in the gun	To be measured
Ti	Delay of electron detected in a beam monitor in the injector	To be calculated from the z-postion of the monitor
Te	Delay of electron detected in a beam monitor	To be calculated from the z-postion of the monitor
Ta	Delay between timing receiver and ADC clock	To be measured
Tc	Cable delay from beam monitor to ADC	Calculated from the cable length
Nm	ADC latency plus latency of the memory in number of clock cycles	Calculated from data sheets

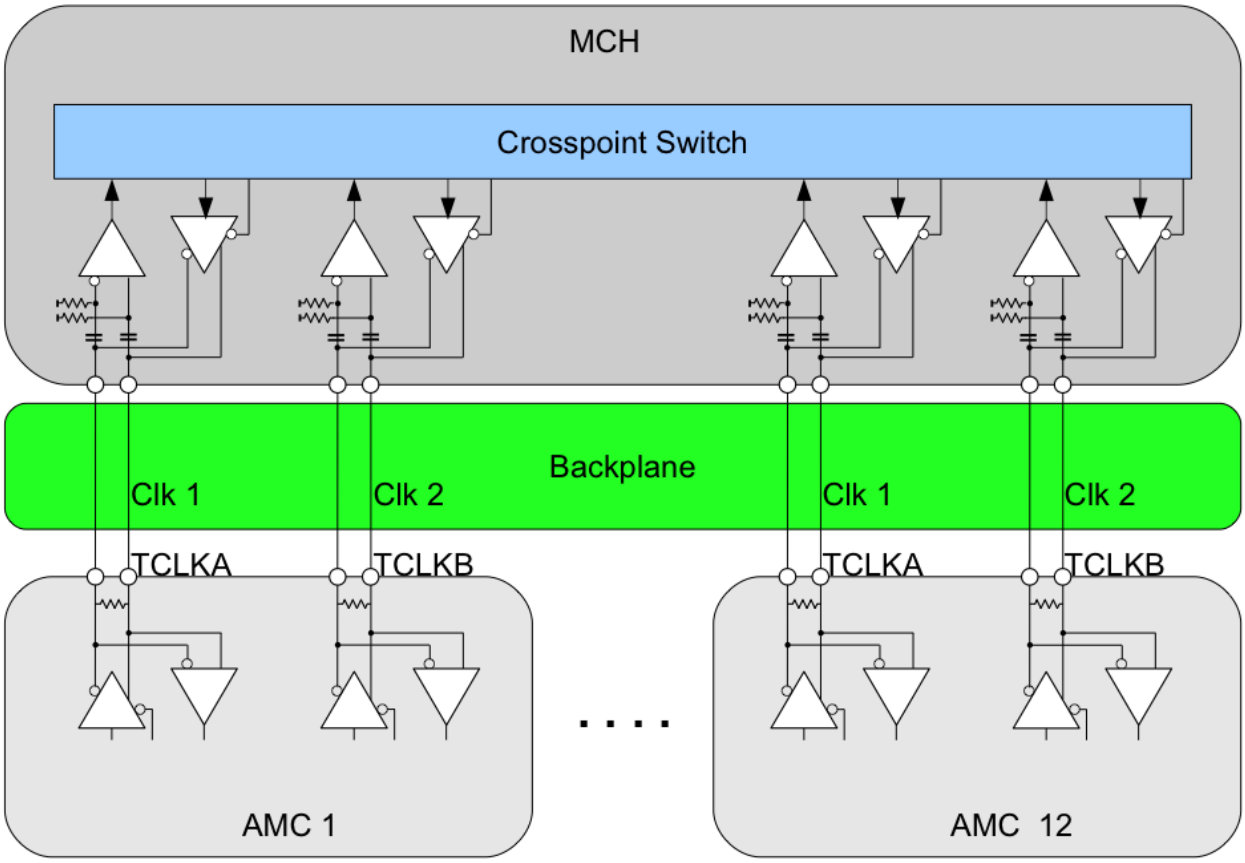


Drawing 6: Calculation of the timing relations

With these numbers one should be able to calculate the position of data in the memory for e.g. the first bunch.

7 Timing distribution within a µTCA crate

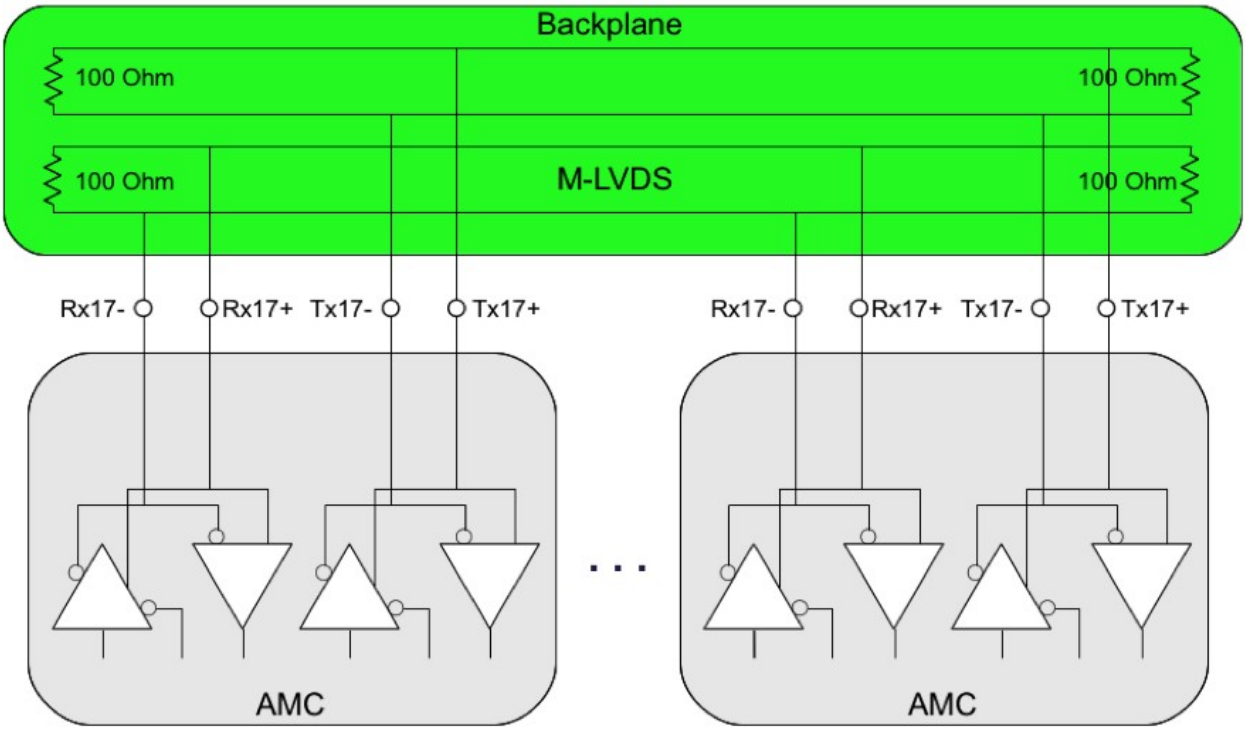
TCLKA and TCLKB are used to distribute low jitter clocks (see Drawing 7). The timing receiver is the source of the clocks and the MCH distributes the clocks to all requesting AMC's. The electrical standard is LVDS (as defined in AMC specs) and the connections are point-to-point with proper termination.



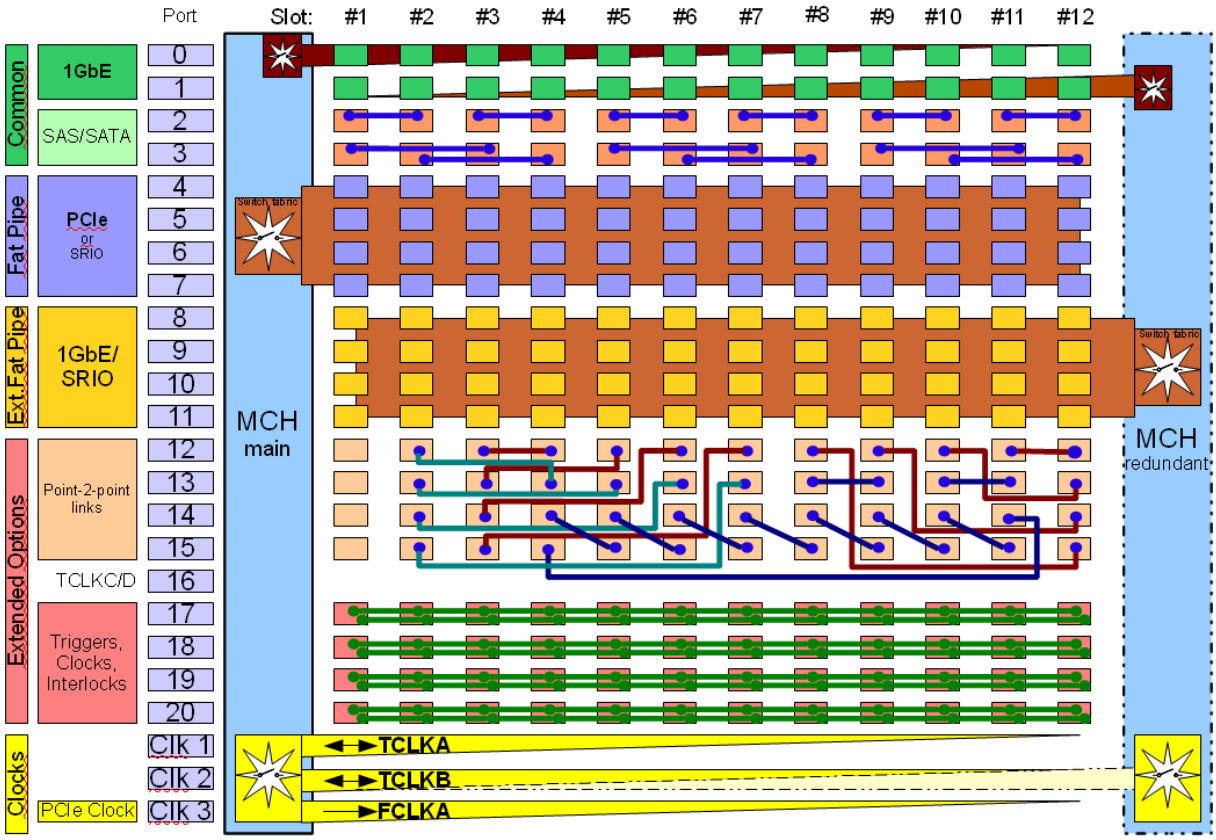
Drawing 7: Radial clock distribution within a µTCA crate

The backplane as defined for the XFEL project will contain in addition 8 M-LVDS lines to distribute further clocks, triggers and interlock signals. It is foreseen to use one of these lines to distribute an encoded clock that contains all the event information. This clock shall have a frequency of 108 MHz (1.3GHz/12) with a fixed phase relation to the master oscillator and the XFEL or other facility main RF. It will pass the same information of the 1.3GHz clock distribution between the master timing and the receivers to the AMC modules in a crate but with a factor 12 slower rate. The electrical connection is shown in drawing 8.

Port	Name	Description
Rx17	TrigStart	Trigger to start ADC readout
Tx17	EnClock	Encoded 108MHz clock
Rx18	BunchClock	100kHz ... 4.514MHz clock in sync with bunches
Tx18		
Rx19	Reset	Reset of counters, dividers to synchronize the next shot
Tx19	Ilock0	Interlock wired OR line 0
Rx20	Ilock1	Interlock wired OR line 1
Tx20	Ilock2	Interlock wired OR line 2



Drawing 8: Bussed clock, trigger and interlock lines. One of 4 ports shown.



Drawing 9: 12 slot backplane (preliminary)

8 Parameter distribution

Bunch patterns f(location, sequence number)

9 Interface to the Machine Protection System

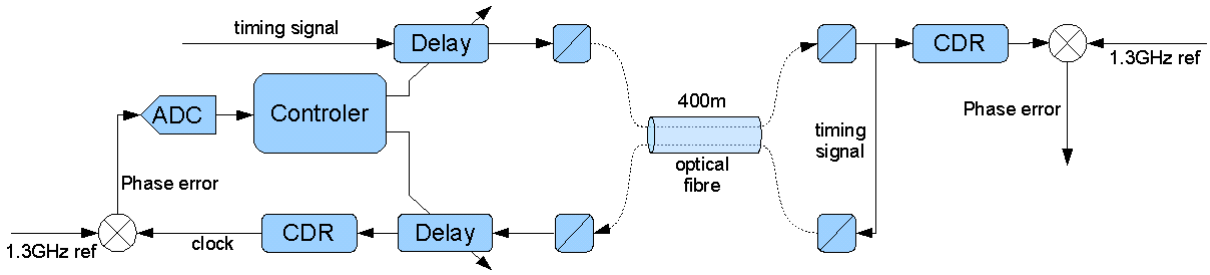
TBD

10 Operator Interface

TBD

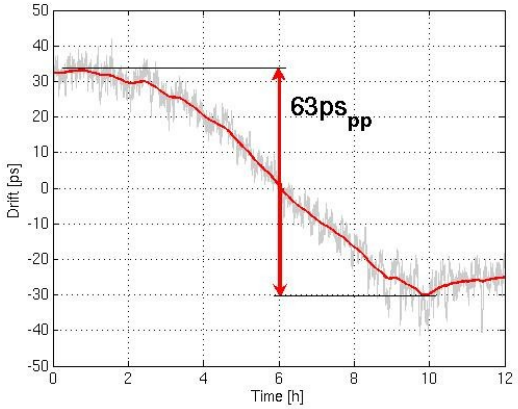
11 Performance Data

Preliminary results from measurements of the design principles are shown in the following figures. The measurement was done with a circuit shown in drawing 10.

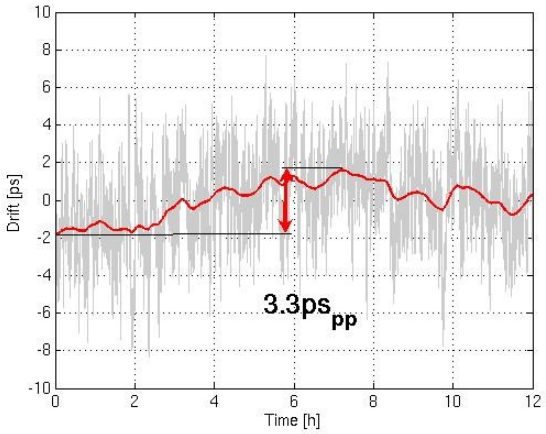


Drawing 10: Drawing of the used circuit to measure the performance

Without any compensation the drift caused by 8 degrees of temperature change is about 63 ps peak-peak as shown in picture .



Drawing 11: Uncompensated temperature drift caused by 8 degrees temperature change



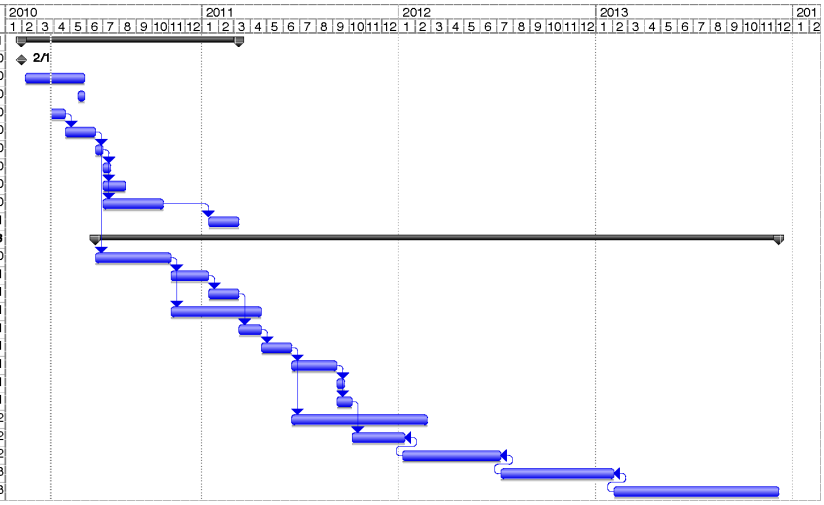
Drawing 12: Results with drift compensation (preliminary)

After compensation with the prototype the drift was reduced to 3.3ps peak-peak as shown in figure 12.

12 Milestones

The milestones are very PRELIMINARY!! - just a first guess.

ID	Task Name	Duration	Finish
1	**Single size AMC Timing rec/trans**	**289 days?**	**3/10/2011**
2	6 units prototypes	0 days	2/1/2010
3	basic FPGA controls, PCIe interfac	80 days	5/28/2010
4	FLASH adapter (events from old s	10 days?	5/28/2010
5	single AMC receiver/transmitter co	20 days?	4/22/2010
6	single AMC production	40 days?	6/17/2010
7	AMC function tests	10 days?	7/1/2010
8	installation in FLASH	10 days?	7/15/2010
9	UNIX driver,DOOCS server	30 days?	8/12/2010
10	drift compensation and full feature	80 days?	10/21/2010
11	series production	40 days?	3/10/2011
12	**double size AMC Timing trans/rec**	**906 days?**	**12/6/2013**
13	design	100 days?	11/4/2010
14	PCB layout	50 days?	1/13/2011
15	production	40 days?	3/10/2011
16	software development	120 days?	4/21/2011
17	test	30 days?	4/21/2011
20	design corrections	40 days?	6/16/2011
21	production of 2. prototype	60 days?	9/8/2011
22	installation in projects	10 days?	9/22/2011
23	tests	20 days?	10/6/2011
24	final software	180 days?	2/23/2012
25	time for corrections	70 days?	1/12/2012
26	series production purchase proces	130 days?	7/9/2012
27	series production + tests	150 days	2/4/2013
28	installation in XFEL	220 days	12/6/2013



Drawing 13: Possible project plan PRELIMINARY!!!

Task	Date
20 single size AMC modules produced and tested	01.07.10
Basic software for first prototype	01.07.10
Software with ps fiber drift compensation	21.10.10
Double size AMC (sender/ receiver), prototype ready and tested	21.04.11
Software for double size AMC ready	21.04.11
Production process start for XFEL timing modules	12.01.12
Series production finished, all timings are ready for installation in XFEL	04.02.13

Table 7: Milestones derived from the preliminary project plan