

XFEL Timing System Specifications

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Table of Contents

1	Introduction	2
2	Applications	3
2.1	XFEL	3
2.2	FLASH and FLASH2	4
2.3	REGAE	5
3	Principle of Operation	6
4	Bunch Pattern Table	10
5	Timing Transmitter	11
5.1	The Protocol	13
6	Timing Receiver / Transmitter – Double Size AMC (x2timer)	16
6.1	Timing Receiver	16
6.2	Timing Receiver RTM	19
6.3	Timing Transmitter	19
7	Timing Receiver Prototype (x1timer)	20
8	Events in XFEL	21
8.1	Requirements for the Phase Relations	24
9	Trigger and Clock Channel Capabilities	24
9.1	Calculation of the Timing Relations	25
10	Hardware Interfaces	27
10.1	Front Panel IO	27
10.2	Timing Distribution within a μ TCA Crate	27
11	Software and FPGA Interface	30
11.1	Configuration	30
11.2	Fast Data Link in MicroTCA	30
11.3	Slow data link	32
11.4	Fast data link	32
12	Subsystem Connections	32
12.1	Laser	32
12.2	RF (Modulator/Klystron)	33
12.3	LLRF	33
12.4	BPM	33
12.5	Toroid, BLM, Halo	33
12.6	Wire Scanner	34
12.7	TDS	34
12.8	Kickers	35
12.9	Experiments and Photon Diagnostics	35
13	Measurement of the Total Delay Time (Transmitter \rightarrow Receiver)	36
14	Timing System DOOCS Server	36
15	Operator Interface	36
16	Performance Data	36
	Glossary	37

1 Introduction

The initial layout of the European XFEL provides 5 beamlines for user experiments. In a future extension a second injector will be added to the XFEL. It is the task of the timing system to coordinate the complex operation of all subsystems by distributing the required clocks, triggers and bunch information:

- The repetition rate of the RF pulse (macro pulse) will be 10 Hz (max. 25 Hz).
- The XFEL can deliver multiple bunch spacings within a macro pulse for selected beamlines (this we call a bunch pattern). The expected bunch pattern must be provided to all timing receivers.
- The desired charge range for all bunches should be provided.
- Lasers and kickers have to be controlled in-sync to provide the bunch pattern
- RF, diagnostic and protection devices need to receive the bunch pattern before the beam is accelerated.
- All timing and bunch pattern information must be distributed very reliable. Therefore the timing system provides a hardware-based communication, that can not be disrupted by e.g. network congestion.
- All timing receivers must have a fixed phase relation of all frequencies to each other. This relation must be recovered after any interruption within a few hundred milliseconds.
- Triggers and clocks must have a fixed relation to the bunches and a low enough jitter to be able to identify an individual single 1.3 GHz wave.
- The macro pulse triggers must be in-sync with the 50 Hz mains frequency.
- The traveling-time variation due to temperature changes must be compensated for.
- The traveling time from a transmitter to timing receivers should be measured and compensated to allow a setup of the timings before bunches can be used as a reference. The accuracy of this measurement should be better than a microsecond.
- The timing system should distribute an absolute time with microsecond resolution e.g. to time stamp interlocks and other events.
- The timing system has to distribute a unique macro pulse number for each shot (32 bit integer).

An introduction to the XFEL timing concept can be found under:

http://flash.desy.de/sites/site_vuvfel/content/e403/e1644/e1136/e1137/infoboxContent1838/TESLA-2006-12.pdf

This timing system will be implemented in MicroTCA. A prototype version as a single size AMC module is available. It is named x1timer. A double size AMC module, called x2timer, is under construction. This x2timer will be the final version used in XFEL and FLASH.

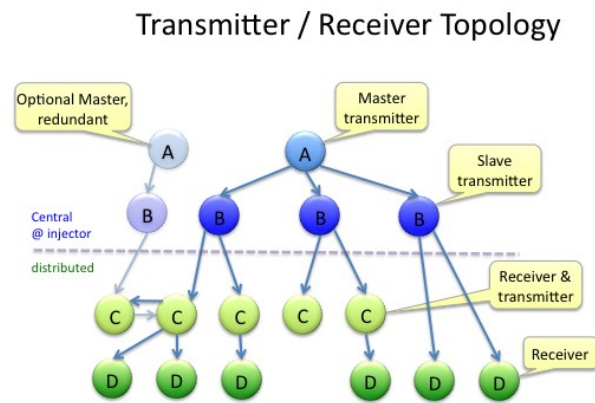
2 Applications

2.1 XFEL

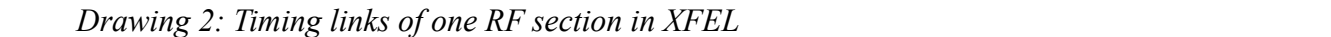
The XFEL timing will be distributed from a central place in the injector building close to the Master Oscillator (MO). It will receive a stable 1.3 GHz clock from the MO (Master Oscillator). A further input will be a 50 Hz signal from the mains.

One master timing module is programmed to deliver all information to the other modules in a hierarchical topology Drawing 1.

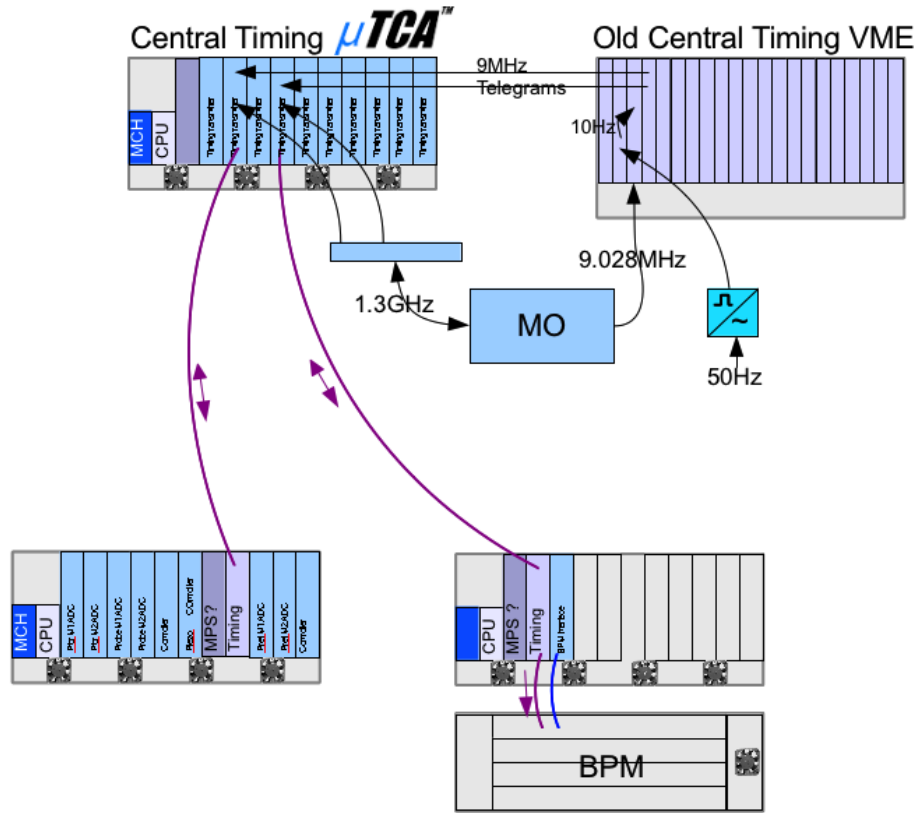
For the receivers a redundant option is foreseen. Two timing receivers can receive 1.3 GHz telegrams from the central station via separate fiber optic cables. A link between the two receiver AMCs (the left most C-modules in the drawing) is used as an update channel. If one link to the central timing transmitter fails the receiver detects this and switches to the update link from the second receiver. This update link is bidirectional and directly transmits the incoming telegrams to the AMC with the broken master connection. A redundant master transmitter can be added in a second MicroTCA crate close to the master oscillator.



Drawing 1: Four level topology of transmitter and receiver modules



The FLASH timing system is based on an event distribution system originally designed by



Drawing 3: Communication of the old FLASH timing with the new XFEL timing to be operated in FLASH

To be able to run the old timing and the new XFEL timing system in parallel at FLASH, it is required to receive the 9 MHz telegrams from the old timing and extract the events from it as the basis for the events distributed in the new timing. In a second stage the new timing system will act as the master and the old system will receive triggers from the new MicroTCA timing.

New electronics for FLASH2 will be equipped with the new timing system only. Since FLASH2 will have a similar bunch distribution as XFEL, with two or more users of a bunch train, the new timing system is required. Furthermore, it is planned to use the same μ TCA based hardware of XFEL for FLASH, too.

2.3 REGAE

REGAE operates at 3 GHz and the timing requirements are quite different compared to XFEL and FLASH. A 1 GHz clock from the master oscillator is envisioned.

Preliminary requirements of the REGAE timing are:

- 1 trigger for the EMCCD camera as a gate for the image amplifier
- 1 trigger for two JAI cameras

- 1 trigger for the modulator
- 1 gate for the RF-gate
- 1 gate for the pulse power amplifier
- 1 trigger on the backplane for the LLRF ADC
- 1 reset for the LLRF (required later with a new LO, e.g. with x2timer)
- 1 trigger for lasers (later)
- 1 trigger for dark current monitor (ADC in LLRF crate, via backplane)

A resolution of 10 ns for the adjustment of triggers/gates is sufficient. The rep-rate should be set-able in a range of 1 to 50 Hz. Several triggers can be delivered by one output of the timing system and distributed with a TTL-fan-out and different cable length to the same type of camera. In a first implementation only one x1timer is required.

REGAE is included in this specification since it is a testbed for the hardware. It also allows to gain experience in defining the specs for the XFEL timing in a more general way. This will allow enlarging the scope of the XFEL timing system in additional projects.

3 Principle of Operation

The XFEL timing system will have many receiver modules and several transmitters. A primary transmitter receives 1.3 GHz from the master oscillator and the line frequency. It holds a programmable table with the complete timing sequence. The 1.3 GHz is used as the clock frequency to send 8b/10b encoded data to further timing transmitters. These transmitters send the data stream to timing receivers. This data is sent back to the transmitter as a loopback to compensate drifts of the fiber optical links within the transmitter. A transmitter keeps the delay time over the fiber link constant by compensating effective fiber length, affected by temperature variations, in adjustable delay modules. See Drawing 5 and Drawing 28.

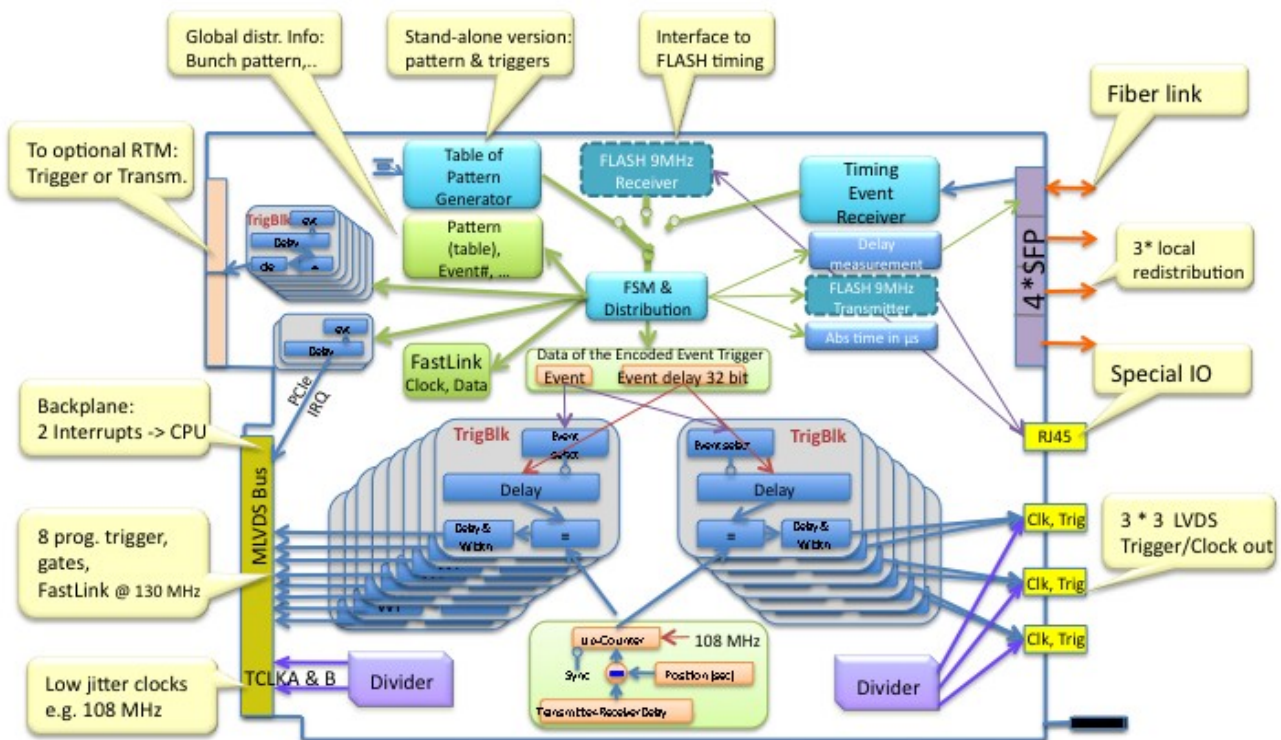
On the receiver side the stable 1.3 GHz clock is extracted from the data stream along with the data. The clock is fed into precision dividers. A FPGA receives the data to extract trigger, bunch pattern, and other information. The outputs of a timing receiver are:

- Triggers on a local MicroTCA backplane (to start e.g. ADCs) and on the front panel. They are generated by the timing FPGA and controlled by the control system.
- Clocks on the local MicroTCA backplane and on the front panel. These clocks are generated by dedicated dividers for best performance and to avoid additional drift and jitter induced by a FPGA. The dividers are programable by the control system .
- Interrupts to the local CPU within the MicroTCA system, distributed by PCIe.
- Bunch patterns and other parameters available via PCIe. The local CPU has access to these parameters.
- A data stream together with a clock on the local MicroTCA backplane to transfer event numbers, bunch patterns and other information received by the timing receivers. This data is received by FPGAs in other diagnostic devices.
- Triggers and encoded data on fiber links on an optional Rear Transition Module.

A x1timer or x2timer AMC module can be used as a receiver or transmitter. Drawing 4 shows the main functional blocks. Some of these blocks are optional: “Table of Pattern Generator” is used in the main transmitter or in stand-alone applications only. The FLASH transmitter and receiver part is used to interface with the old FLASH timing system only. All the other blocks are common:

- The “timing and event receiver” decodes the incoming protocol (1.3 GHz) and controls the synchronization of the on-board dividers.
- “FSM & Distribution” delivers the extracted protocol data to the other blocks.
- “Pattern (table), MacroPulse number, ..” is a storage of the distributed information and provides the bunch pattern table with section permissions and requested charges per bunch as well as the unique macro-pulse number etc.
- “Data of the encoded event trigger” is a block that holds the event number and delay information for all trigger blocks.

Timing Main Functions

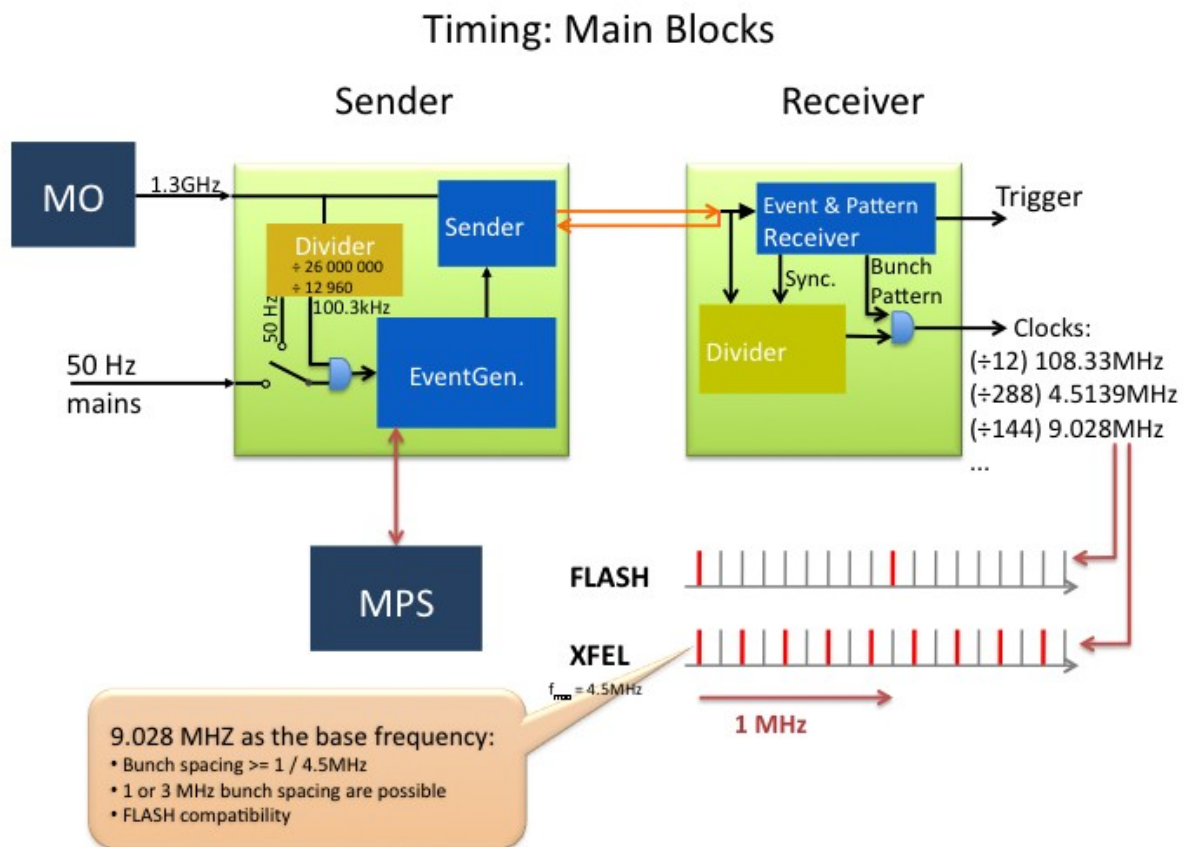


Drawing 4: Functions provided by the timing system on a double size AMC module.

- The “TrigBlk” receives selected events with delay times and generates triggers that are corrected by the absolute delay time between transmitter and receiver and the position in the machine. Trigger blocks are used for the front panel outputs, backplane triggers, interrupts to the CPU and an optional Rear Transition Module with further trigger outputs.
- Two different interrupts are selectable to be transferred by PCIe to the CPU.

- Stable, low jitter clocks TCLKA and TCLKB on the backplane and (radial distribution) and stable clocks on the front panel plugs.
- The “delay measurement” is used to help the timing transmitter calculating the cable delay time.

In a distributed system a main requirement is to have synchronized receivers. All clocks and triggers must have the same phase relation e.g. to the first bunch. This relation must be kept constant even after a global or local power failure. A special action of an operator should not be required if the power of a single crate of the distributed system was cycled. All timing and clock dividers must be resynchronized automatically. Therefore it is foreseen to transmit a synchronization event before every linac shot.



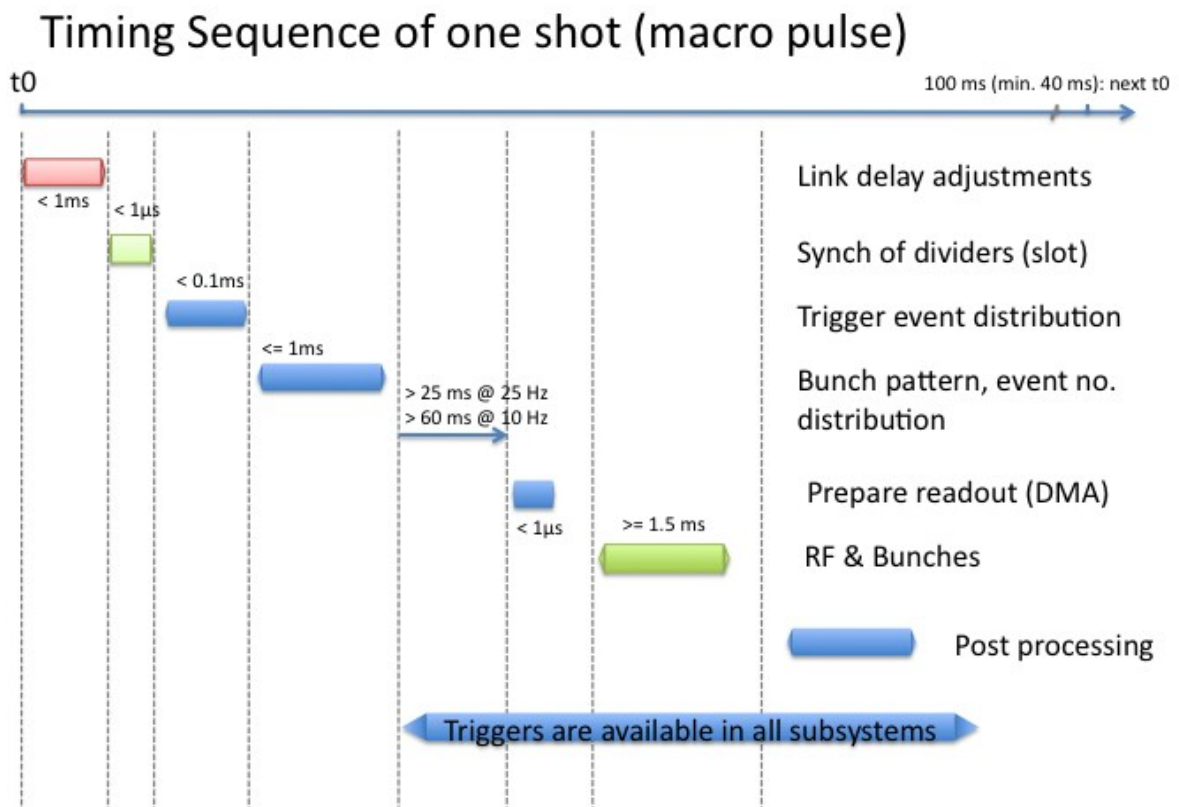
Drawing 5: Transmitter and receiver block diagram: the transmitter block implements the drift compensation of the fiber links

The XFEL will serve more than one experiment at the same time. A part of the bunch train will travel through different beamlines. And bunches might have different fillings/spacings even from shot-to-shot. It's the task of the timing system to provide the necessary information along the entire machine before each acceleration. Diagnostics, protection systems and feedbacks need this information in advance, e.g. a few ms before the first bunch arrives. This information is distributed as a table from the main timing transmitter to all slave transmitters and receivers.

In a more advanced operation mode subsequent shots can have different settings. They are

marked with shot-IDs. These shot-IDs are transmitted well in advance of the first bunch. One shot-ID is used for one set of parameters. This has of course strong limitations on the linac settings and some parameters in subsystems have to implement different parameters that are switched from shot-to-shot. Running in such a mode is not meant to be used in the first days of operation. It's a feature to be used when standard operation has been established!

The general sequence of information distributed by the timing system is repeated for every macro pulse (e.g. with 10 Hz). A trigger of the zero-crossing of the 50 Hz mains is synchronized with the lowest possible frequency in the system. This frequency was selected to be 100 kHz ($1.3 \text{ GHz} / 12960$). This synchronized 50 Hz is divided by typically 5 and the signal t_0 is generated (Drawing 6). The first millisecond after t_0 is reserved for the timing link length compensation. Then the master timing transmitter sends a synchronization command. This is used to reset all receiver dividers. During normal operation this reset is in-sync and therefore no change of the clocks derived from the dividers are effected. In case of an interruption of the normal operation due to disconnected cables or switched power a receiver will be resynchronized and clock phases will be reestablished.



Drawing 6: Timing sequence of a macro-pulse

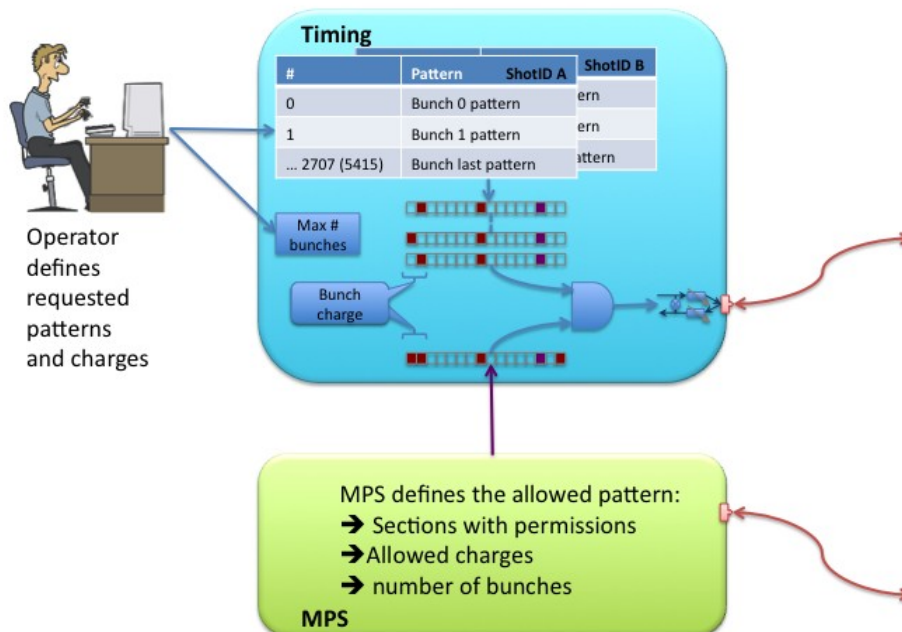
After the sync-command the trigger information is distributed (trigger commands followed by event number and time data). This is followed by a long table of bunch pattern information for the current macro pulse. Now all data is available in the receivers and is distributed to the local FPGAs within a crate. Depending on the subsystem the following $> 25 \text{ ms}$ are used to prepare for the acceleration of bunches. During this period triggers will be generated by the timing receivers according to the programmed delays. Delays are a combination of the global delay as send by the master timing unit and local delays to compensate the position in the linac, the differences of cable length and differences of the startup time of components.

4 Bunch Pattern Table

The final format of the bunch pattern table should be defined soon in a separate paper. The pattern definition in this chapter is preliminary – just to show the principal implementation in the timing system!

The content of the table is prepared by an operator. It defines a goal. The Machine Protection System (MPS) can restrict the operation of beamlines, the number of bunches and the allowed charges.

Bunch Pattern Generation in Timing and MPS

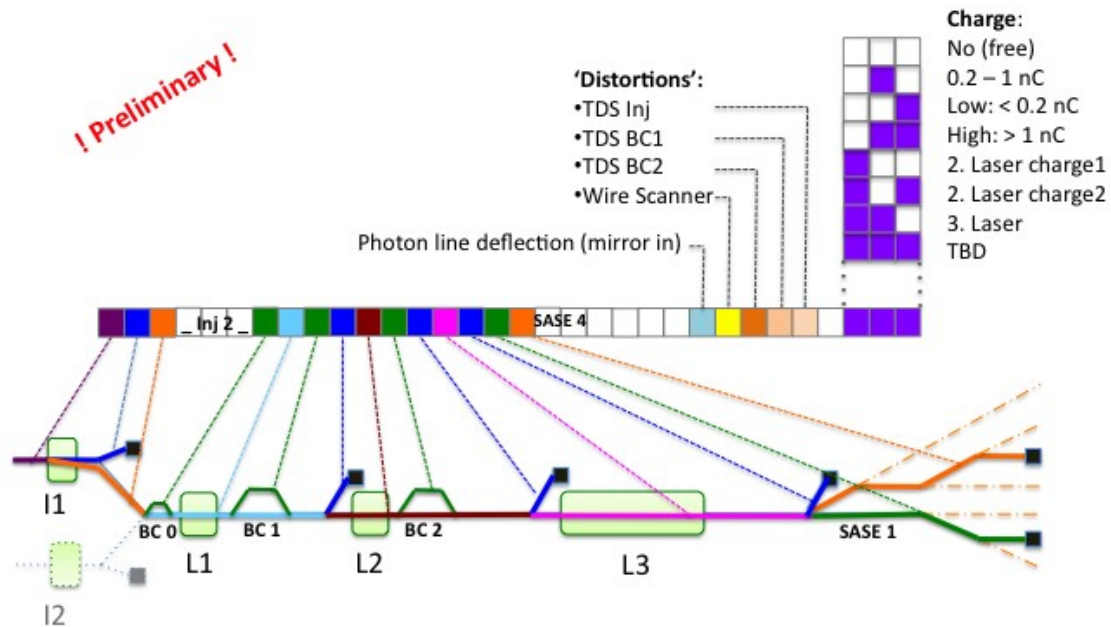


Drawing 7: An operator creates a list with requested targets and charges of bunches in the timing system (blue box). The MPS permits machine sections, charges, and number of bunches on a shot-to-shot basis.

A fast hardware connection from the MPS to the master timing module is used to “gate” the permitted linac sections and to restrict the max. number of bunches. A simple logical *AND* of the requested pattern with the permitted pattern from the MPS is used to control the bunches. This is based on a direct hardware link between the MPS and timing firmware and does not depend on any control system software.

To provide the highest flexibility of bunch repetition rates and compatibility with FLASH the bunch pattern should be based on a 9 MHz structure (Drawing 5). Since XFEL defines a maximum of 4.5 MHz bunch rate at least every second entry has to be marked as “no bunch”. But, this scheme allows 3 and 1 MHz bunch frequencies for example. A 4.5 MHz raster would not allow these often used FLASH frequencies. This requires a table with 5400 entries for a maximum of 2700 bunches in XFEL. The table length for FLASH is 7200. One table entry is a 32 bit word that defines the bunch charge, the planned path of a single bunch up to a beam dump, and if the bunch might be distorted by e.g. a Transverse Deflecting diagnostic station (Drawing 8).

32 bit Bunch Pattern Definition



January 6, 2012

Kay Rehlich, !!!PRELIMINARY!!!

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Drawing 8: 32 bit word defining the properties of a single bunch.

One bunch pattern table defines the paths of all bunches for one macro pulse. It is marked with a ShotID, let's say A. The next macro pulse might be defined by a different pattern table and with a different ShotID, e.g. B. As an example, the accelerator might be driven by 9 shots of type A followed by a single shot of type B. Some slow feedbacks or learning algorithms require this ShotID to be able to optimize shots with the two different types separately. Therefore the timing system sends before each shot (macro pulse) a complete table and a ShotID as a single number.

Running with different ShotIDs is a complicated procedure since it requires different settings of certain parameters in the subsystems. It also complicates learning procedures. The timing system hardware and the specifications include this feature. During the start-up of the XFEL a single pattern should be used only. After stable operations of FLASH 2 or XFEL have been established one could activate this flexible feature in subsystems.

5 Timing Transmitter

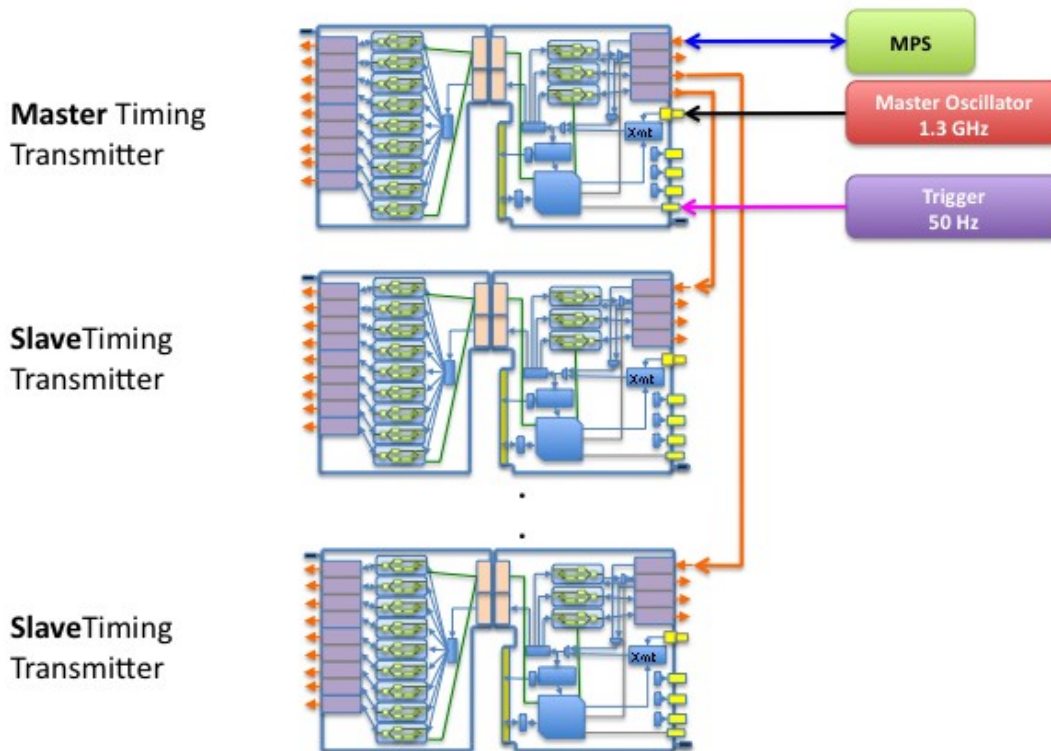
The central timing transmitter is located close to the master RF oscillator. In case of XFEL it is located in the injector building, at FLASH in the injector hutch. A single transmitter AMC is programmed by the control system. It stores the information of all triggers and requested bunch patterns in one table per shot-ID. This table is transmitted with every trigger (e.g. 10 Hz) to the slave transmitters (Drawing 9). A slave is mainly a fan-out and sends the received information to all its clients. Every output of a transmitter has a delay compensation to keep the propagation

time to the receivers constant.

Central timing transmitter inputs:

- 1.3 GHz from master RF oscillator (level to be defined)
- 50 Hz from the mains, filtered, level: LVDS
- Limits from the MPS (Machine Protection System)

x2timer with RTM: Central Transmitter μ TCA Crate



Drawing 9: One master transmitter can drive up to 12 slave transmitters

Transmitter outputs:

- 12 fiber optic (SFP) outputs with telegrams, bidirectional (3 on front AMC and 9 outputs on the RTM) (see Drawing 9).
- Optional encoded clock to drive the old FLASH timing.

The link between a central station and receiver boards is accomplished by a bidirectional fiber optic cable. The return line of this connection is used to compensate drifts and to measure the round trip time. On this link a stable clock is modulated with encoded 8b/10b data. This combined clock and data is decoded in the receiver where clock and data will be separated.

All timing transmitters are placed close to the master RF oscillator in the injector building or injector hutch in case of FLASH. The timing is programmed in the master transmitter. This master connects to several slave transmitters. Each transmitter provides 12 links to slaves or

receivers. And a receiver can retransmit the signals to up to 3 further receivers. All output links are drift-compensated. Furthermore, a local system can be setup in a redundant network. When the main receiving link breaks, signals can be rerouted via a redundant fiber (Drawing 10). Switching to a redundant link should occur very seldom. Therefore it is not foreseen to automatically compensate the phase differences after switching to the second link. This requires some manual adjustments only in a very few effected systems.

The topology in Drawing 9 shows one timing master module that sends a 1.3 GHz encoded data stream to up to 12 slave transmitters. Each slave transmitter has 12 fiber optical outputs to drive 12 timing receivers. One central MicroTCA transmitter crate can drive up to 120 receivers. A fully redundant version would need two master timing crates and one fiber link from each crate to the receivers. A receiver module can redistribute the timing signal to further local receivers.

Via PCIe a CPU can communicate with all local timing modules. All parameters that need to be changed by an operator or subsystem expert, are available on this interface. This is the interface to the DOOCS control system.

5.1 The Protocol

Telegrams from a timing transmitter to a receiver are based on a stable 1.3 GHz clock with encoded data. Standard 8b/10b coding is used on fiber links. The encoded data contains commands, parameters and additional protocol data like length or CRCs. On a timing receiver the incoming byte-rate is 130 MHz. The same telegrams are redistributed on the optical output links of the receiver. With a bit-rate of 130 MHz the protocol information is also redistributed within the local MicroTCA crate.

A telegram starts with a START comma character (these are special control characters reserved for non data functions) followed by a LENGTH and a command (CMD), followed by optional data bytes and ends with correction bytes:

<START><LENGTH><CMD><DataByte-1><DataByte-n><CRC>

To be able to distribute the incoming 1.3 GHz bit-rate on a slower 130 MHz clock data buffering on the timing receiver will be provided.

Character	Name	Function	8b Data	10b Data
D21.5	FILL	Idle filler	001 11001	101010 1010
K28.5	START	Start of packet	101 11100	001111 1010
K28.0	END	End of packet, not used	000 11100	001111 0100
K28.7	SYNC	Synchronization of all dividers	111 11100	001111 1000

Table 1: Special characters used in the protocol.

The trigger command “Event” is followed by a event number (one byte) and a 32 bit word T with timing information. T is the time delay started from SYNC (K28.7) in units of the receiver counting clock. For XFEL and FLASH this clock is $1.3 \text{ GHz} / 12 = 108.33 \text{ MHz}$. On the receiver SYNC sets a counter to the measured receiver-transmitter delay plus a programmable constant that corrects an location-dependent offset. This offset takes into account the time an electron travels from the Gun to the position of the timing receiver.

The commands LinkDelay, RequestID and ResponseID are used internally and are subject to

be changed.

Name	Function	CMD	Data byte, Length (L)
Filler	used for phase comparison to compensate drifts (D10.2)	D21 . 5	-
Sync	Synchronization of the receivers, before each macro pulse	K28 . 7	-
Probe	Measure total link delay	K28 . 4	-
Event	Trigger event	0x02	L=6
	Event number (0..255)		EEEEEEEE
	Relative time to Sync (high byte)		TTTTTTTT
	Relative time to Sync		TTTTTTTT
	Relative time to Sync		TTTTTTTT
	Relative time to Sync (low byte)		TTTTTTTT
Mode	Linac operation mode, see Table 3	0x03	L=2
	Mode (0..255)		MMMMMMMM
MacroPulseNumber	Unique number for each macro pulse	0x04	L=5
	64 bit integer with unique event number		8 * byte
ShotID	An ID of the sequence/cycle number of the actual macro pulse	0x08	L=2
	ShotID number in the range of 0..3 (max 255)		SSSSSSSS
Table	Byte array to describe the e.g. bunch pattern	0x05	L=3 + N
	Table identifier (e.g. bunch pattern) (0..255)		PPPPPPPP
	Segment number (0..255)		SSSSSSSS
	Byte array with fill pattern, N=0..255		N * byte
Time	Abs. time	0x06	L=9
	Time from master transmitter, 64 bit, micro second resolution		8 * byte
MPS	Interlock from MPS was detected, OPTIONAL, units and relation TBD	0x07	L=5
	Time of interlock event (high byte)		TTTTTTTT
	Time of interlock event		TTTTTTTT
	Time of interlock event		TTTTTTTT
	Time of interlock event (low byte)		TTTTTTTT
ImmediateTrigger	Trigger, executed once	0x0A	L=2
	Trigger number (0..255)		GGGGGGGG
LinkDelay	Delay time from transmitter to receiver ?????	0x0B	L=5
	ID		4 * byte
RequestID	Request receiver ID (master requests ID from first receiver)	0x0C	L=5
	ID of master		4 * byte
ResponseID	Response of the RequestID by the receiver	0x0D	L=5
	ID of receiver		4 * byte
SetFlag	Marks bits in receiver registers for optional functions	0x10	
	32 bit mask		4 * byte

Table 2: Data telegrams, protocol overview

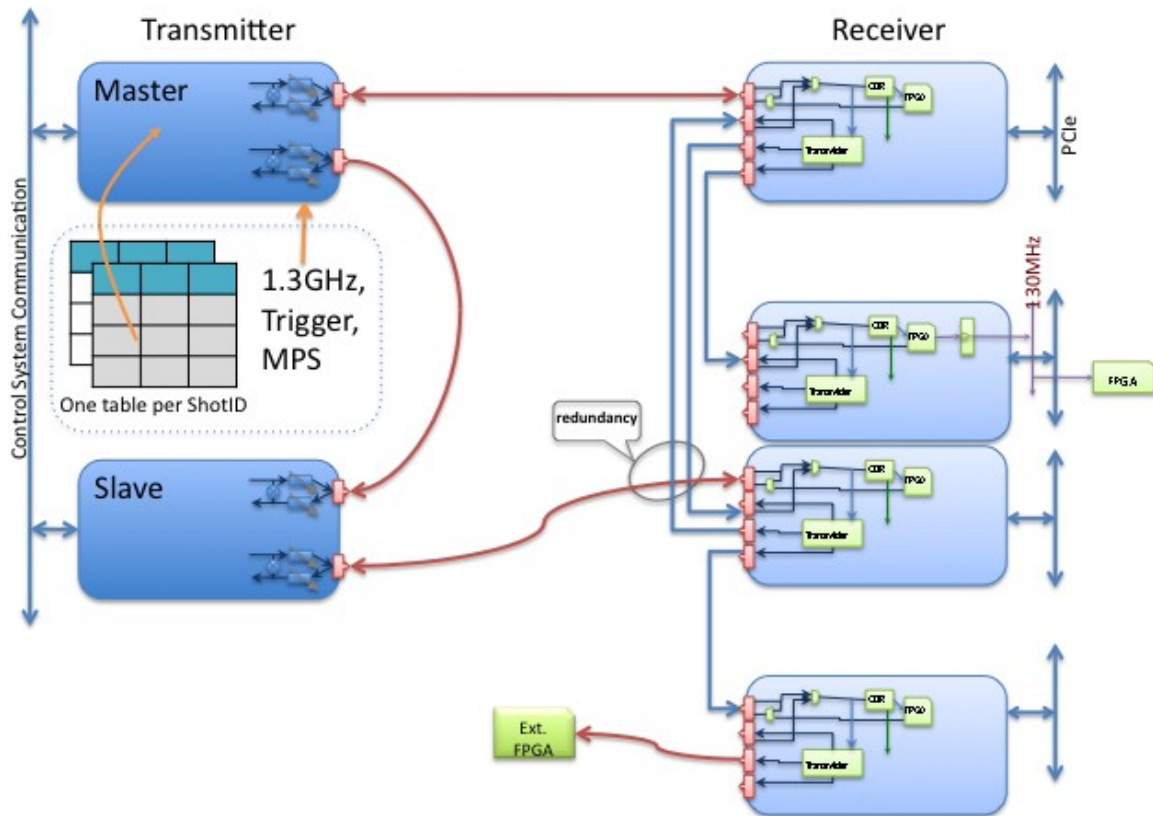
Bit		Description
1	0	No beam
0	1	Single bunch mode
1	0	Short bunch mode (≤ 30 bunches allowed)
1	1	Long bunch mode (all bunches allowed)

Table 3: Linac operation mode as defined by the MPS

Part A	Part B	Part C	Part D, Local part
0...255	0...255	0...255	0...255

Table 4: Each timing unit has an individual ID to be used in addressing specific modules.

Transmitter <-> Receiver Connections



Drawing 10: Left side shows the timing transmitters at the injector building, on the right side are local receivers with a redundant links.

6 *Timing Receiver / Transmitter – Double Size AMC (x2timer)*

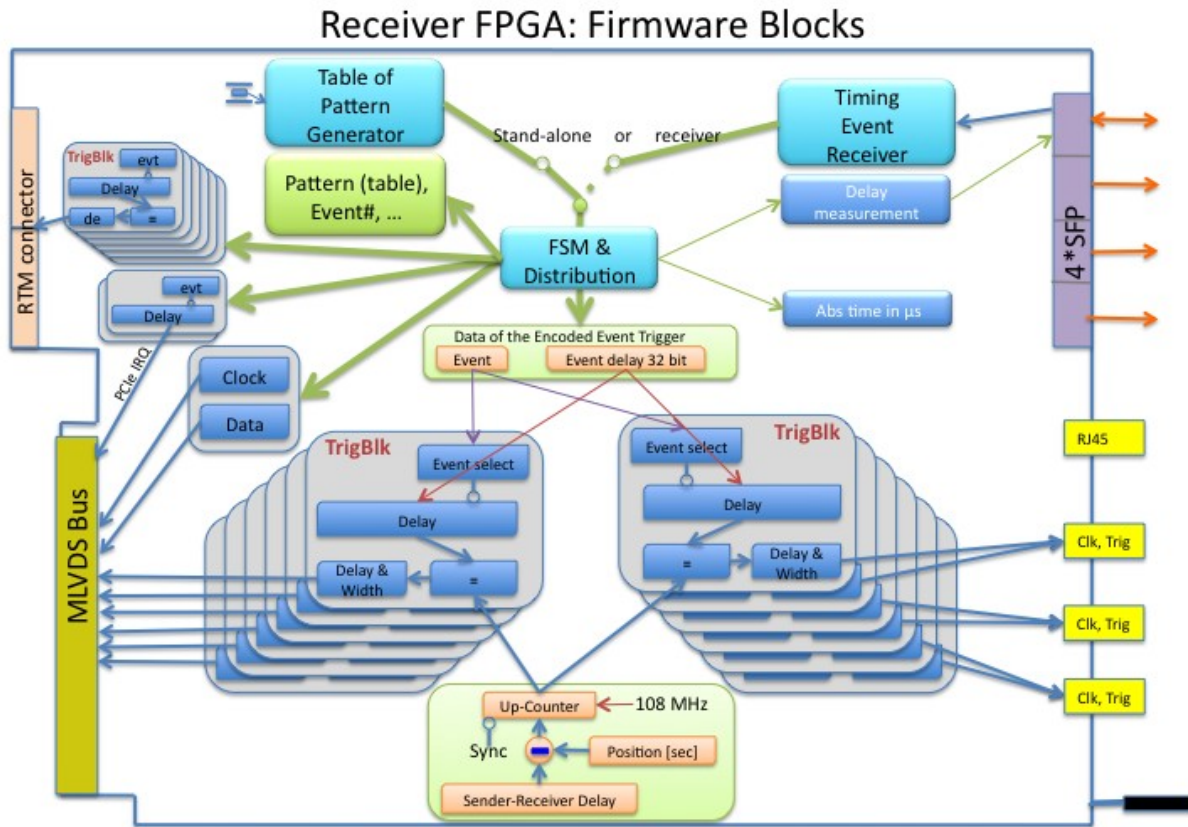
6.1 Timing Receiver

Timing receiver functions:

- Receives a 1.3 GHz clock and events on fiber optics
- Loop-back of the 1.3 GHz clock to the transmitter for link drift compensation
- Decodes events
- Generates programmable timing signals out of the events ($\sim 1\text{ ns} \dots 100\text{ ms}$)
- Delay, output pulse width, and fine delay are individually programmable
- Generates programmable clocks (1.3 GHz, 108 MHz, 216.7 MHz, see Drawing 12)
- Generates two programmable local interrupts within a crate on PCIe
- Provides data registers for macro pulse type and event number
- Holds a table with bunch pattern information of the current macro pulse
- Has a readable counter for precise time measurements, set by an abs. time event, the resolution is $1\mu\text{s}$
- Receives time delay of the link from transmitter to correct delays
- Provides a transmitter of event broadcasts on Ethernet (implemented in software, timing server)

Inputs:

- SFP plug with fiber optic receiver for incoming telegrams
- RJ45 connector for future extensions (LVDS signals to FPGA)



Outputs.

- on AMC plug: TCLKA , TCLKB from precision clock divider (see chapter 10.2)
- on AMC plug as M-LVDS on ports 17 to 20: 8 clocks, gates, data links or triggers (see chapter 10.2)
- on front RJ45 plugs, level: CML

All outputs are equipped with a multiplexer to select the signal source: trigger, clock, bunch clock, gate, synchronization, fast data link (11.2) or slow data link (11.3). Further outputs can be implemented on RTMs. The precision clocks TCLKA and TCLKB are provided by a programmable divider and are not passed through a FPGA. Triggers and gates are generated by a FPGA and are described in chapter 9.

Mechanics:

AMC board, double mid size form factor according to MTCA.4.

XFEL Timing System Specs, Version 0.9

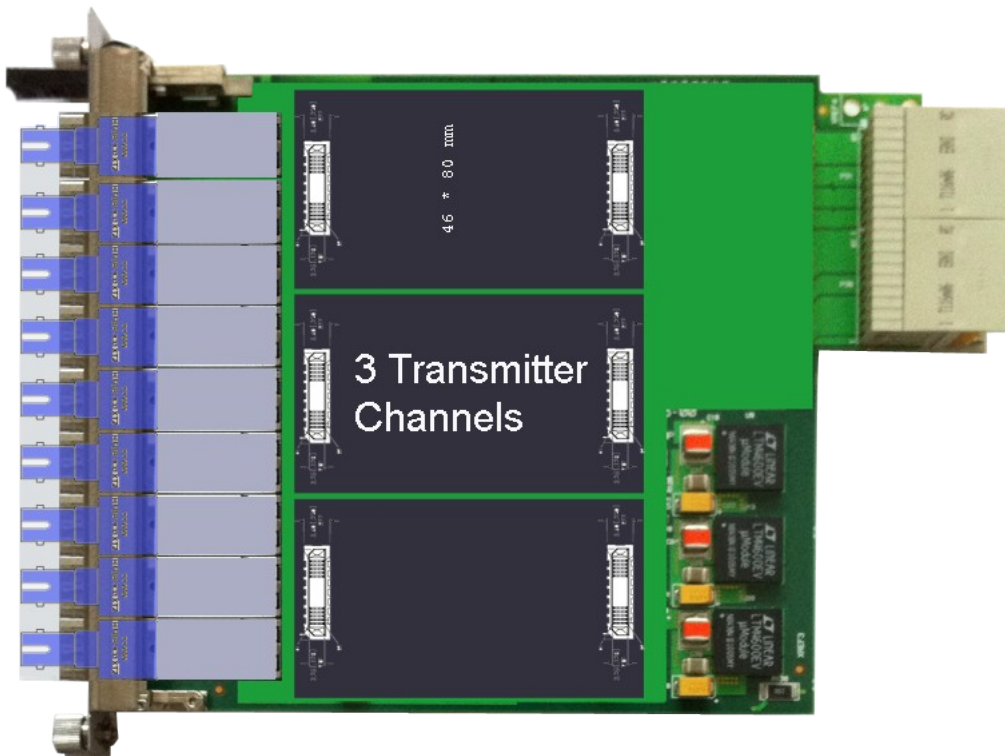
Divider	f	Divider	f	Divider	f	Divider	f	Divider	f	Divider	f	Divider	f	Divider	f
1	1300,000	64	20.31	128	10.156	192	6.771	256	5.078	320	4.063	384	3.385	448	2.902
2	650,000	66	19.70	130	10.000	194	6.701	258	5.039	322	4.037	386	3.368	450	2.889
4	325,000	68	19.12	132	9.848	196	6.633	260	5.000	324	4.012	388	3.351	452	2.876
6	216,667	70	18.57	134	9.701	198	6.566	262	4.962	326	3.988	390	3.333	454	2.863
8	162,500	72	18.06	136	9.559	200	6.500	264	4.924	328	3.963	392	3.316	456	2.851
10	130,000	74	17.57	138	9.420	202	6.436	266	4.887	330	3.939	394	3.299	458	2.838
12	108,333	76	17.11	140	9.286	204	6.373	268	4.851	332	3.916	396	3.283	460	2.826
14	92,857	78	16.67	142	9.155	206	6.311	270	4.815	334	3.892	398	3.266	462	2.814
16	81,250	80	16.25	144	9.028	208	6.250	272	4.779	336	3.869	400	3.250	464	2.802
18	72,222	82	15.85	146	8.904	210	6.190	274	4.745	338	3.846	402	3.234	466	2.790
20	65,000	84	15.48	148	8.784	212	6.132	276	4.710	340	3.824	404	3.218	468	2.778
22	59,091	86	15.12	150	8.667	214	6.075	278	4.676	342	3.801	406	3.202	470	2.766
24	54,167	88	14.77	152	8.553	216	6.019	280	4.643	344	3.779	408	3.186	472	2.754
26	50,000	90	14.44	154	8.442	218	5.963	282	4.610	346	3.757	410	3.171	474	2.743
28	46,429	92	14.13	156	8.333	220	5.909	284	4.577	348	3.736	412	3.155	476	2.731
30	43,333	94	13.83	158	8.228	222	5.856	286	4.545	350	3.714	414	3.140	478	2.720
32	40,625	96	13.54	160	8.125	224	5.804	288	4.514	352	3.693	416	3.125	480	2.708
34	38,235	98	13.27	162	8.025	226	5.752	290	4.483	354	3.672	418	3.110	482	2.697
36	36,111	100	13.00	164	7.927	228	5.702	292	4.452	356	3.652	420	3.095	484	2.686
38	34,211	102	12.75	166	7.831	230	5.652	294	4.422	358	3.631	422	3.081	486	2.675
40	32,500	104	12.50	168	7.738	232	5.603	296	4.392	360	3.611	424	3.066	488	2.664
42	30,952	106	12.26	170	7.647	234	5.556	298	4.362	362	3.591	426	3.052	490	2.653
44	29,545	108	12.04	172	7.558	236	5.508	300	4.333	364	3.571	428	3.037	492	2.642
46	28,261	110	11.82	174	7.471	238	5.462	302	4.305	366	3.552	430	3.023	494	2.632
48	27,083	112	11.61	176	7.386	240	5.417	304	4.276	368	3.533	432	3.009	496	2.621
50	26,000	114	11.40	178	7.303	242	5.372	306	4.248	370	3.514	434	2.995	498	2.610
52	25,000	116	11.21	180	7.222	244	5.328	308	4.221	372	3.495	436	2.982	500	2.600
54	24,074	118	11.02	182	7.143	246	5.285	310	4.194	374	3.476	438	2.968	502	2.590
56	23,214	120	10.83	184	7.065	248	5.242	312	4.167	376	3.457	440	2.955	504	2.579
58	22,414	122	10.66	186	6.989	250	5.200	314	4.140	378	3.439	442	2.941	506	2.569
60	21,667	124	10.48	188	6.915	252	5.159	316	4.114	380	3.421	444	2.928	508	2.559
62	20,968	126	10.32	190	6.842	254	5.118	318	4.088	382	3.403	446	2.915	510	2.549

Drawing 12: Possible divider settings and resulting frequencies in MHz. Often used frequencies are marked yellow. Cells marked grey indicate frequencies that are not multiple of 100 kHz and will have a phase jump every shot.

6.2 Timing Receiver RTM

Some subsystems require several timing signals from one timing receiver. So far two versions of Rear Transition Modules (RTM) are foreseen:

- Modulator triggers (Drawing 14): can drive 4 modulator stations with one trigger output and one event number output as a coded telegram at 115 kbaud (UART).
- BPM clocks and triggers: can drive 4 (up to 8) MBUs with BPMs by fiber optical links, 1.3 GHz clock and data protocol.



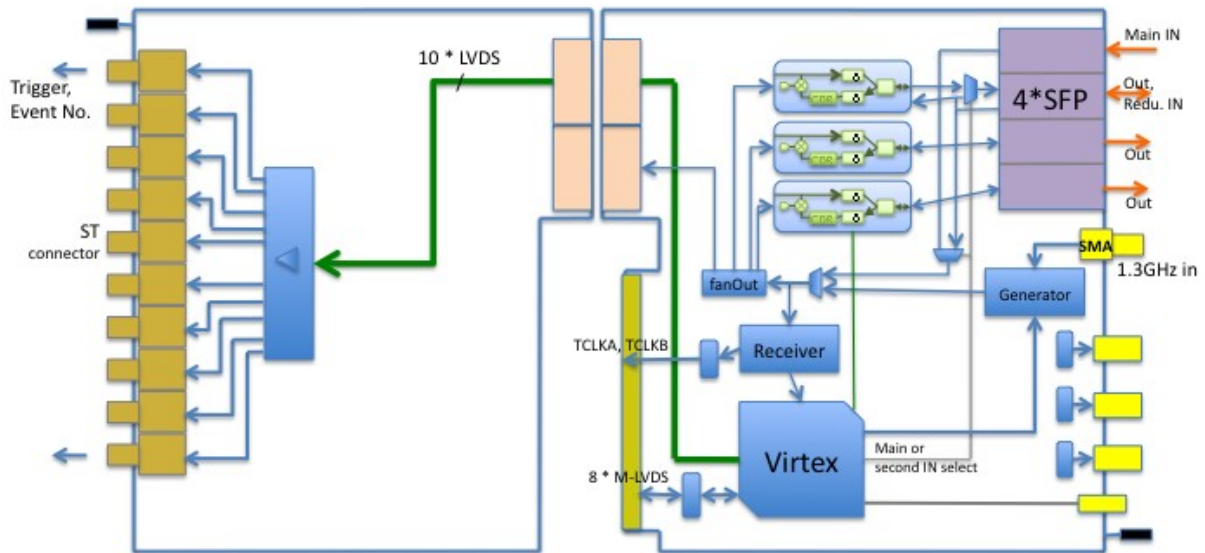
Drawing 13: Hardware layout of the RTM: can be equipped with simple ST fiber optic drivers or SFP modules for higher frequencies. Has space for three optional transmitter mezzanines with up to 3 channels each.

Further RTMs can be manufactured as an adapter to special signal levels or protocol requirements if needed. RTMs will be always equipped with a standard MTCA.4 management. This allows hot-swap of the RTM and compatibility checks before 12 Volt are asserted to the RTM.

6.3 Timing Transmitter

The timing transmitter will be implemented on the same hardware as the receiver. Transmitter channels are on separate mezzanines and can be added as required to convert a receiver into a master or slave transmitter or simply to retransmit timings. The FPGA code on the master timing transmitter has to be different, all other slave transmitters and receivers get the same firmware.

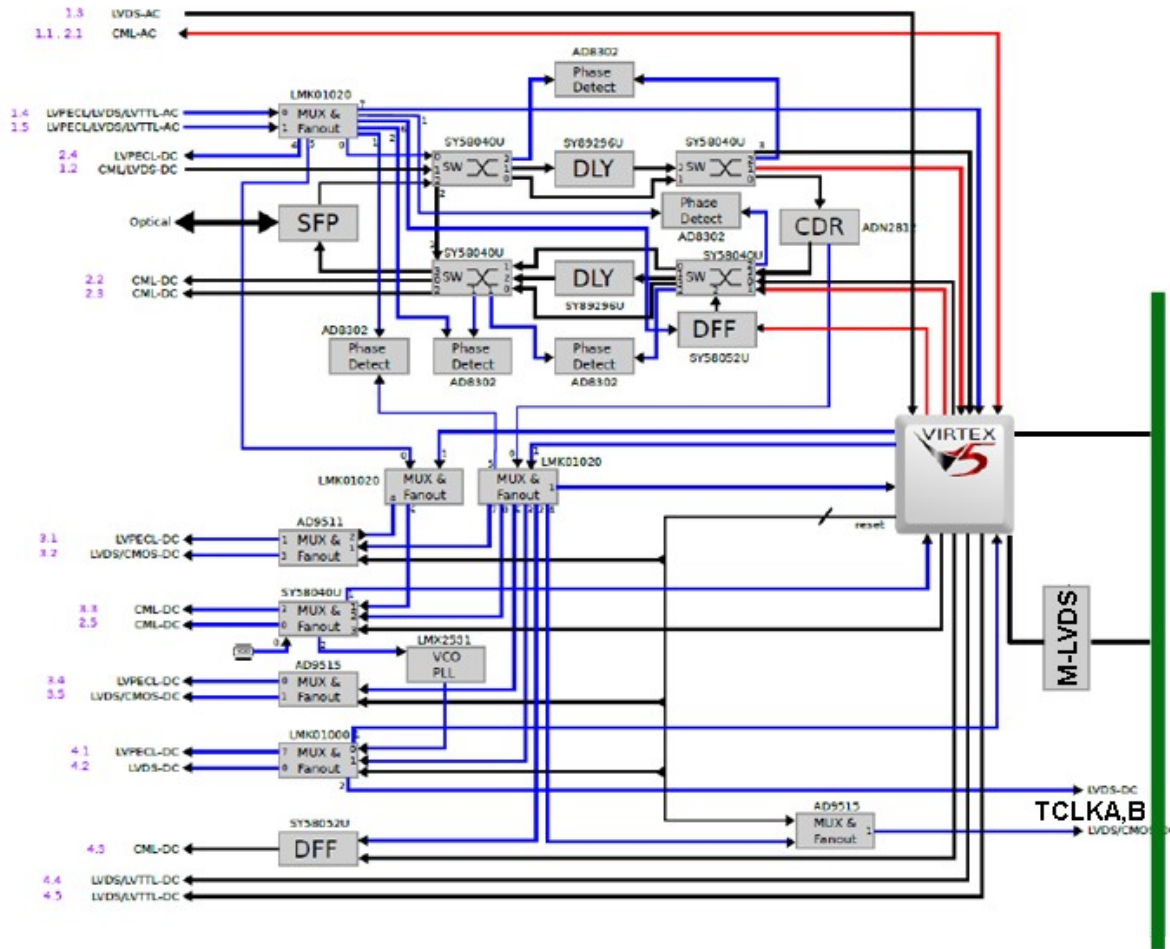
x2timer with RTM for Modulators



7 Timing Receiver Prototype (x1timer)

This first prototype implements a receiver and transmitter on a single module. It is compatible with the planned, second prototype. The differences to the final double size (x2timer board) is the restriction to only one fiber link and the absence of a RTM connector.





Drawing 16: Timing receiver block diagram of the first prototype (x1timer).

For a test of concepts and the evaluation of timing chips this single size AMC was designed and more than 20 modules produced. It is used in stand-alone applications to simulate a trigger sequence of XFEL for hardware developers as well as the first MicroTCA prototype systems in FLASH, CMTB and REGAE. A Linux driver, a DOOCS server and a jddd panel are available to be used in these prototype setups.

8 Events in XFEL

Events are used to synchronize all subsystems in XFEL. These triggers are generated at the rate of accelerator shots (macro pulses). They are synchronized with the line frequency (50 Hz) and 100.309 kHz ($= 1.3 \text{ GHz} / 12960$). This yields in a rejection of distortions from the mains since all sensitive electronics “see” the bunches at the same 50 Hz phase. The additional 100 kHz allows PLLs to run without jumps. The main trigger for a macro pulse is then triggered after a divider of the 50 Hz. A typical trigger rate is 10 Hz, 25 Hz will probably be the highest rate for XFEL. REGAE can run with up to 50 Hz. All further generated events are relative to this trigger. A concept of grouping of triggers for subsystems will be provided. This allows to shift e.g. the klystron high voltage with respect to the bunches. It is important to relate subsystems to the corresponding triggers in order to shift signals without losing the synchronization to e.g. the bunches. Further complications are caused by the wire scanners since they require a pre-trigger

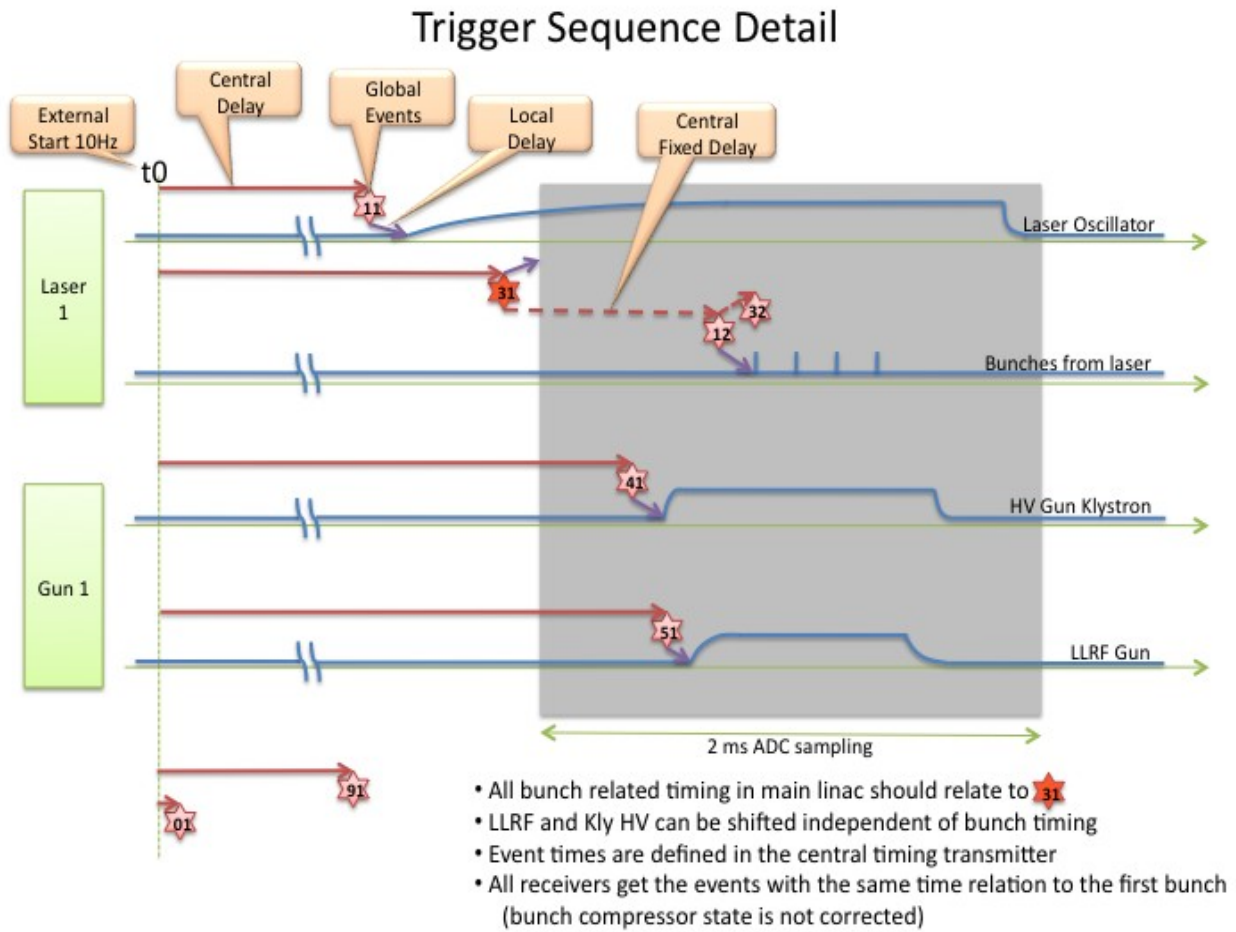
≥ 53 ms before the bunches. Switching from 10 Hz (100 ms) to 25 Hz (40 ms) demands a pre-trigger in the preceding macro-pulse.

XFEL needs to agree on a set of main trigger groups! Shown here is one possible solution only.

The following Table 5 demonstrates an example of grouping of triggers. The timing system provides global triggers that are defined in the central transmitter and local delays to adjust for local delays caused by e.g. different cable length from the detector to the electronics (Drawing 17).

Trigger #	Subsystem	Trigger #	Subsystem
1	Wire Scanner start motor	2	Camera trigger
11	Laser Gun 1 start	12	Laser Gun 1 start first bunch
21	Laser Gun 2 start	22	Laser Gun 2 start first bunch
31	Diagnostics main linac start	32	First bunch in main linac
41	RF Gun 1 start HV	51	LLRF Gun1 start
42	RF Inj1 start HV	52	LLRF Inj1 start
43	RF L1 start HV	53	LLRF L1 start
44	RF L2 start HV	54	LLRF L2 start
45	RF L3 start HV	55	LLRF L3 start
60	TDS start	61	
91	DMA setup	99	End of data acquisition

Table 5: A possible assignment of triggers. It allows to operate two injectors in parallel and to shift subsystems independently from each other.



Drawing 17: A possible trigger sequence of the injector as an example of global and local timing

To be able to shift e.g. the gun RF in relation to the beam, the timing of the gun (klystron and LLRF) must get the timing from the same event number. One parameter will be defined in the control system to shift the whole gun RF without influencing the other timings. Special care has to be taken that the recorded data is at a correct position relative to the overall diagnostics shown in the control system. Furthermore, if the RF is shifted with respect to the bunches, possible consequences in the LLRF system have to be considered (e.g. beam loading compensation tables must be rebuild, different phases from the klystron flat-top etc.).

Name	Frequency	Divider	Comment
1.3 GHz	1300.000000 MHz	-	
108 MHz	108.333333 MHz	12	
9 MHz	9.02777777 NHz	144	
4.5 MHz	4.513888 MHz	288	XFEL bunch rate
1 MHz	1.003086 MHz	1296	FLASH typical bunch rate
100 kHz	0.100309 MHz	12960	Lowest synchronization

Table 6: Frequencies in the system and the dividers from 1.3GHz reference

Name	Description
Trigger	A trigger with programmable delay (0..max repetition rate, e.g.100ms), width and fine delay.
Clock	Global clock supplied by a divider. If this clock is used by one “bunch clock” function then it requires to be 9.028 MHz since the pattern table is based on this frequency.
Gate	A signal that starts with a programmable event and delay and ends with the delay of a second channel.
Sync pulse	A synchronization pulse at the beginning of a macro pulse.
Bunch clock	A bunch synchronous clock that is gated with the expected bunches at the location of this timing receiver (logical AND with the pattern table). This clock uses a global 9.028 MHz output of a divider to generate a clock burst matches the pattern of the bunches. Depending on the desired pattern this signal can have variable distances between clock edges.
Slow data link	115 kbaud encoded data with e.g. the Macro Pulse Number.
Fast data link: clock	130 MHz clock to strobe the data.
Fast data link: data	130 MHz serial data with all information transferred from the master timing transmitter.

Table 7: Trigger output selection

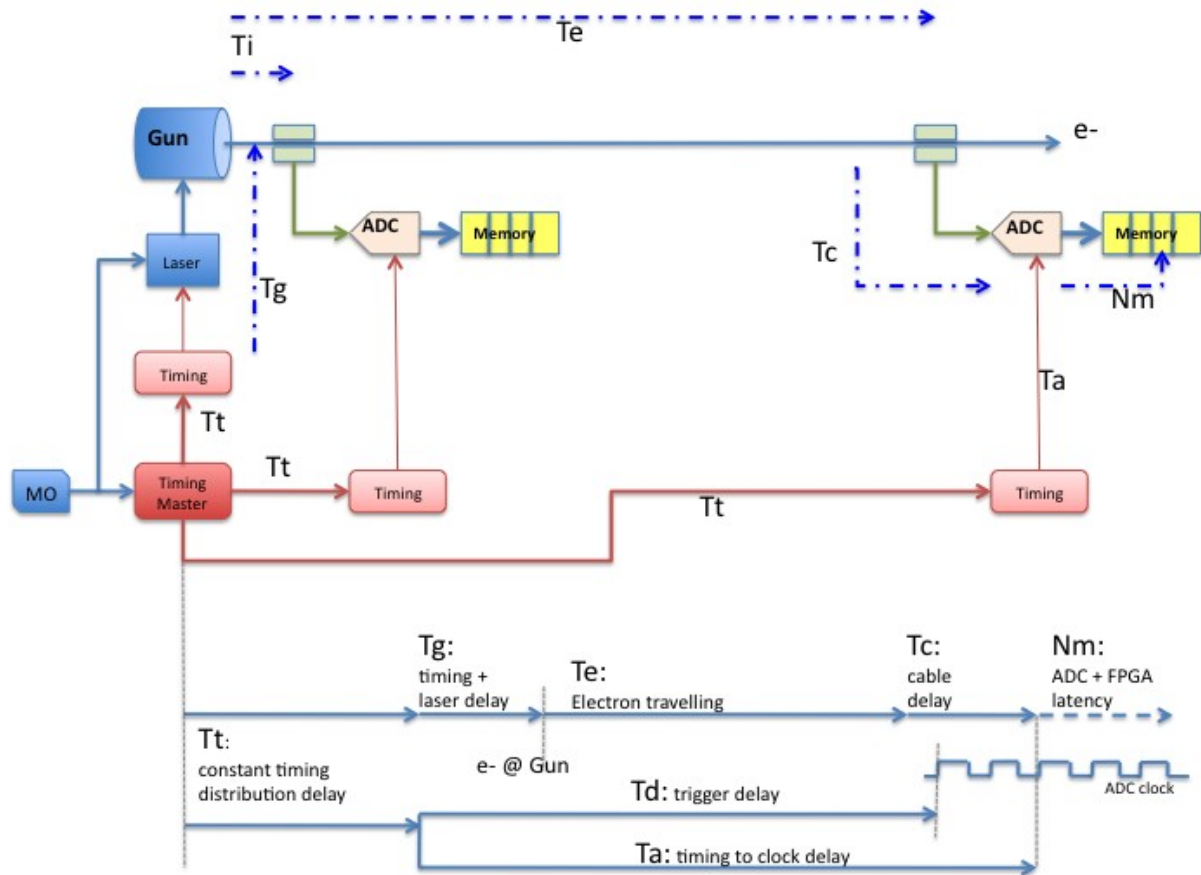
Stable clocks are available as TCLKA and TCLKB clocks on the MicroTCA backplane (Drawing 14). These clocks are direct outputs of highly stable dividers without a FPGA path in between. TCLKA will be typically set to provide 108 MHz, TCLKB can have any selectable frequency from Drawing 12. The dividers will be synchronized if required before every macro pulse by the SYNC command.

9.1 Calculation of the Timing Relations

Explanation of Drawing 19: the timing system receives 1.3 GHz from the Master Oscillator. This and other frequencies are used in the laser system to provide phase stable bunches. The selection of bunches by the pockels cells of the laser is controlled by the timing system by means of the defined bunch pattern of the macro-pulse. A timing master keeps the time T_t constant. The absolute time is determined by the fiber length and the delay of the transmitter. The total delay is measured and can be used by the transmitter to keep all T_t 's in the system identical.

XFEL Timing System Specs, Version 0.9

	Description	Derived from
Tt	Constant delay between the master timing transmitter and all receivers	Constant
Tg	Delay timing receiver to electron in the gun	To be measured or estimated
Ti	Delay of electron detected in a beam monitor in the injector	To be calculated from the z-position of the monitor
Te	Delay of electron detected in a beam monitor	To be calculated from the z-position of the monitor
Ta	Delay between timing receiver and start of ADC aquisition	To be measured
Tc	Cable delay from beam monitor to ADC	Calculated from the cable length
Nm	ADC latency plus latency of the memory in number of clock cycles	Calculated from data sheets



Drawing 19: Calculation of the timing relations

With these numbers one should be able to calculate the position of data in memory for e.g. the first bunch.

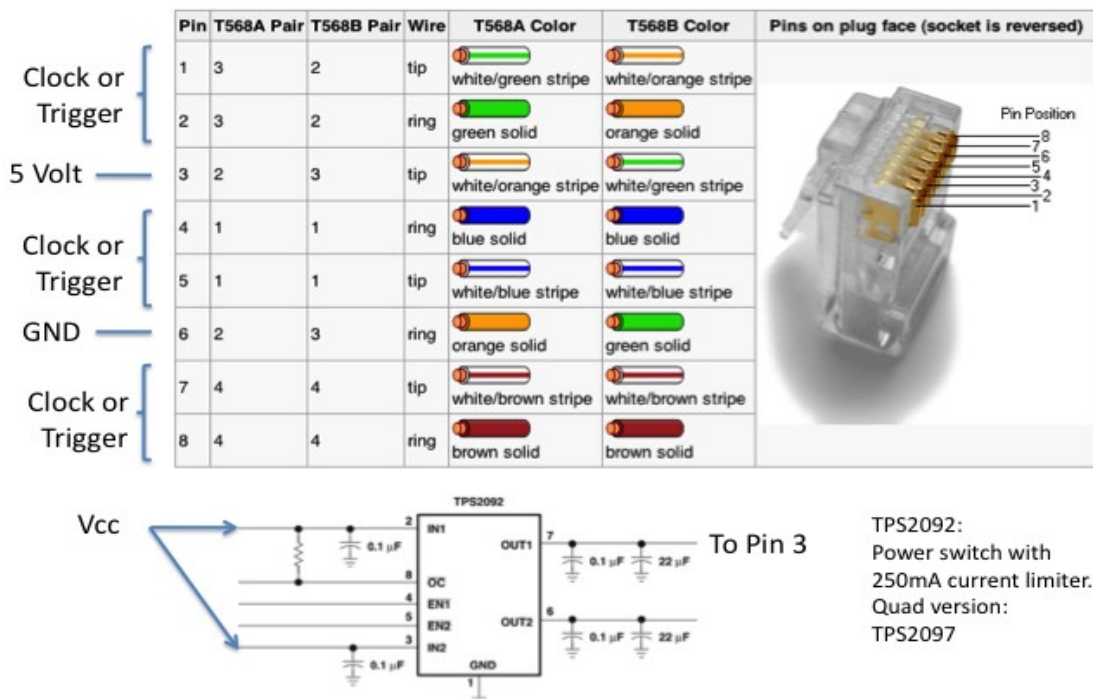
The triggers and clocks of the timing system are constant and will not be changed by e.g. the settings of the bunch compressors. Compressors can change the arrival times of bunch in the order of a few hundred picoseconds. Therefore, the phase relation of the first bunch to clocks and triggers may vary up to a ns, depending on the actual orbit in the bunch compressors, especially between the compressor on and off (in XFEL BC1 and BC2 can not be switched off).

10 Hardware Interfaces

10.1 Front Panel IO

The front panel outputs are provided as standard RJ45 plugs. The outputs are three differential clock/triggers and the 4th pair is a 5 Volt supply. CML standard was chosen since it allows driving high frequency signals (more than 1.3 GHz). Level conversion to e.g. TTL can be implemented by simple receiver modules with the help of the provided 5 Volt. A further advantage of RJ45 is that standard Ethernet cables are usable to drive the triggers to devices. The pin layout was selected to minimize crosstalk. This is not compatible with Power over Ethernet and one should not mix clock and trigger cables with network equipment.

RJ45 as IO Connector



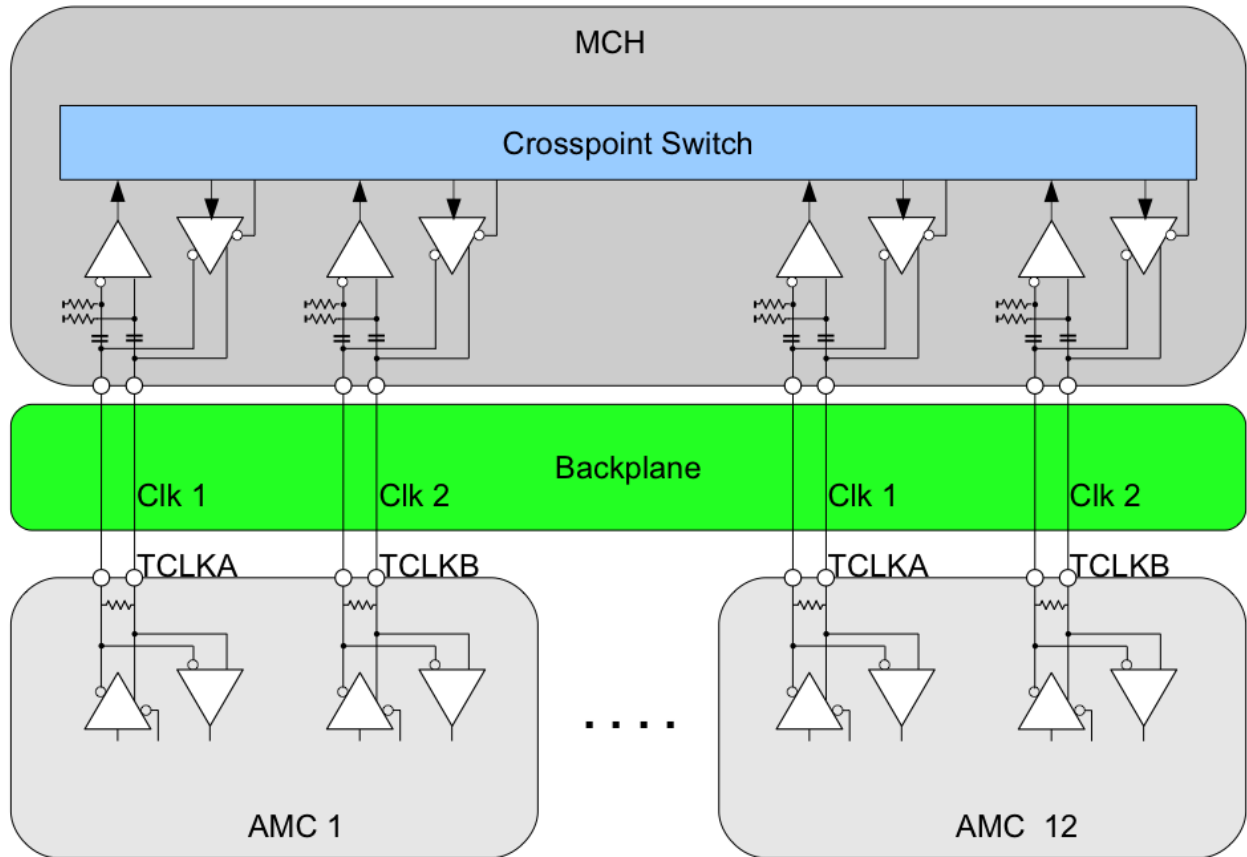
Drawing 20: RJ45 connector layout.

10.2 Timing Distribution within a µTCA Crate

The clock and trigger distribution within a MicroTCA crate is defined in the MTCA.4 document of PICMG ®. This specification was strongly influenced by the XFEL requirements. TCLKA and TCLKB are used to distribute low jitter clocks (see Drawing 21). The timing receiver is the source of the clocks and the MCH distributes the clocks to all requesting AMC's. The electrical standard is LVDS (as defined in MTCA.4 specs) and the connections are point-to-point with proper termination. Since this clock distribution is radial from the MCH to the receiving AMCs the arrival time differs by up to about a nano second between slot 1 and 12.

Clock	Frequency	Comment
TCLKA	108.333333 MHz	
TCLKB	Variable, e.g. bunch clock	Can be programmed, if bunch clock: 4.51388888 MHz

Table 8: Standard clocks in μ TCA crates for the XFEL



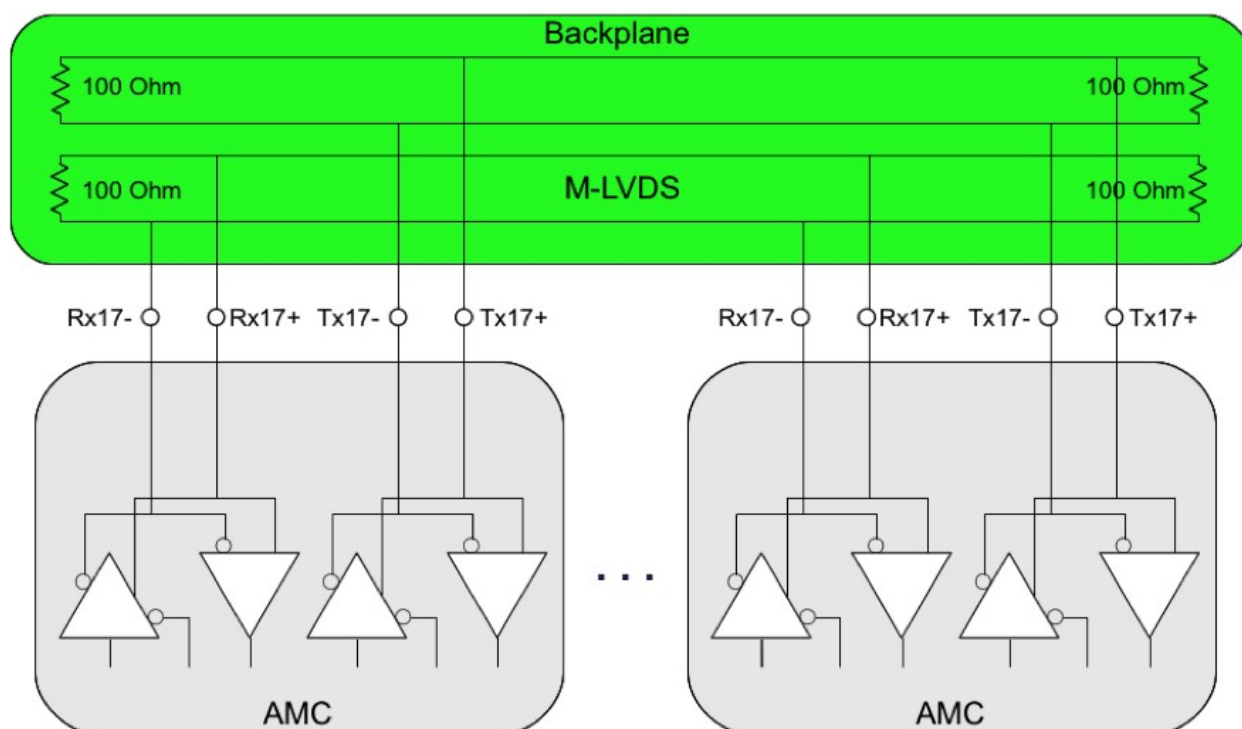
Drawing 21: Radial clock distribution within a μ TCA crate

The backplane as defined in MTCA.4 will contain in addition 8 M-LVDS lines to distribute further clocks, triggers and interlock signals. It is foreseen to use two of these lines to distribute an encoded clock that contains all the event information. This clock shall have a frequency of 130 MHz ($1.3 \text{ GHz} / 10$). This clock should be used to strobe the encoded data on the second line to be processed by FPGAs within the MicroTCA crate. The serial data on these BusData and BusDClock lines will pass the same information as the 1.3 GHz clock distribution between the master timing and the receivers to the AMC modules in a crate, but with a 10-times lower rate. This information contains all parameters of the timing, the event number and bunch patterns. The electrical connection is shown in drawing 22.

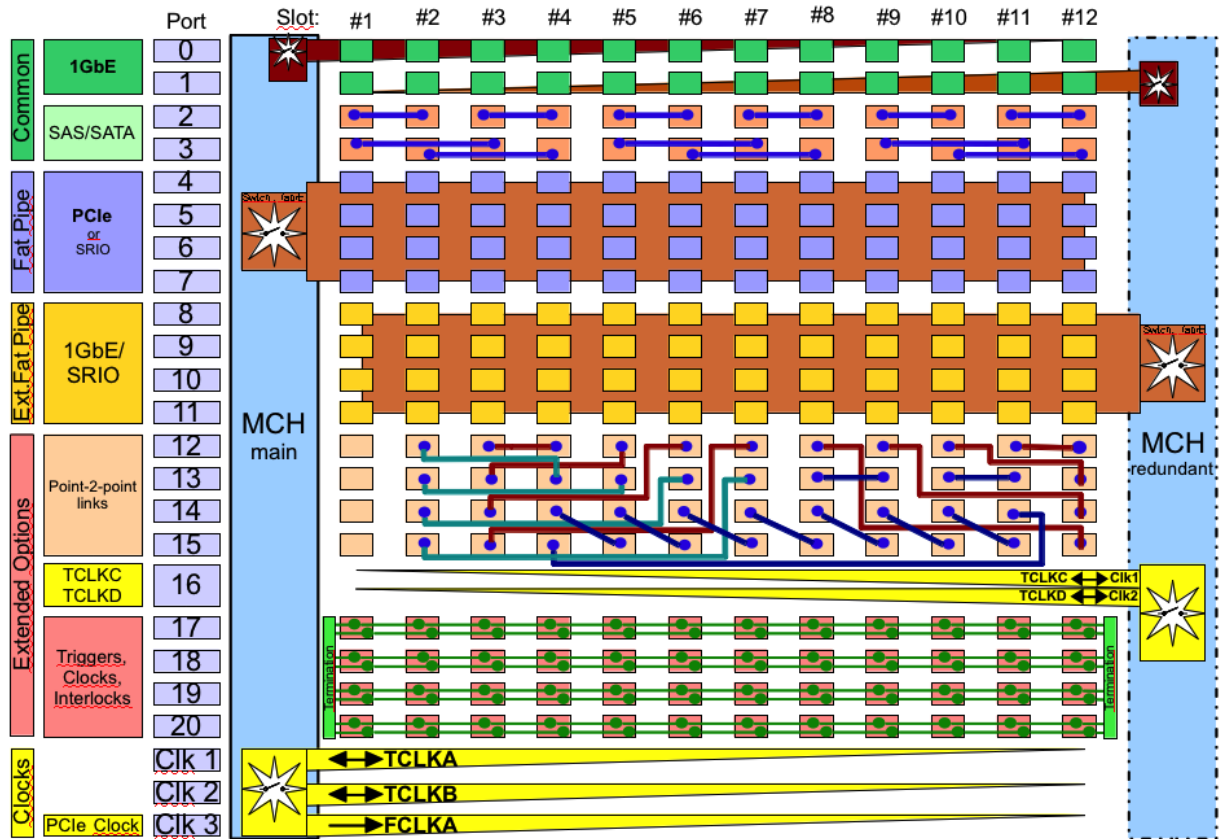
The topology of a XFEL backplane is shown in Drawing 23. A special variant was designed by the LLRF group to provide more board-to-board communication links. Nevertheless, the timing distribution is identical.

Port	Name	Description
Rx17	BusDClock	Clock to strobe the encoded 130 MHz data
Tx17	BusData	Encoded 130 MHz data
Rx18	StartTrigger	Beam Trigger with a fixed delay to first bunch
Tx18	PreTrigger	PreTrigger (about 30 ms @ 25 Hz, >= 60 ms @ 10 Hz before first bunch)
Rx19	AppTrigger	Free to be defined by application
Tx19	Ilock0	Interlock wired OR line 0
Rx20	Ilock1	Interlock wired OR line 1
Tx20	Ilock2	Interlock wired OR line 2

Table 9: Distribution of clocks and triggers on the bussed ports available on all slots



Drawing 22: Electrical interface of the bussed clock, trigger and interlock lines. One of 4 ports shown.



Drawing 23: 12 slot backplane for diagnostics

11 Software and FPGA Interface

11.1 Configuration

The configuration of the timing system is done via a PCIe interface on the MicroTCA backplane. A DOOCS server will provide all configuration parameters on the global control system network. This device server communicates via a Linux driver with the AMC module.

11.2 Fast Data Link in MicroTCA

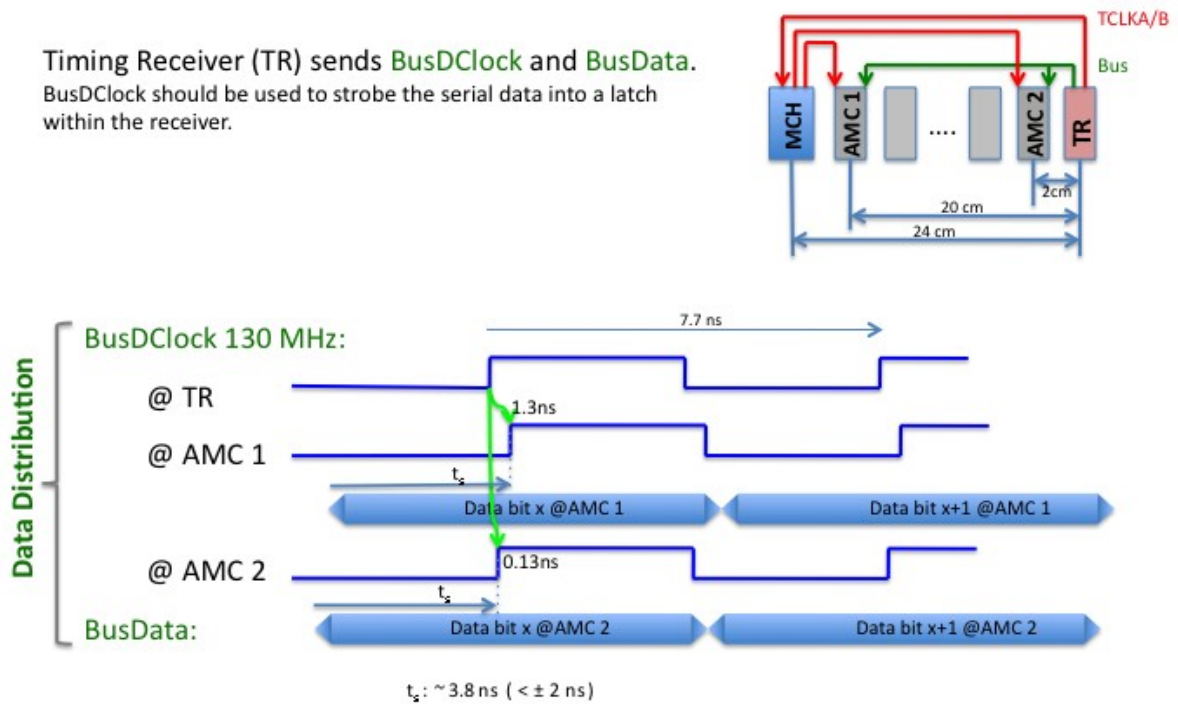
A serial data stream with all protocol information will be available on two M-LVDS bussed links of the MicroTCA backplane:

- BusDClock (Rx17): a 130 MHz clock on port Rx17 with a fixed relation to BusData.
- BusData (Tx17): serial data stream, 130 MHz bit rate

A simple UART protocol is used on the BusData line. It is described in Drawing 25. It should be noted that this 130 MHz clock has no reliable relation to the bunches in the linac. BusDClock should be used for serial data strobing only.

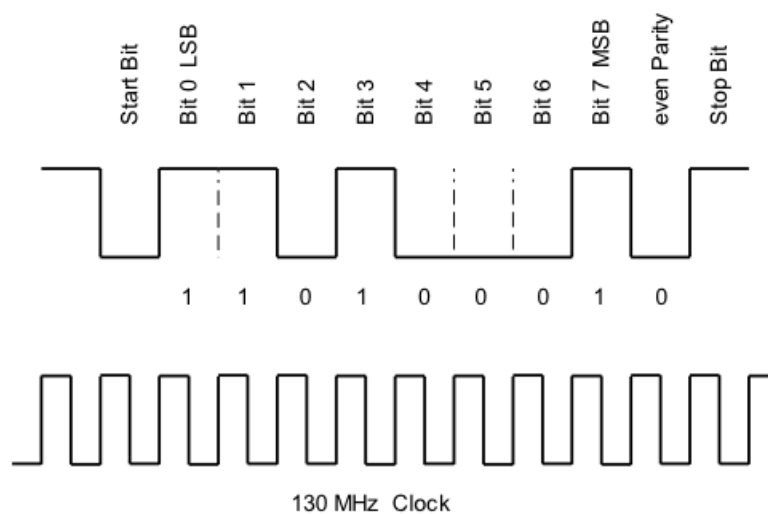
Data Distribution within a Receiving Crate

Timing Receiver (TR) sends **BusDClock** and **BusData**.
BusDClock should be used to strobe the serial data into a latch within the receiver.



Drawing 24: The diagram shows the relation of both the clock at the timing receiver (@ TR) and the BusData. Both signals are delayed by the propagation time on the backplane. The clock-data relation is fixed for all AMC positions. On the timing receiver the clock output positive edge is in the middle of the data to allow a relaxed strobing in the AMC.

Data on this data link is a buffered one-to-one copy of the incoming 1.3 GHz. If no data is received on the 1.3 GHz fiber link no data will be available on the data link.



Drawing 25: BusData protocol.

11.3 Slow data link

The slow data link is an UART-based protocol running at 115 kbaud. It will be used for the modulator and klystron controllers as defined in the respective CDRs.

11.4 Fast data link

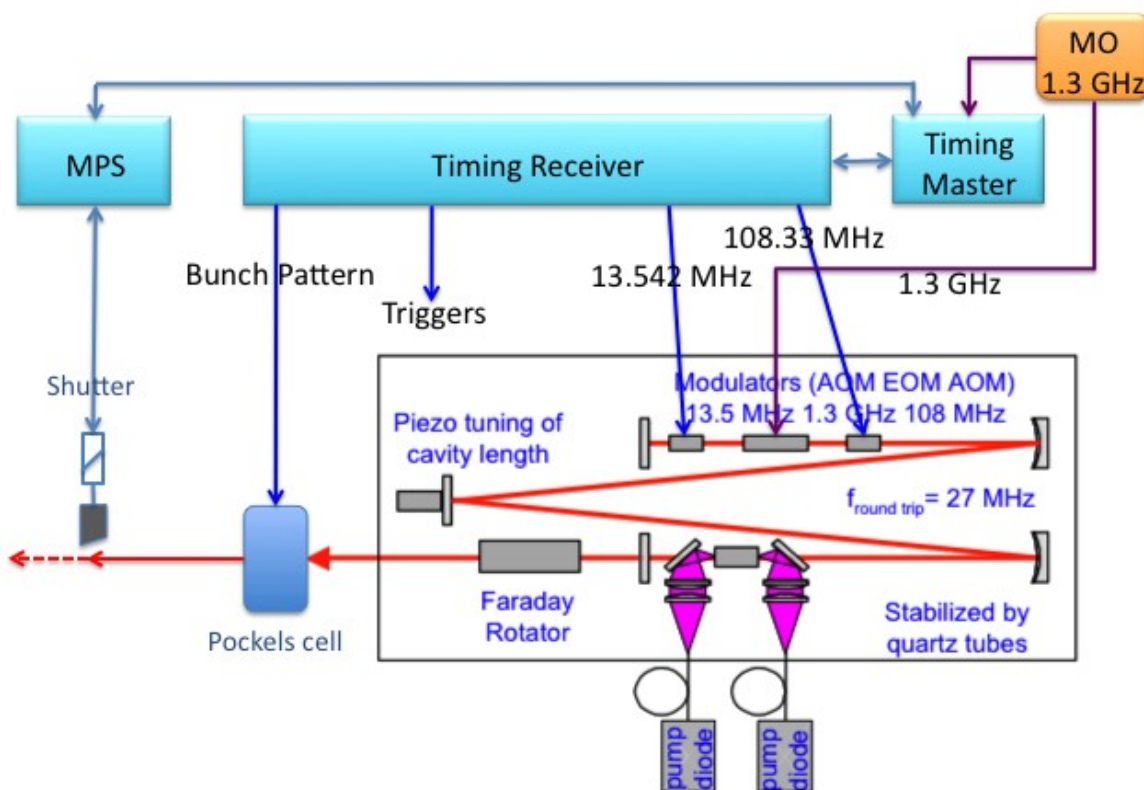
Optionally, the clock/data pair information on the MicroTCA backplane can be transmitted by a serializer with a 130 MHz rate on the front and RTM channels.

12 Subsystem Connections

12.1 Laser

The injector lasers have to receive the bunch pattern information from the timing. The pattern can directly be used to drive a pockels cell. But, special care has to be taken that varying patterns do not destroy laser amplifiers. All required triggers for a laser can be derived from a timing receiver. The timing could also provide the lower modulation frequencies of the oscillator since the dividers have to be reset by the timing system anyway (see Drawing 26).

Timing for the Injector Laser



Drawing 26: The timing system drives the injector lasers.

The laser shutter is controlled by the MPS. If the shutter is closed no bunches will arrive at the Gun and a corresponding mask inhibits all section bit in the bunch pattern table to mark that no bunch will be available in all parts of the linac.

12.2 RF (Modulator/Klystron)

A separate trigger and encoded data stream will be sent to all high power RF stations. The hardware interface is described in Drawing 14, the software interface in chapter 11.3.

12.3 LLRF

The LLRF subsystem will receive triggers and interrupts via the backplane connection. FPGAs in a MicroTCA crate can receive bunch pattern and further information from the serial lines described in chapter 11.2.

12.4 BPM

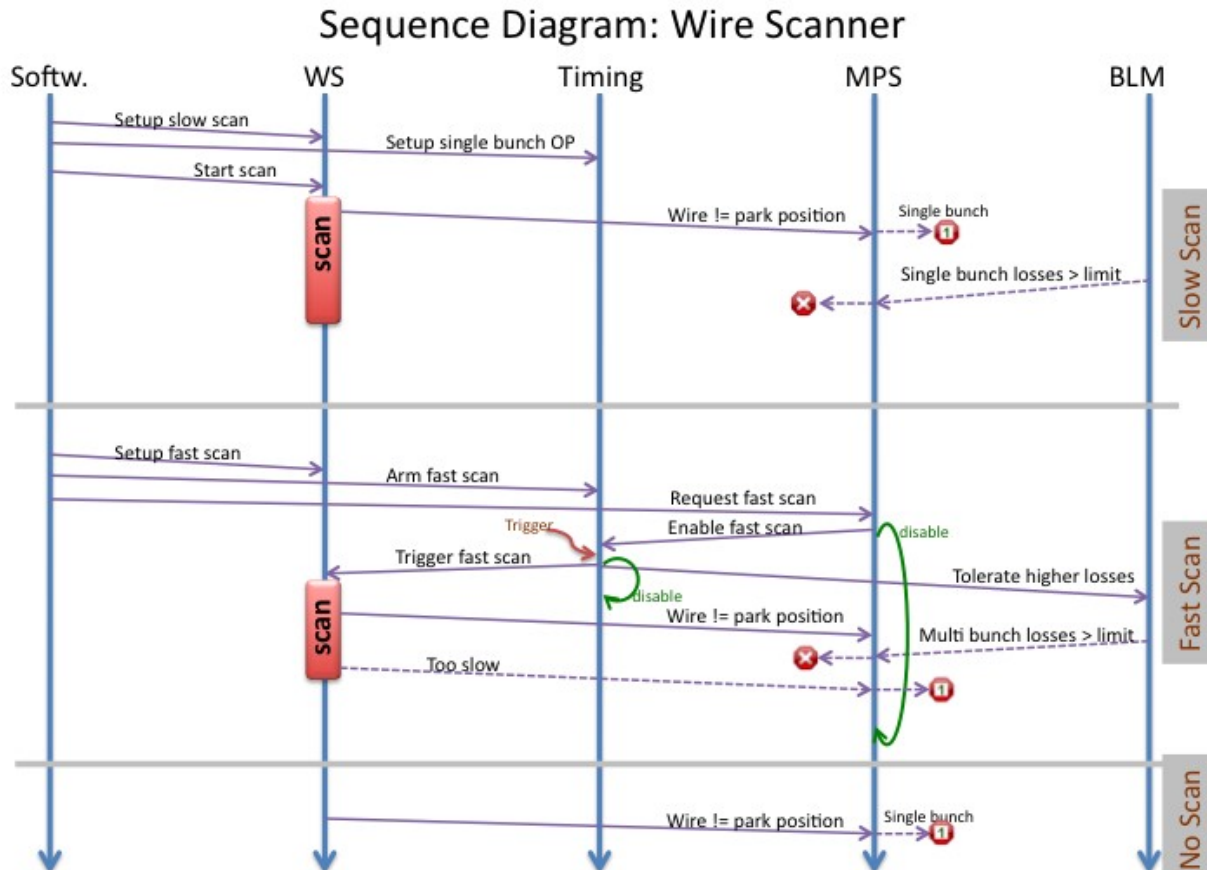
MBUs from PSI will directly decode the 1.3 GHz protocol received from a fiber link. Clocks can be extracted from this link as well. The protocol includes timing information for triggers and all required data like bunch pattern and bunch charge.

12.5 Toroid, BLM, Halo

- These systems require a fixed 108 MHz clock on TCLKA with a fixed time delay with respect to the bunches, see chapter 10.2
- A serial data stream with 130 MHz clock on the M-LVDS bus with e.g. bunch pattern and macro pulse numbers as described in 10.2 and 11.2.
- A trigger with a well-defined distance before the first bunch, e.g. trigger # 31.

12.6 Wire Scanner

Synchronization of wire-scanners requires several steps (a preliminary proposal is shown in Drawing 27). The timing system is used to inform all contributing systems if a scan will be



Drawing 27: Sequence diagram with software, WireScanner, timing, machine protection and beam loss monitors.

active for the next macro pulse. A scanner software sets up the subsystems involved and starts the sequence by requesting a scan from the master timing server. Bunches are marked with wire-scanner bit on. The wire-scanner FPGA starts by early trigger the motors. Beam-Loss-Monitors and the Machine-Protection-System are informed to tolerate certain losses. In slow scan mode is only permitted if the accelerator runs in “single bunch” or “short bunch” mode. After the bunches the corresponding ADCs have the information that a scan has to be processed and tag the data blocks for further processing in the DAQ and scanner software.

More considerations are required in fast scan mode in 25 Hz repetition rate. The scanners need a 53 ms trigger before the bunches. This requires a start trigger in the preceding macro pulse. The BLM system has to tolerate higher losses in the macro pulse following the scanner start.

12.7 TDS

Steps to operate a Transverse Deflecting Structure (TDS):

1. set-up subsystems
2. request the timing server to mark a bunch to be kicked

3. the deflecting cavity is triggered at the right time
4. MPS and TPS are ignoring the marked bunches

This complex sequencing has to be defined by WP 18 and WP 28.

12.8 Kickers

Kicker electronics are based on MicroTCA and the triggers are programmed and provided by a timing receiver within the crate.

12.9 Experiments and Photon Diagnostics

12.9.1 2D pixel detectors

The 2D pixel detectors for XFEL will be connected to the timing system via an interfacing MicroTCA module called “Clock & Control”. This module is a special RTM, compatible to the DAMC2. As timing related input it uses TCLKA or TCLKB to receive the continuously running 4.5 MHz bunch clock as well as the 8 M-LVDS bus signals. The bus is used for triggers and to decode the information provided on the BusData line.

12.9.2 0D detectors

The first currently implemented 0D detector is based on an avalanche photo diode. The read out hardware is based on an AMC (SIS8300) compatible to MTCA.4 and therefore uses the standard lines as TCLKA and TCLKB as well as the 8 MLVDS lines.

Future developments will be based on MTCA.4 and hence use the same interfacing.

If commercial systems have to be used and integrated, which are not based on MTCA.4, they will be most likely be connected via the RJ45 front panel connector.

12.9.3 Digitizer (incl. GMD, PES, BSM, Undulator Commissioning Spectrometer)

In experiments and photon diagnostics digitizers are commonly used devices. The finally used hardware for XFEL has not been decided on. If it will be an AMC, the standard MTCA.4 lines will be used. However, if other standards have to be used, the interfacing will most likely be done via the RJ45 front panel connector and a converter module to provide signal levels and connectors required by the system.

12.9.4 Beckhoff

The PCL-based solution for slow control and monitoring applications will use Beckhoff’s EtherCAT series. Most applications don’t require synchronization with the machine. However, for those, which do rely on timing, special synchronization modules are used, which allow hardware triggering down to ns-levels. Those modules will be connected to the timing systems via the RJ45 connector and a level converter or via a specialized RTM for the timing receiver, which allows a higher fan out and longer distances to the PLC modules.

12.10 Pump-probe laser

The pump-probe laser system for XFEL consists of different lasers and stages. The general, first laser in a chain is regarded as seeding laser and has to be phase stabilized to the MO with highest accuracy. Therefore those lasers will be locked by the optical synchronization system (WP18).

In the following stages, however, the repetition rate of the pulses has to be divided and gated

similar to the injector laser. Those stages require synchronization through the timing system.

As for almost all non-MTCA.4 systems also here will the interfacing been done with RJ45 connectors and level/connector converters. For the systems defined up to now, this will be TTL level and BNC connectors.

13 Measurement of the Total Delay Time (Transmitter → Receiver)

1. Transmitter sends out a “Probe” command and measures how long it takes to receive the signal back at the transmitter. The measured delay is divided by two and stored in the transmitter for each link.
2. The transmitter asks for the ID of the first receiver (“RecIdReq” command). Remember, a receiver might locally distribute the clocks. The first receiver is the local master and returns his ID with a “RecIdResp” command.
3. The transmitter sends out the delay information to the ID of the local master with the last byte set to 255 = local broadcast. All local receivers can detect this delay command and store the information if the first 3 bytes matches their ID.

ID's are individual address like IP numbers in Ethernet (see Table 4). They are configured by software. A local group of receivers must have the same part A to C of the ID.

14 Timing System DOOCS Server

Every crate with timing hardware installed requires a DOOCS server to setup and configure various parameters. This server is the interface between all timing settings and user interfaces like jddd panels or MATLAB scripts. ALL timing configurations have to pass this server. After a power-failure or any other restart of the system, the DOOCS server will restore all timing parameters to the previous state. It is also responsible to restrict access modifying timing parameters.

A Linux driver interfaces the DOOCS server and the timing hardware. All data transfer between server and hardware is handled by the driver. The driver also distributes the interrupts from the timing.

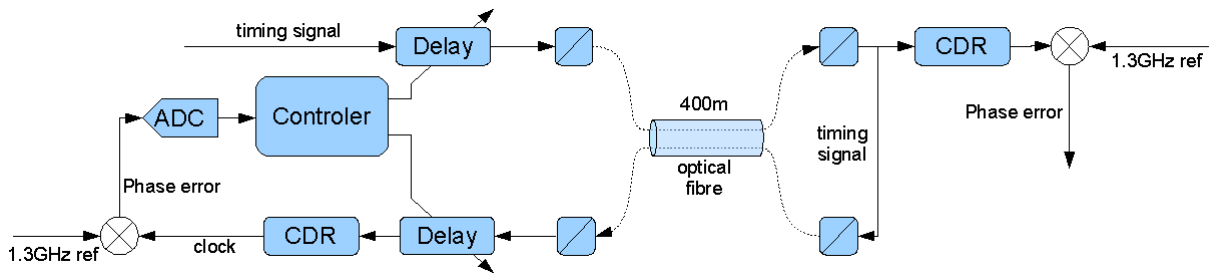
For the x1timer a DOOCS server was developed. It controls more than 500 properties including settings for all trigger channels, interrupt control, configuration of the chips and the FPGA. All delay and pulse duration settings are also archived by the server to be able to track changes of parameter settings.

15 Operator Interface

TBD

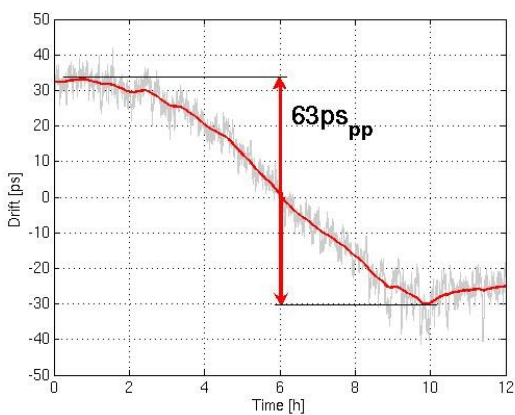
16 Performance Data

Preliminary(!) results from measurements of the design principles are shown in the following figures. The measurement was done with a circuit shown in Drawing 28 and a 400 m long fiber link. It was intended to check only the long time drifts during this test.

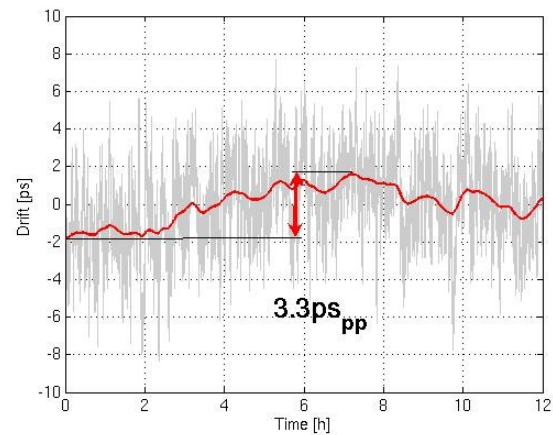


Drawing 28: Drawing of the used circuit to measure the performance

Without any compensation the drift caused by 8 degrees of temperature change is about 63 ps peak-peak as shown in Drawing 30. After compensation with the prototype the drift was reduced to 3.3 ps peak-peak as shown in figure 29.



Drawing 30: Uncompensated temperature drift caused by temperature change



Drawing 29: Results with drift compensation (preliminary)

Drift and jitter specifications of timing system:

- Jitter and drift of high precision clock edge (e.g. TCLKA) to the bunches: ≤ 5 ps RMS
- Jitter and drift of low precision clock edge to the bunches: ≤ 200 ps pk-pk
- Jitter and drift of triggers with respect to bunches: ≤ 200 ps pk-pk
- The timing system will NOT compensate different delays caused by bunch compressors!

Glossary

Term	Definition
AMC	Advanced Mezzanine Card: An IO card or a CPU for a MicroTCA crate.
Event	A fiducial with a fixed relation to the bunches. Events are numbered and used for many different synchronization tasks. They are repeated every macro-pulse.
Macro-pulse	A shot of the linac with bunches of electrons with a duration up to 800 μ s plus the filling and decay time of the cavities. Usually repeated with 10 Hz.

XFEL Timing System Specs, Version 0.9

MacroPulseNumber	A unique integer that is incremented by one for every macro-pulse. It is used to tag the data from all subsystems to allow a correct correlation of data.
Mode	Operation mode of the linac. It defines the maximum number of bunches permitted per macro-pulse as: single, short or long bunch mode. The MPS grants the mode by reading the machine settings and interlocks.
MPS	Machine Protection System: a distributed hardware system that collects interlock conditions and safety relevant states. It stops the beam when it detects possible harmful situations.
MTCA.4	Micro Telecom Computing Architecture 4: A PICMG specification that specifies MicroTCA enhancements for Rear I/O and precision timing.
ShotID	An ID of the sequence/cycle type of the actual macro pulse. Consecutive macro-pulses can have different bunch properties. Bunches with identical properties are marked with the same ShotID:
RTM	Rear Transition Module: I/O signal conditioning card plugged from the rear side in a MicroTCA crate. Is defined in MTCA.4.
x1timer	A single size AMC module that implements a timing receiver and transmitter.
x2timer	A double size AMC timing module. This will be the final version for XFEL.