

C&C veto definition

23.10.2009.

The May 2009 XDAC requested a review of the veto handling scenario for 2D pixel detectors. The proposal below develops the original veto by encoding more information into the signal sent to the FEE. The original suggestion came from Heinz.

We (C&C and detectors) should discuss this at the next TB+C&C meeting, but immediate feedback is welcome/required in view of the Oct. 2009 XDAC. The development has implications for the design of the FEE and C&C systems.

1 Original definition of 2D veto

The veto was conceived to reduce the number of “poor quality” images stored in the storage pipelines of the FEE ASICs by flagging pulses to be rejected at the FEE. The veto implementation foresaw the C&C distributing a 5MHz clock, with accept/reject decisions encoded onto it, to the FEE which then reuse the rejected storage location.

The original design foresaw vetoing the current pulse, which required the veto reject latency at the FEE to be $< 200\text{ns}$, the inter bunch period. This was later relaxed by introducing intermediate storage buffers of depth ≤ 10 into the ASICs which store data before final commitment to the storage pipeline.

The veto is clearly more important for those detectors with limitations in storage pipeline lengths.

2 Improved definition of 2D veto

It is now intended to relax the latency requirement further by replacing the 5MHz veto reject/accept clock, distributed by the C&C, by a higher frequency clock with bunch numbers to be rejected encoded onto it. A schematic showing the generation of the improved veto is shown below.

The veto unit (VU) receives input signals from veto detectors, derives bunch numbers to reject by evaluating logic expressions on the inputs, and outputs bunch numbers to be rejected. The FEE is required to translate the bunch number received into the corresponding storage pipeline column number and enable its reuse.

The following sections list the requirements for the various parts of the system.

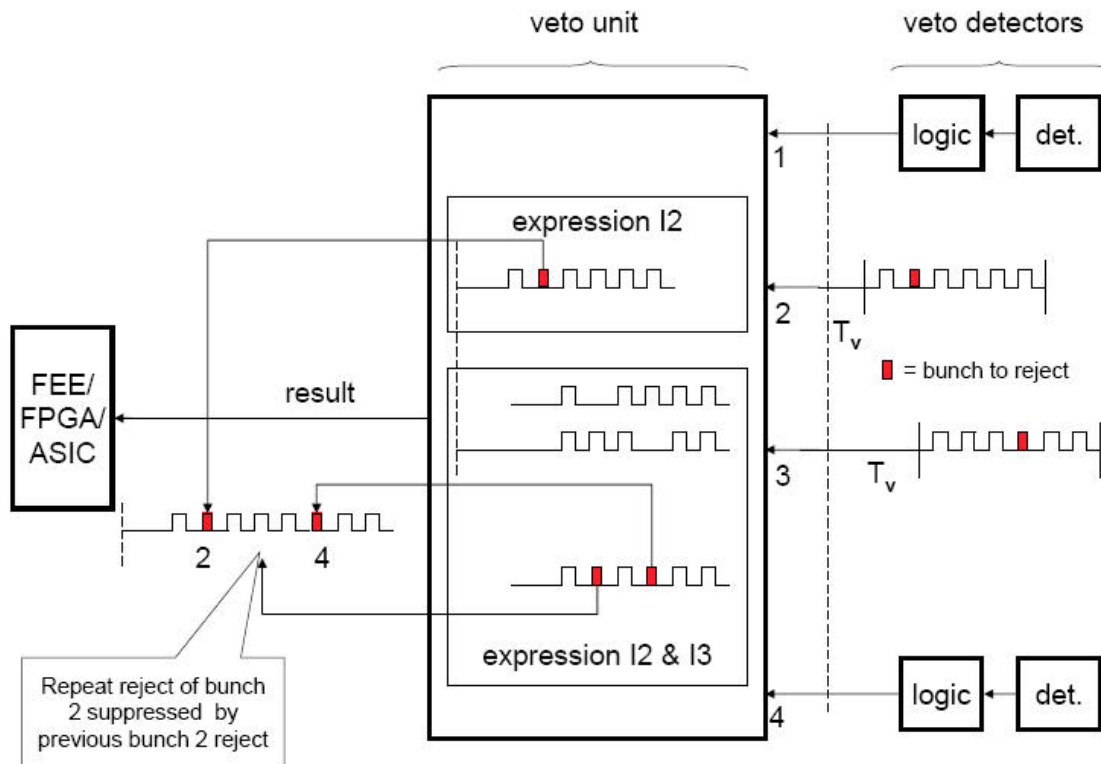


Figure 1 Overview of improved veto generation

2.1 Input signals

Input signals satisfy the following:

- Inputs are 5MHz clocks onto which accept/reject information (i.e. 1 bit) from a veto detector are encoded. This is the same as the original veto.
- Clock generation and data encoding are the responsibility of the detector builder.

2.2 Veto unit (VU)

The veto unit satisfy the following:

- Multiple detector inputs are foreseen (4?)
- Programmed logic expressions (e.g. I2 & I3, I2...) are evaluated to determine bunch numbers to be rejected. All results from all expressions are passed to the output handling layer.
- To evaluate an expression involving different inputs (e.g. I2 & I3), the VU must handle input delay difference (either using programmable delays or ...). The timing delay is determined by special timing runs (how?).

- Single input expressions (e.g. I2) are evaluated without delay, synchronization to the next 5MHz bunch clock cycle is required (special runs required?)
- The VU enforces the rule that a bunch number can be rejected only once by suppressing later occurrences. A bunch number can be rejected more than once because multiple expressions may be programmed.
- Bunch numbers to reject are pipelined (written to FIFO). Pipelining is required because multiple expressions can generate bunch numbers to reject at the same time.

2.3 *Output signals*

The output signal satisfies the following:

- The output is a 100MHz clock allowing 20 bit payload.
- 12 bits are used for bunch number encoding, additional payload bits are reserved for later use.
- The output is synchronized (by the VU) for use at the FEE to the 5MHz bunch clock in the same way as other C&C fast signals.
- The output payload is a bunch number taken from the FIFO, if no bunch number is to be rejected 0xFF... is sent(?)
- The VU must be fully programmable and allow monitoring at the pulse train frequency.

2.4 *FEE requirements*

The FEE is required to:

- Capture the bunch numbers to be rejected.
- Translate captured bunch numbers into the storage pipeline columns
- Reuse the rejected columns.

3 **Issues**

The input delay due to: veto detector hardware, veto detector logic and propagation times have to be determined. This can be done using identifiable pulse patterns in special timing runs (can it?). The delay would then be programmed at the VU.

The input veto latency (T_v) should be as short as possible for each veto detector. Values $\geq \frac{1}{2}$ RF flat top ($\sim 300\mu s$) are inefficient as not enough pulses remain to be delivered to fill vetoed pipeline columns.

The overall improvement in data quality depends on: the probability that a pulse is good (P), the probability that a pulse is bad (1-P?) and ΔT (a few plots would be useful?). As no simulations exist the efficiency of the veto remains uncertain.