VETO strategy and requirements

XDAC review
12-14th Oct. 2009
HLL - Munich

C.Youngman and H.Graafsma
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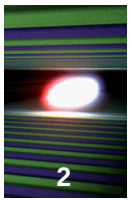
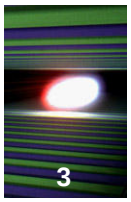
VETO Requirements – the original plan



- Original plan
  - external detector + logic generate veto decision
    - ➔ binary yes/no VETO decision
    - ➔ encoded onto 5 MHz VETO clock
  - 2D “Clock and Control” sub-system
    - ➔ receive VETO clock,
    - ➔ distribute clock to FEEs (synch for propagation delay, etc.)
  - FEEs mark storage cell vetoed for reuse
- Problems
  - VETO decision had to arrive before the next bunch
    - ➔ tight requirements on VETO generator
  - relaxing “before next bunch” requirement
    - ➔ led to intermediate buffering in the ASIC (LPD+AGIPD)
    - ➔ note: DSSC’s digital pipeline not affected

VETO strategy



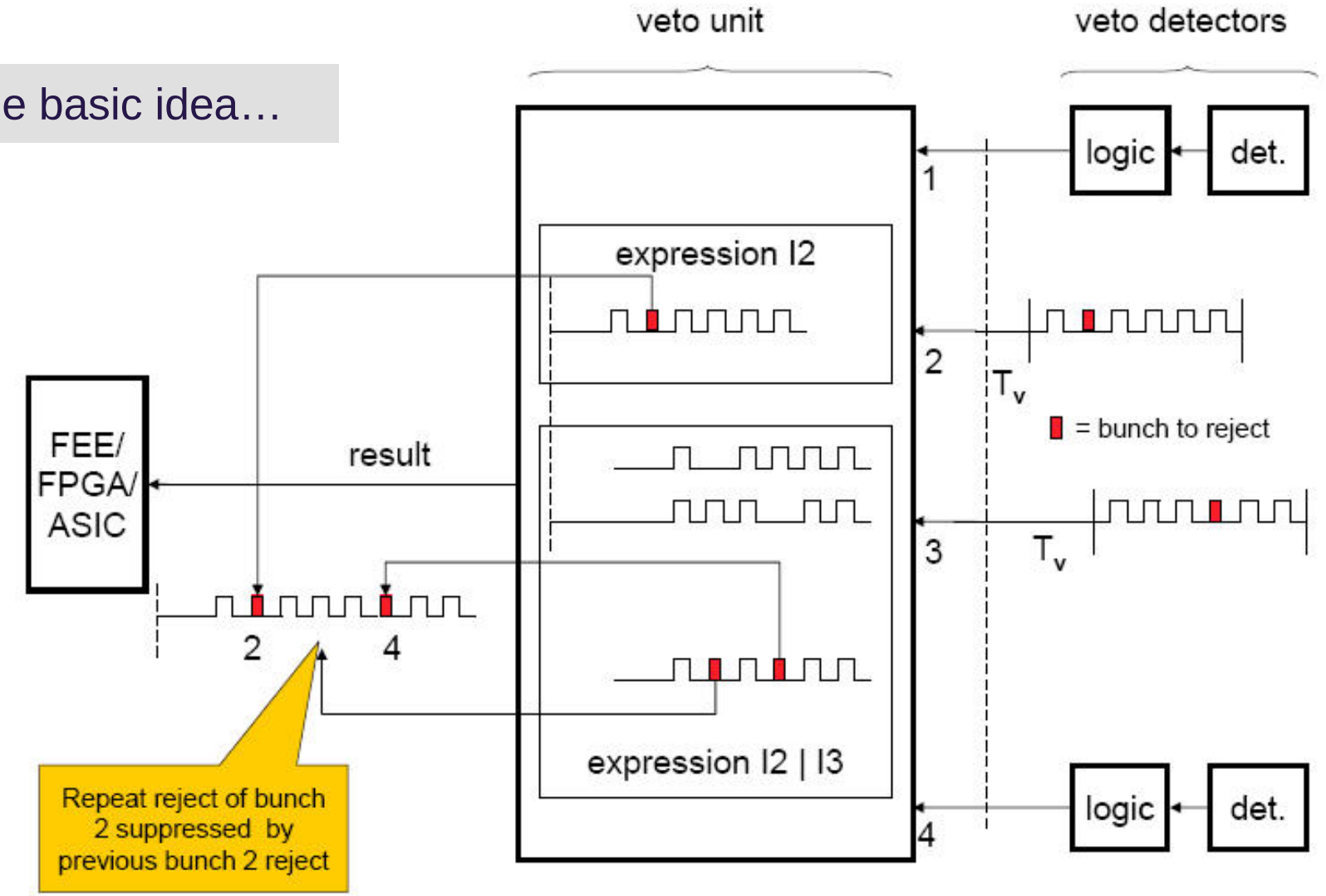
- New proposal
  - allow multiple veto generators
    - ➔ use original decision signal definition (binary yes/no, 5MHz)
  - 2D “Clock and Control” sub-system
    - ➔ receive multiple VETO clocks,
    - ➔ evaluate decision clauses between inputs (if >1)
    - ➔ distribute vetoed bunch number to FEEs (~20bit on 100MHz) (synch for propagation delay, etc.)
  - FEEs mark storage cell vetoed for reuse

See schematic on next slide

European XFEL

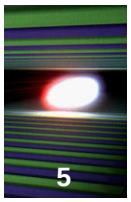
VETO proposal

The basic idea…



European XFEL

VETO conclusion



- Benefits
  - removes intermediate buffers
  - further relaxation of timing restrictions
    - ➔ improved pipeline cell usage efficiency
  - increased flexibility
    - ➔ 20 bit payload (12 bit veto decision + 8 for later use)
    - ➔ multiple veto inputs and clause evaluation allowed
- Uncertainties
  - no simulations of generators or efficiencies
  - discussion at the 22nd Oct TB+C&C meeting

Proposal distributed to FEE and C&C groups (mid Sept) - discussion at the 22nd Oct TB+C&C meeting.