# Introduction

## Train builder and clock and control meeting

C.Youngman for WP76

UCL, 11-May-2010

European XFEL

# Status of contracts


- Status of contracts
- Actions from last meeting
- Update on single crate “small” DAQ system development

European XFEL

# Status of contracts

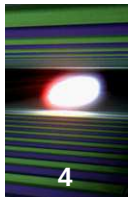

- Clock and Control (pre UK pullout from EuXFEL)
  - Contract signed in Dec 2010

- Train Builder (post UK pullout from XFEL)
  - Memorandum of Understanding (MoU)
    - ➔ umbrella for post pullout work with STFC,
    - ➔ STFC and EuXFEL have agreed on the text (significance to TB?)
    - ➔ status: complete, needs signing
  - TB contract updated for terms of MoU
    - ➔ EuXFEL versions sent to STFC
    - ➔ receive STFC checked version today?
    - ➔ status: present for signing a.s.a.p.

It is important to sign quickly, as many contracts will appear soon.

European XFEL

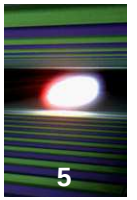
# Actions from last meeting




- 1. Check correctness of mailing lists
  - Done – send any additional updates to me
- 2. Nicola Coppola – LCLS non lazing pulse rate
  - Done – low (≤ mean - 3δ) intensity pulse rate ~few %
  - May be different at XFEL, but not encouraging for VETO
- 3. Planning of VETO meeting
  - Input from 2
  - Use of single APD detectors for VETO – cf. 1 crate DAQ.
  - Not done – still needed, reason to rush?

European XFEL

# Actions from last meeting




- 4. UCL's requirements for timing system
  - Status from K.Rehlich
    - ➔ Prototype tests complete – components to give required stability now fixed.
    - ➔ Production series boards – being finalized
  - K.Rehlich promises description by 1.6.2010
    - ➔ Includes backplane bus and p2p lines usage
  - Pressure needed – engineers asking questions.
    - ➔ UCL CC folk need to come to HH – apply pressure
    - ➔ Pressure also coming from 1 crate DAQ development
    - ➔ Need a meeting in HH soon – when?

European XFEL

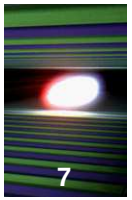
# Actions from last meeting


- 5. Uncertainties in TR and MPS interface definitions
  - For TR see point 4.
  - For MPS: A meeting in June discussed by LINAC group
    - ➔ On mail notification list – no date fixed.

- 6 + 7. Software development between WP76 and FEEs
  - Boundary definition – not done
  - Discussion of development – note done
  - Suggest 1 week meeting in HH – fix date now?:
    - ➔ June 7th, June 14th (what are Sergey's holiday plans)

European XFEL

# Actions from last meeting




- 8. Design decision concerning CC physical interface
  - See Martin's talk
- 9. CC fast signal specification note
  - Done – available on website, new since March:
    - ➔ LPD & DSSC = fixed latency VETO implementation
    - ➔ AGIPD & ~~DSSC~~ = variable latency
- 10. MoU – see status of contracts above.

# Update on single crate “small” DAQ system development


- Planning since Jan. single crate DAQ system to:
  - DAQ for APD pulse probe experiment:
    - ➔ Phase 1 = 130 kHz, 12 bit, ~4 channels
      - Run at PETRA 3 (1 bunch mode) at end of 2010
    - ➔ Phase 2 = 5.2 MHz, 16 bit, ~4 channels
      - Run at PETRA 3 (40 bunch mode)

- Details on
  - http://www.xfel.eu/project/organization/work_packages/wp_76/daq/single_crate_daq/
  - Also see appended spare slides

# Update on single crate “small” DAQ system development



- Two implementation solutions worked through:
  - Common features:
    - one xTCA crate,
    - one timing synchronization board, Synch Board
  - Different features:
    - 1. DESY DAMC2 front board + custom integrating ADC RTM
    - 2. STRUCK 125 MHz 10 channel ADC front board + custom shaper.
- Decision on which solution to implemented – end of this week
  - Which crate to order: Elma or other - 17.5 decision of Rehlich
  - Have already requested 2 DAMC2 (not affected by decision)
  - …

Overlap with 2D systems: Non XFEL timing board, VETO generation… discussion is needed.

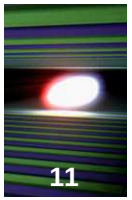
European XFEL

# Website - reminder


- WP76 website on:
  - http://xfel.eu – where it is difficult to find
  - Home directory is:
    - ➔ http://www.xfel.eu/project/organization/work_packages/wp_76/
- Use the right hand side navigation menu !
- 2D pixel related in:
  - $HOME/daq/2d_pixel_detectors/
  - Internal is pwd protected
- Your names are visible as mailing list members

European XFEL

# Spare slides – single crate DAQ PBS talk



European XFEL

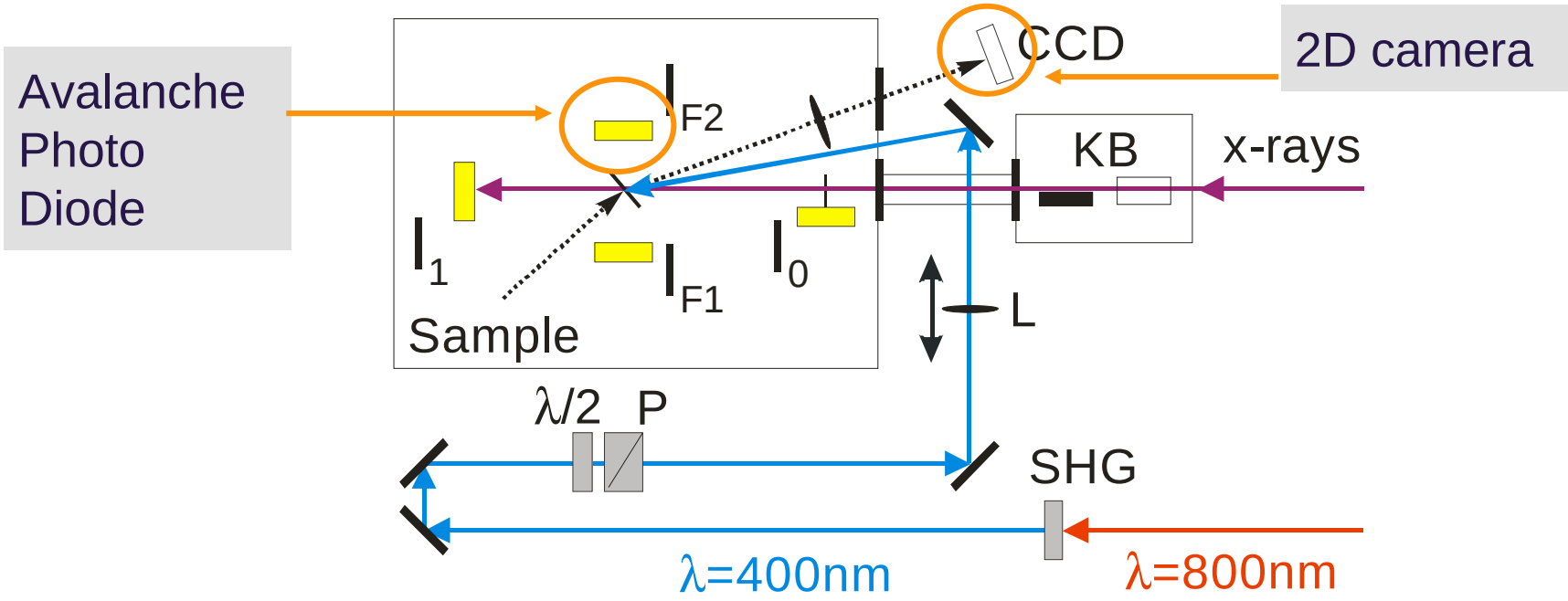
# Why develop small DAQ systems?


- Whether at EuXFEL or elsewhere: custom or commercial solutions need (some) interfacing
- Potentially there are many “small”, non 2D, pixel DAQ users:
  - Experiments: e.g. Ch. Bressler’s APD, strip detectors…
  - Diagnostics: e.g. PES…
  - DAQ: veto management…
- A single implementation standard is advantageous.
  - Once available other uses will appear.
- Need to develop in house expertise.

Starting point (Jan 2010) = prepare designs for APD and veto management

# Usage showcase – APD (Ch. Bressler slide)






- Expt. setup: Time-Resolved XAFS at SLS
- Detectors used: small number of APDs and 2D camera
  - result derived from APD data
  - CCD used for setup diagnostics, not to derive the result

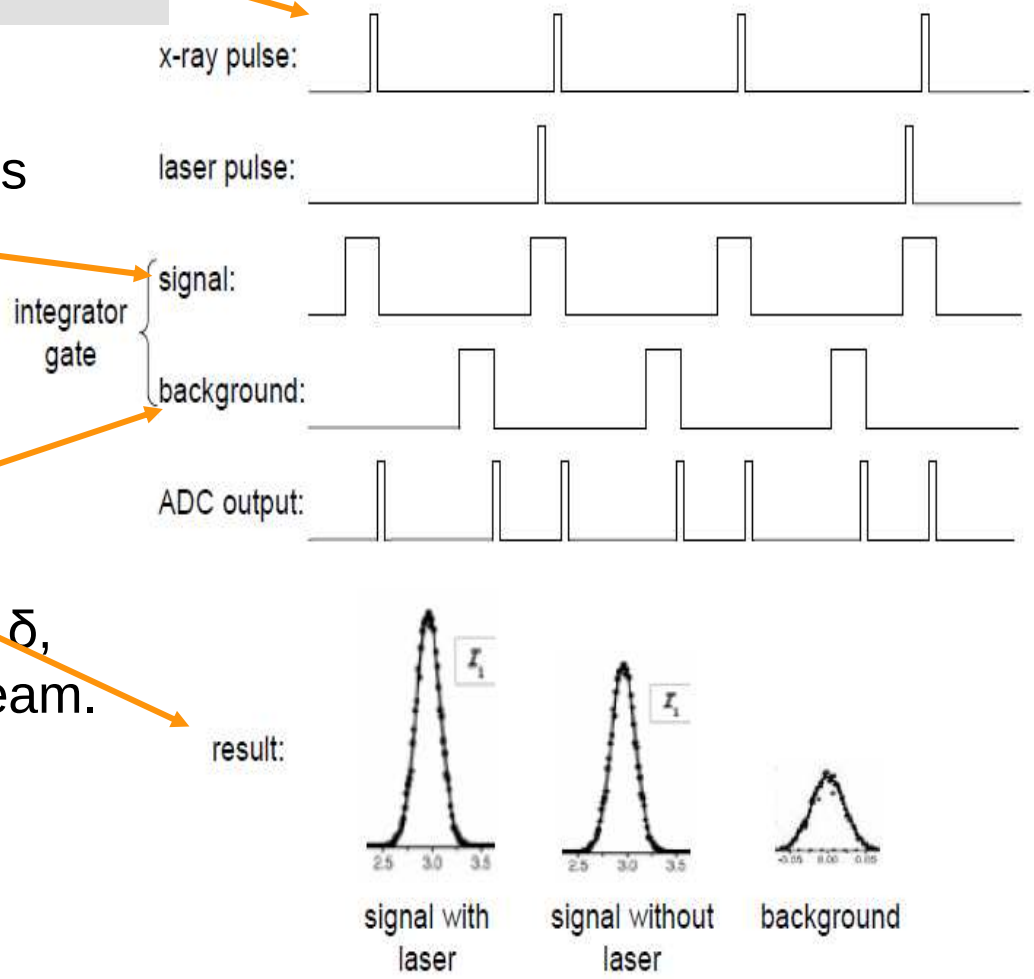
European XFEL

# APD – measurement scheme



130 kHz – 5.2 MHz

- DAQ required to:
  - control and synchronize APDs
  - digitize APD signal
    - ➔ at x-ray pulse rate
    - ➔ mark with laser (yes/no)
  - digitize APD background
  - fill result histograms
  - transfer result (histograms or δ, <>) and/or raw data downstream.



European XFEL

# APD – DAQ requirements & time lines



| # | Property | Value |
|---|---|---|
| 1 | To operate where | PETRA3 and XFEL |
| 2 | Pulse frequency (see #10) | ~100 kHz – 5 MHz |
| 3 | Bunch synchronization accuracy | ~100 psec |
| 4 | Readout channels per APD | 1 |
| 5 | Number of APDs in experiment | ≤ 16 |
| 6 | Signal input width | 5-20ns |
| 7 | Signal input height | 10 – 100 mV |
| 8 | Resolution above noise | 16 bit (initially ≥12bit) |
| 9 | Readout size per APD per pulse | 16 bits |
| 10 | Calibration doubles frequency | Alternate empty / full bunches for pedestal, common mode… |
| 11 | Data bandwidth B/s/channel | XFEL: 2700 x 10 x 2 x 2 = 108x$10^{+3}$ B/s,<br>PETRA (1 bunch/rev): 130 x $10^{+3}$ x 2 x 2 = 520 x $10^{+3}$ B/s<br>PETRA (40 b/rev): 5200 x $10^{+3}$ x 2 x 2 = 20800 x $10^{+3}$ B/s |

**Table 1 APD readout requirements**

- Readout parameters shown above.
- Time lines:
  - Prototype 130 kHz, 12 bit for use at PETRA3 by end of 2010
  - 5.2 MHz, 14-16 bit for use at PETRA3 (40 bunch) 2011/2012
  - 4.5 MHz, 14-16 bit for use at EuXFEL 2014

European XFEL

# Possible ADC implementation for APD



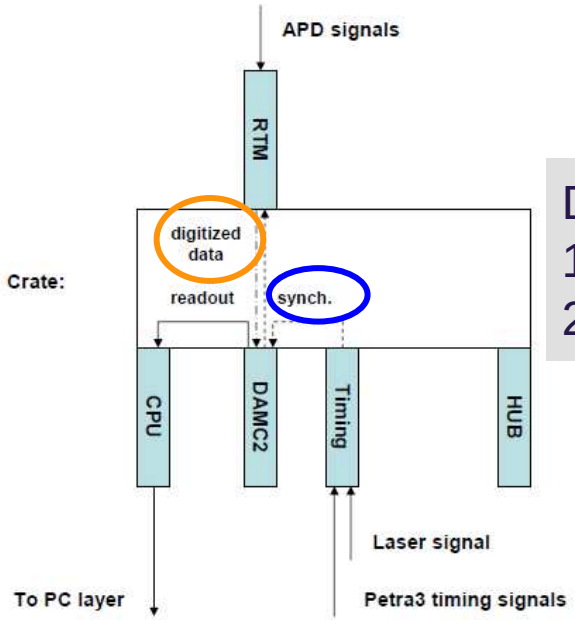
- APD pulse is relatively fast = few ns, 10 – 100 mV…
- Two candidate ADC implementations:
  - gated integrator:
    - ➔ single digitization after ~20-40 ns collection gate
    - ➔ requires moderate ADC performance (~10 MHz)
    - ➔ e.g. ZEUS luminosity monitor gated integrator
  - fast sampling:
    - ➔ multiple digitization: before, at, and after peak
    - ➔ requires faster ADC ≥100MHz and input shaper
    - ➔ e.g. Struck SIS8300 10 channel 125 MHz ADC

European XFEL

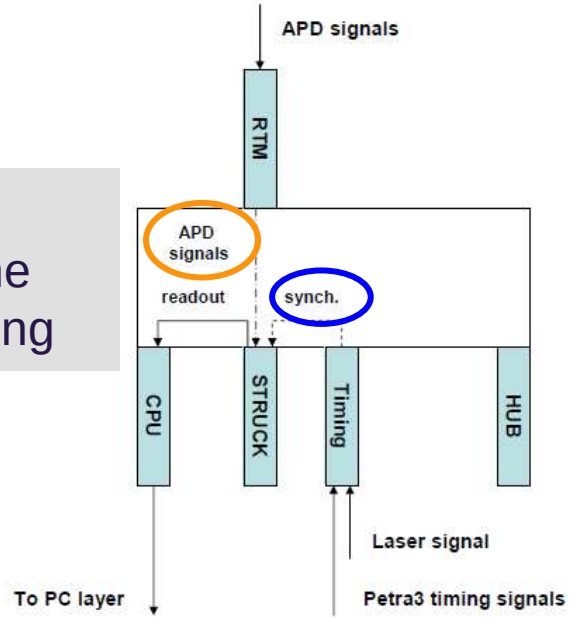
# Aimed for DAQ setup



- Use standard xTCA crate with CPU (control) and HUB (arbitration)
  - Both ADC solutions can be used, see schematic below
    - ➔ Integrator: DAMC2 + RTM (= integrator ADC)
    - ➔ Fast sampling: STRUCK (GmbH) + RTM (= shaper)
  - xTCA and DAMC2 developed by DESY-MCS and -FEA




Differences:
1. where analogue work is done
2. possibly timing signal handling

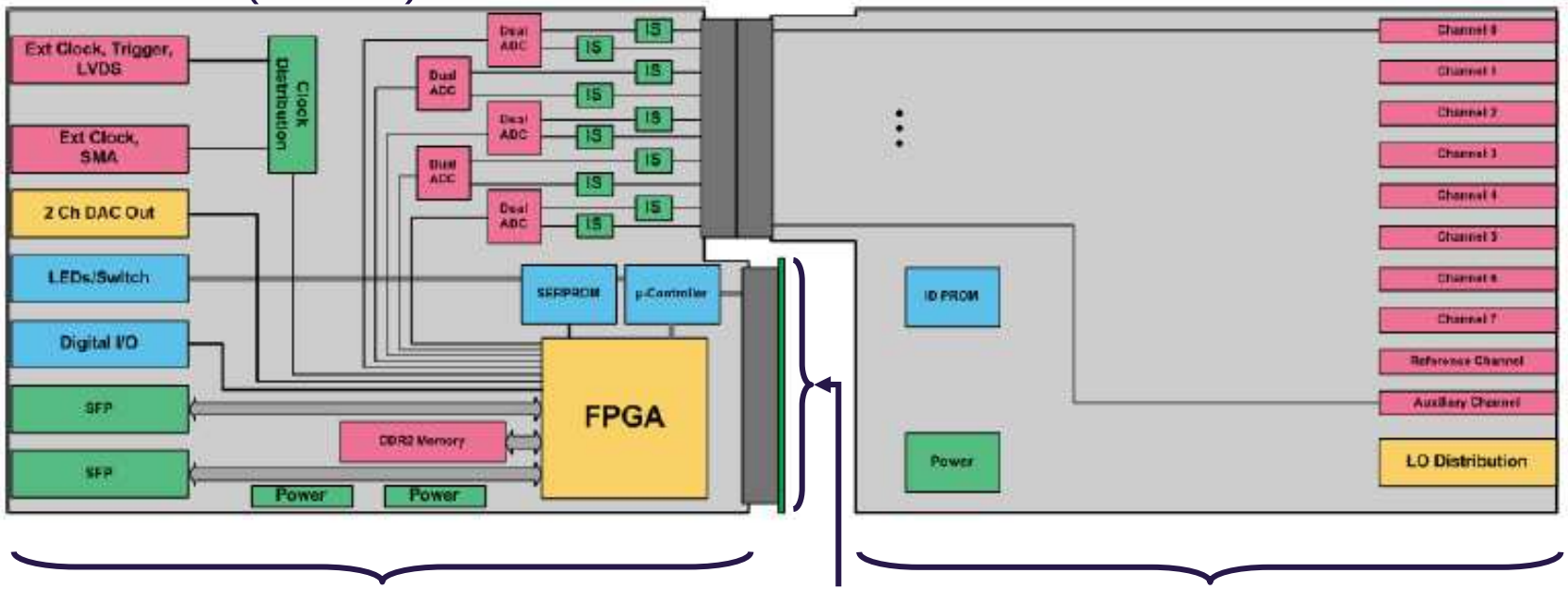


European XFEL

# ADC boards



STRUCK (shown) or DAMC2




- xTCA backplane:
  - top half open = RTM – front board connection (~54 pairs)
  - bottom half = inter front board (CPU, timing…) connection

DAMC2 = digital only, analogue on RTM = reduce noise, increase reusability

European XFEL

# ADC and FPGA developments



- ADC hardware development needed:
  - Rear Transition Modules (RTM)
    - integrator: shaper and integrator ADC
    - fast sampler: shaper (?)
- FPGA programming required (not exhaustive):
  - DAMC2
    - Digitized data capture, data processing (histogramming), and formatting
  - STRUCK
    - data processing and formatting
  - Reuse available DAMC2 or STRUCK FPGA software modules for non specific programming tasks (data transfer to backend)

# Timing development



- Timing interfaces using backplane CLK lines
  - PETRA3 PBU:
    - ➔ need to condition input signals & clocks
    - ➔ need to fine tune delays
    - ➔ need to interface to backplane CLK lines
    - ➔ PBU design not fully fixed

  } need to develop interface board

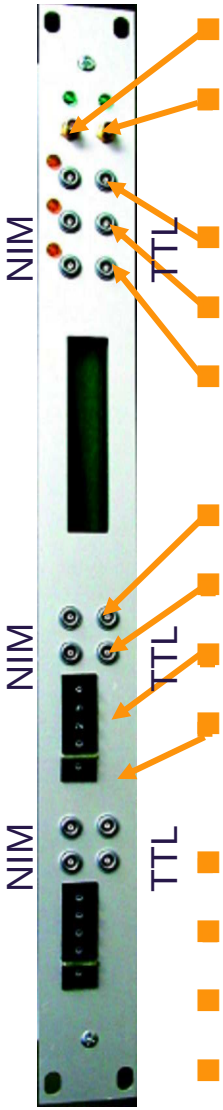
  - EuXFEL TR:
    - ➔ should be compatible with TR timing board
    - ➔ TR design not fully fixed

  } wait and see

European XFEL

# PETRA3 timing interface – PBU front (20.4.2010)






- 500 MHz reference (derived from internal 20 MHz)
- 125 MHz reference (derived form internal 20 MHz)

} clean? continuous

PBU = Petra Bunch Uhr

- Beam lost (level)
- Free

} ??Stable conditions for DAQ, is this a network message??

- Injection (2 ms level, 1.5 ms before injection)

- BC = bunch clock (for pattern defined below)

} See scope view - not always continuous

- BT = bunch trigger (= revolution frequency 130 kHz)

} continuous

- N x 1 ns offset selector (delays BT and BC)

} Timing is relative – must use offset and fine tune

- Bunch pattern (selects 1 or 7 pre installed patterns)

- BC = bunch clock (for pattern defined below)
- BT = bunch trigger (= revolution frequency 130 kHz)
- N x 1 ns offset selector (delays BT and BC)
- Bunch pattern (selects 1 or 7 pre installed patterns)

} second set – why duplication?

European XFEL

# VETO management – only one slide


- VETO = signal saying reject this frame
- What is VETO management
  - receive all VETO signals (APDs could generate VETOs)
    - ➔ hopefully all digital, but probably 2 encoding standards
  - process VETO signals
    - ➔ user Clause evaluation
  - distribute to users
- Idea: perform VETO management in a DAQ crate
  - Significant overlap with APD – have two groups working
    - ➔ EuXFEL = Dana mostly VETO FPGA and control
    - ➔ Collaborator = APD FPGA and RTM

European XFEL

# Conclusions



- Have defined two projects:
  - APD DAQ
  - VETO manager
- Both are built around the same hardware, allows:
  - WP76 to increase hardware expertise
  - Reuse and profit from machine control group's standard
  - Reuse solutions for other PBS expt. and diag. detectors
  - Hardware is new = engineer/collaborator interest
- Projects have
  - Large overlap with each other
  - Some overlap with 2D pixel projects

European XFEL

# Conclusions



- Suggest following both ADC variants:
  - As investment cost is low, see table
  - Needs ~1 FTE from WP76 and ~2 from collaborator

| Item | VETO units | APD units | Deliverable | Unit cost (k€) |
|---|---|---|---|---|
| xTCA crate + cpu + hub | 1 | 1 | ~4.2010 | 5.0 |
| DAMC2 | 1 | 1 | ≥ 6.2010 | 4.0 |
| STRUCK SIS300 + RTM | (1) | 1 | ≥ 6.2010 | 5.7 |
| Custom RTM | 0 | 1 | ≥ 9.2010 | 5.0 |
| Timing Simple Front Board | (1) | 1 | ? | 5.0 |

**Table 2 Hardware cost and date of earliest delivery**

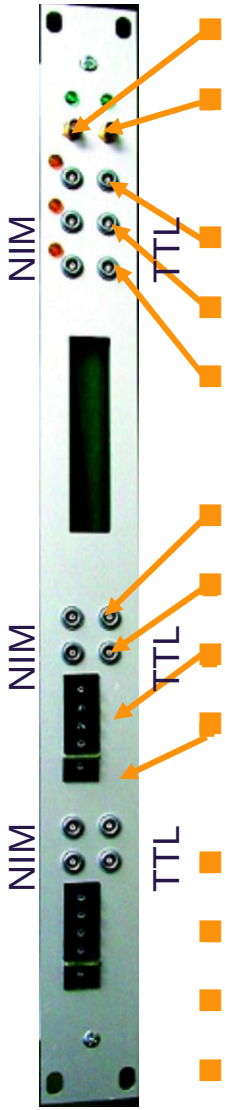
- This may need funding
  - MB should read note and endorse/reject
  - We visit our target collaborator next week

# Spare slides

European XFEL

# PETRA3 timing interface – PBU front (20.4.2010)






- 500 MHz reference (derived from internal 20 MHz)
- 125 MHz reference (derived form internal 20 MHz)

} clean? continuous

PBU = Petra Bunch Uhr

- Beam lost (level)
- Free

} ??Stable conditions for DAQ, is this a network message??

- Injection (2 ms level, 1.5 ms before injection)

- BC = bunch clock (for pattern defined below)

} See scope view - not always continuous

- BT = bunch trigger (= revolution frequency 130 kHz)

} continuous

- N x 1 ns offset selector (delays BT and BC)

} Timing is relative – must use offset and fine tune

- Bunch pattern (selects 1 or 7 pre installed patterns)

- BC = bunch clock (for pattern defined below)
- BT = bunch trigger (= revolution frequency 130 kHz)
- N x 1 ns offset selector (delays BT and BC)
- Bunch pattern (selects 1 or 7 pre installed patterns)

} second set – why duplication?

European XFEL

# PETRA3 timing interface - PBU back (20.4.2010)



- out timing signal daisy chain
- in timing signal daisy chain

- BC = bunch clock
- BT = bunch trigger (= 130 kHz)

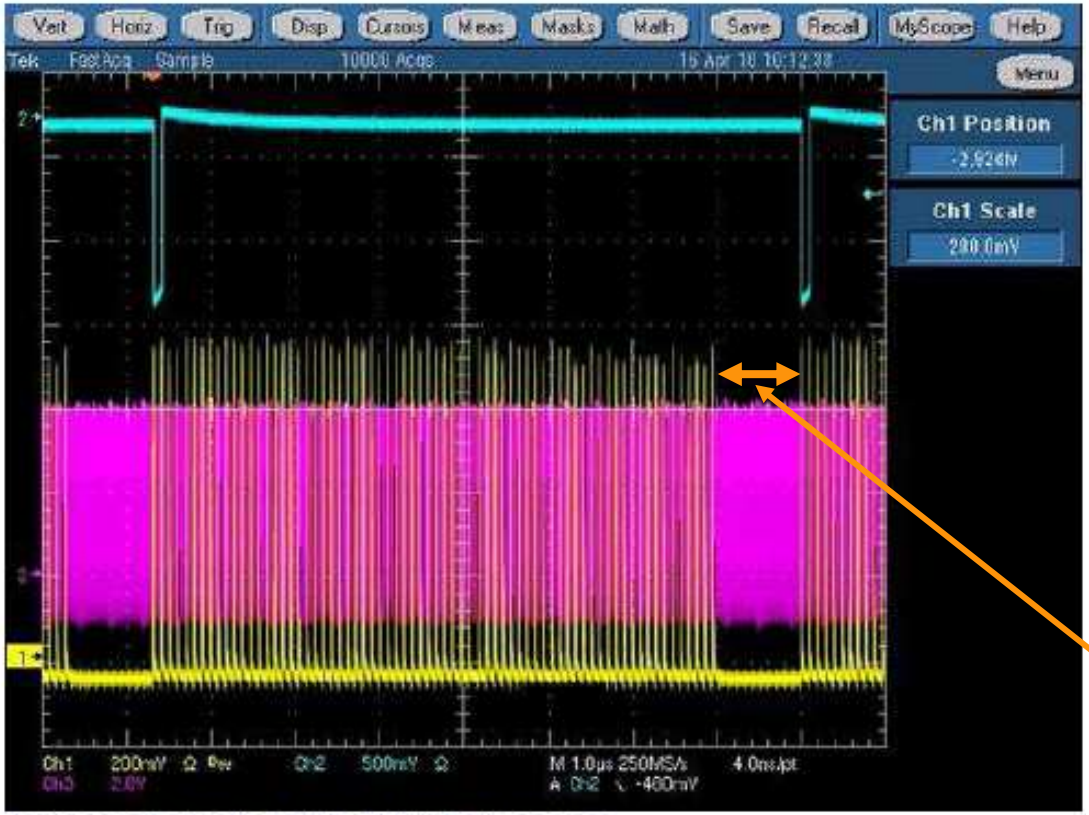
} remotely writeable

- V.24 serial port (write pattern used by BC and BT above, read pattern set on front panel and bunch count(?))

European XFEL

# Petra3 PBU – scope view 1






Screenshot of 1GHz BW TEK scope.

Ch1: beam pic-up signal of PETRAIII 70 bunch filling
Ch2: NIM output of revolution signal
Ch3: 125MHz output

yellow = BC output & not continuous

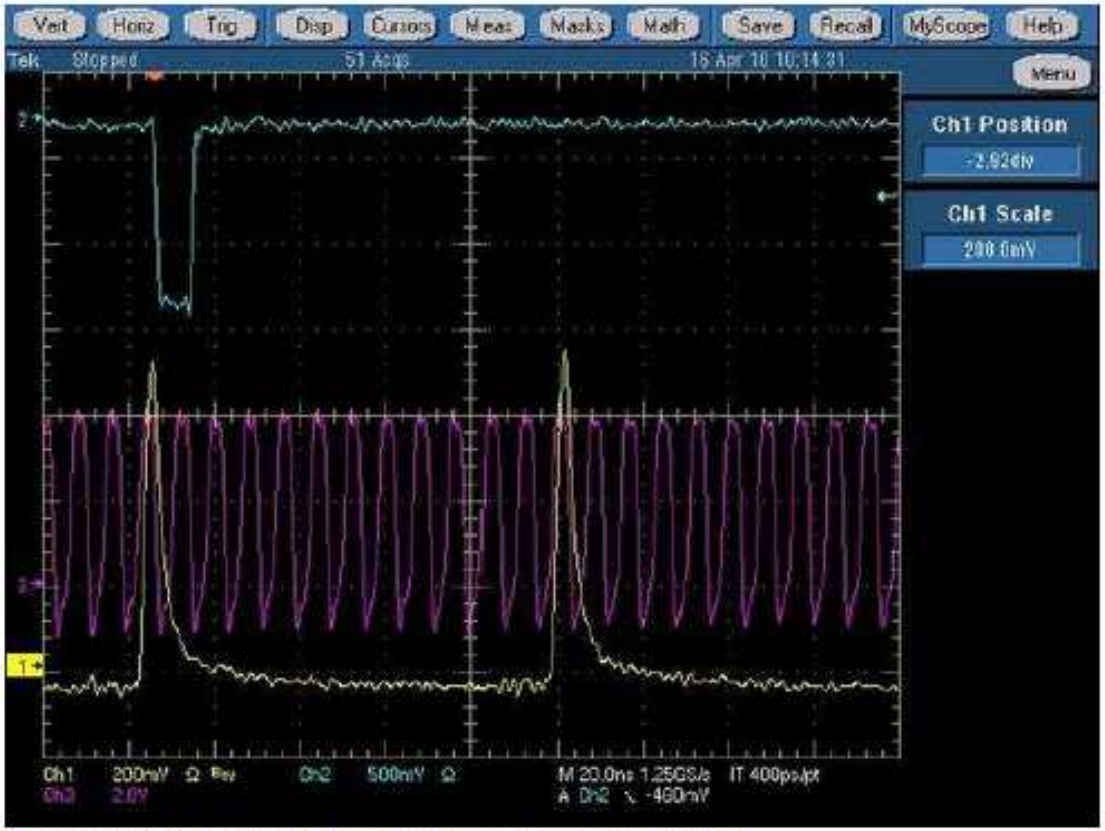
blue

magenta

European XFEL

# Petra3 PBU – scope view 2



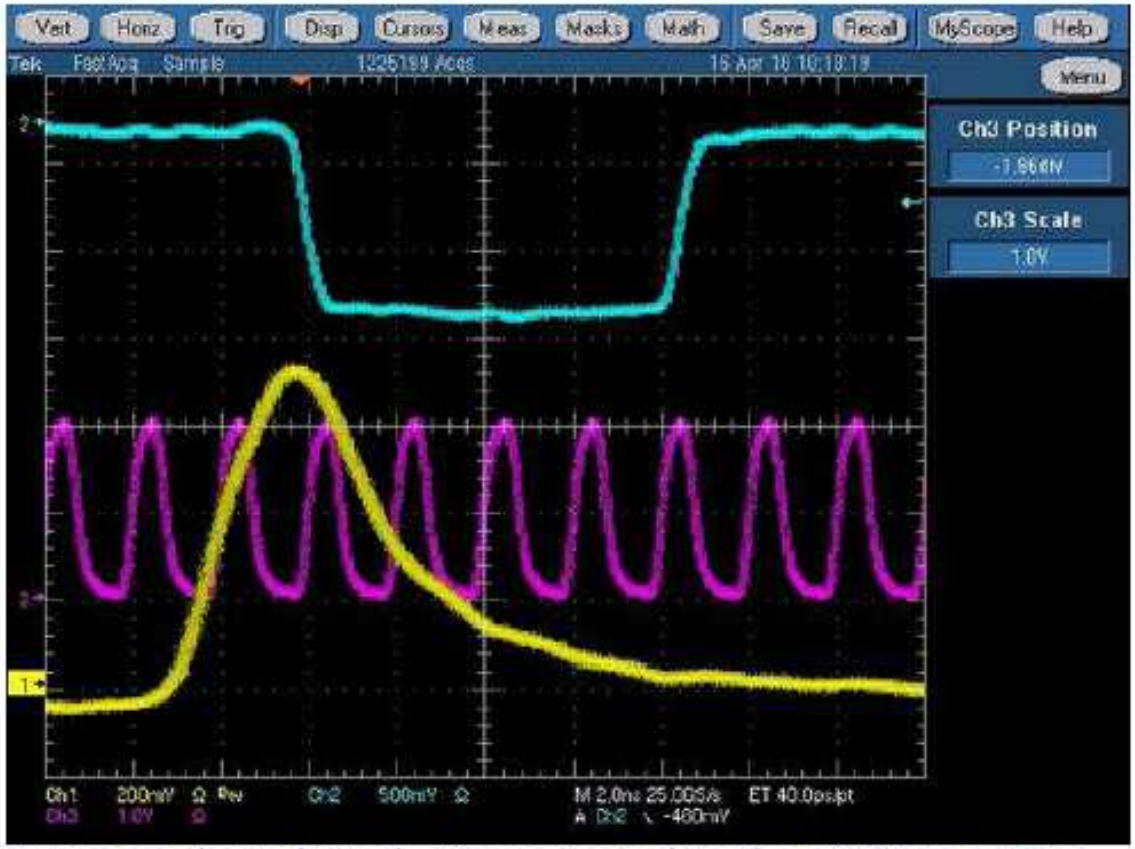



Horizontal zoom of same signals as above

European XFEL

# Petra3 PBU – scope view 3






Same as above but Ch3 is connected to the 500MHz output