Minutes of the Train Builder meeting (9.9.2010)

AER 21, Hamburg, C.Youngman (12.9.2010)

1 Attendance list

WP76: N.Coppola, S.Esanov (am), I.Kozlova (am) and C.Youngman.
LPD+TB: B.Halsall and J.Coughlan,
AGIPG: P.Goettlicher
DSSC: T.Gerlach.
UCL: E.Motuk, M.Postranecky, M.Warren and M.Wing
FEA: I.Sheviakov and M.Zimmer.
MCS4: K.Rehlich (am)
FS-DS: S.Smoljanin (pm)

The minutes, agenda and talks are reachable via:
http://www.xfel.eu/project/organization/work_packages/wp_76/daq/2d_pixel_detectors/meetings/ .

Actions are rendered bold. Items of interest are underlined.

If you do not have time or do not want to read entire document, then skip to the summary and actions.

2 Last meeting actions and purpose of meeting – C.Youngman

Last meeting action status:

- **1.** The meetings with the XFEL (MCS4) and Petra3 (Viefhaus and MSK), timing groups with UCL and WP76 took place end of June. A meeting between UCL and FEA to discuss use of the DAMC2 digital board took place at the same time. The results of the discussions are detailed in the CC talk, see below.
- **2.** The software review meeting has not taken place, see the software talk below.
- **3.** The VETO source and specification meeting has not taken place. Progress on gaining experience with hardware which will probably be used for this developed are reviewed in Dana's talk below.

- **4.** The contract for the development of the train builder was signed in July between XFEL and STFC. This means that all the contracts needed to develop CC and TB sub-systems for the planned 2D pixel detectors are in place.
- **5.** The progress report for the UCL 1st July invoice was submitted and accepted. This document will be used a template for the TB report required 1st Oct. Progress reports are required to allow payment of the half yearly instalments.

The aim of this meeting:

- Receive an update of the CC implementation following the meeting in June . Ensure that all involved parties (UCL – CC implementer, MCS4 – TR implementer, FEA – DAMC2 – implementer, TB and FEEs – CC users) agree and are happy.
- Review time schedules for TR and DAMC2 hardware and firmware, CC and TB developments and single DAQ systems. These projects are highly interdependent.
- Update FEE and TB status.
- etc.

3 Status of APD single DAQ crate – D.Wilson

The implementation of the DAQ readout and control system for Ch. Bressler's APD was explained. As reported at the last meeting we are using the STRUCK SIS8300 10 channel 125 MHz FADC xTCA AMC board to acquire and processes input from APD channels.

A RTM backend for the STRUCK board hosting 2 shaper channels has been developed with the help of the DESY-FEB group. PCB layout and component orders are now in DESY-ZE and we expect to receive a first board mid Oct. The shaper stretches the input Gaussian ~5ns input signal to ~100ns flat top using a six stage delay line, which allow ~12 FADC samples to be digitized by the ADC (aim: 12 bit accuracy in 2011 and 16 in 2012).

Kay summarized the status of the STRUCK board. He has 2 and tests are being made using the firmware provided (1 channel readout). The signal handling qualities appear to be very good and better than a corresponding VME ADC system (STRUCK statement). P.Goettlicher was particularly interested in measurements from consecutive digitisations – these results have been made available by STRUCK. The STRUCK measurements done with a sine generator and internal trigger.

The aim is to use Kay's TR board to interface the DAQ crate to the Petra 3 PBU timing signals with NIM/TTL to LVDS signal conversion.

The chassis will be provided by the xTCA for Physics Picmg MTCA.4 standard development by the MCS4 group. Delivery of the CPU and disk shoe required 2-3 weeks, the MCH 6, and the chassis Since last week we have been testing with a Suse 11.3 kernel (thanks Sergey). Some small problems are seen (DHCP behaviour) but nothing serious – early days however. The cost: crate 1545€, CPU 1382€, MCH 2142€ and disk shoe 324€.

In principle the MCH should self configure w.r.t. AMC boards installed in the crate, if not you get an extensive log. This can happen if the board's description is incorrect. The AMC board description is programmed by the manufacturer (eprom?) – MCS4 can help with boards we are developing (e.g. IPMI code adaptable to the configuration of the board) – we should contact Kay when help is needed. RTMs do not require a program just a table of parameter values.

Next steps:

- Continue working/understanding the crate setup

- Receive the STRUCK ~beginning Oct
- Test with the STRUCK without RTM
- Receive first RTM ~mid Oct (smoke test, tune shaper…)
- Receive the TR ~end Oct
- Work on APD specific firmware of the STRUCK (sum 12, correct pileup, calibration…)
- …
- Bressler needs working system Feb 2011.

The project is on schedule, no show stoppers are seen but a lot of work is required, it is an implementation that can be used in the projected VETO system, CC and single DAQ crate project have significant overlap.

4 C&C status – E.Motuk

The meetings held in June provided information about the TR, DAMC2 and xTCA crate delivery schedules and capabilities. This was required to finalize the hardware implementation of the CC. The meeting with the Petra 3 timing group provided insight into non XFEL CC usage. The conclusions from these meetings were:

- TR card will provide clocks and triggers to CC over the XTCA backplane
- XTCA backplane sufficient for CC functionality
- Bunch clock (4.5 MHz) and 99 MHz clocks will be provided on low-jitter, P2P lines (TCLKA/B)
- DAMC2 can be used as a base for the CC card which can be a master or slave.
- A custom RTM can be designed for CC master and slave functionality

The UCL group will pursue this hardware implementation, should additional functionality not provided by the custom RTM an FMC mezzanine can be used with the DAMC2. In the mid- to long term an upgrade of the DAMC2 board is foreseen which will provide the functionality of the custom RTM (making it redundant?) and, importantly, allow the DAMC2 to distribute TCLKA and TCLKB p-2-p clocks.

The backplane signal usage was shown along with the board occupancy of a 12 slot crate.

- The machine protection card shown in the CC crate is not required; it was inserted as a place holder at a time when the functionality of the MPS was not understood. It may turn into something else like an interlock or used to receive the MPS status?
- This crate could support the connections required for 6M pixels. The RTM is a double height unit, the DAMC2 single (remember in TCA height = width).
- Each DAMC2 can drive 1M pixels.
- xTCA physics slots are mid-size.
- On the CC (master RTM not same as slave?) RTM onboard oscillator and PLL with provide the 99 and 4.5 MHz clocks used when running standalone.
- Backplane bussed LVDS signals were defined (RX17-TX18 TR to CC master; RX19-TX20 CC master to CC slave)
- CC master will interface to Petra3 using the TR (will need firmware)
- The telegram content sent by the TR was defined (start train, train #, end train, bunch pattern index and DAQ ready)
- The telegram handling uses 2 bussed lines (content and strobe)

Current status:

- A design of the firmware blocks required (see diagram) has been made.
- Virtex 5 development board delivered for firmware prototyping and development of small daughter boards where RTM functionality can be tested.

- Two daughter boards being designed: version A) simple RJ45 IO for receiving commands and 99MHz clocks, B) for standalone clock generation and TR interface tests.
- If the DAMC2 were to be available soon a full size RTM would be designed rather than B.
- Tests with A have been made for command handling (since last meeting) and the results are good. All signals from the CC are AC coupled at the receiver end. The same AC coupling used on other signals will be used for the status. The detector head end driving the status has its own ground, i.e. not that of the CC.
- Scope views of the start and stop messages generated were shown.

The schedule was shown.

Outstanding issues and discussion:

- Telegram data protocol – the data and strobe line solution is acceptable UCL are asked to produce an IP core to do this – UCL agreed to provide receiver and sender at 108MHz. No crate user is known to have a problem with allocating two lines.
- DAMC2 update CC and availability schedule – new vendor for PCB production found who are interesting as they offer new technology = lower cost. Expect first board next week for soldering thereafter firmware testing starts. Anticipate if problem free DAMC2 for end users in Nov/Dec. The schedule for the next version of the DAMC2 (e.g. with TCLKA/B drivers) was discussed and Autumn 2011 was envisaged. 20 PCBs and there components will be available in the first charge.
- RTM design specs and grabbing existing power, IPMI implementations – Kay's response: circuit diagrams, schematics, power supply implementation examples, IPMI, etc. are available and can be used by Cadence users where they are not available as spec files – please ask.
- Crate availability: 12 slot – 4 weeks from Schroff and 8 weeks from Elmar. The 6 slot crates are deliverable now from both vendors (Schroff's prototype price is realistic).
- TR issues – hardware end of Oct, thereafter firmware. The 99Mhz can and will be done and it is continuous on TCLKA or B.
- MCH issues – NAT is prepared to provide a clock multiplexer with jitter ~few ps for xTCA for Physics.

The points on the UCL statement list were ticked off. Conclusion: all open issues are resolved, a sensible work plan exists and the schedule looks OK.

5 LPD FEE status – J.Coughlan

Current status:

- ASIC submitted July part of CERN multi wafer run. Expect 6 wafers in Oct.
- Super module test using x-ray source will happen Jan. 2011 – no requirements for CC hardware made.
- FEM interface card – layout require 3-4 weeks for routing, then review. Hope to have boards by end of year (6 ordered, solder 2). Component order and PCB manufacture are running in parallel, subcontracted out. Schematics of the FEM were shown.
- Currently producing test cards to use when FEMs are available.
- Good progress on the firmware continuing from the work of Sam – prototype design for the data receiver working (gain selection at 512 frame rate) and tests passed.
- The FEMs CC interface is there – looping back Sam's logic is not needed immediately, do when sensible.
- Work to do includes: linking up the IO (Spartan) and processing FPGAs (FX100), length matching on memory interface, grounding, etc.

- An IO expert from Xilinx will visit next week to look into the problems of driving bigger (wider) memory (blocks) seen during TB development last year.

On schedule and no show stoppers seen.

6 DSSC FEE status – T. Gerlach

Current status:

- The problems with the 10GbE PHY (same smaller less functional version which is no longer available) reported at the last meeting still exist. Loopback connection between PHY and PC can be established, but not between FPGA and PHY. The PHY status registers contain strange content – no description received from the vendor. Hardwiring RX to TX fixes the problem. Eye diagram with standard XAUI MGT parameters looks bad and is improved using pre-emphasis settings (a designer at HD had experience setting – signal ramp speeds, filtering, etc. – these in an earlier project) these look better, but do not indicate where the error is. The chipscope tool has not been used.. Suspicion is that PHY is damaged and a new PCB is expected in a few weeks – hopefully this does not show the problem.
- The PLL on the 10 GbE prototype board is now working. More investigations are required to optimize the output signal.
- Currently working on the IO-board-1connecting sensor side vacuum board to DAQ board. The board hosts a Spartan6 to control the power system (power down between trains), serialization of data from the 16 sensors stream to the DAQ board, high speed fanout buffers, etc. Schematic almost finished, layout soon.

Some problems exits but these are not thought to be critical. Plan to have a full test of the hexagonal pixel structure with IO-board by end of the year.

7 AGIPD FEE status – P.Goettlicher

Current status:

- Now that the CC implementation has cleared there are few issues w.r.t. that side. All FEE relevant issues are solved.
- No changes have been made to the design including what the micro-processor is required to do. Downloading FPGA firmware from the micro-controller to the FPGA will be implemented by Igor (jTAG over Ethernet?). Should anticipate downloading different firmware according to user requirements.

Conclusion: no recent changes therefore no show stoppers seen.

8 DESY-FEA 10GE, DAMC2 and AGIPD status– I.Sheviakov

Ethernet frame errors were seen on the dual 10GE link FMC board delivered to STFC in May. The faulty module was tested at FEA today and indeed errors are seen. Believe that the problem lies in the parameter values used (MGT) which are currently the defaults – will investigate and fix accordingly. Rob has been given the other working board and will test it tomorrow.

DAMC2 has been discussed in detail above. Firmware modules to be delivered with the base board are: PCIExpress, Gigalinks, µRTM interface and FMC. They are delivered on a best try basis, if problems are found the users will have to report them and fixes developed. The users themselves will have to develop there own modules. A number of test boards are being developed including a simple RTM (include IPMI, power… - by end 2010) – maybe this board is of interest to the CC group.

The status of the AGIPD FEE readout interface board was shown. Design and component identification has started with the aim of having a PCB by March 2011.

9 Discussion of Medipix3 usage of TB

AGIPD and Medipix3 readout requirements have a number of similarities: data input circuits, memeory usage, use of 10GE links, etc. At Petra 3 the Medipix runs as a counting detector with no bunch structure. We are asked to discuss and come to a conclusion on whether the TB can be used to funnel data to the backend processing/storage level.

Sergej Smoljanin (from Heinz Graafsma's detector group FS-DS) gave details of the Medipix requirements. The intension is to use 6 modules which could use the TB functionality of building multiple modules a single module could be handled by going directly into a PC using UDP. The timescale is a working one module detector by Dec 2011.

Sergej was requested to provide a readout specification (which he did immediately after the discussion concluded). This would be looked at in detail offline (implications for TB and CC systems) and a decision given to Heinz.

10 TB status – J.Coughlan

As mentioned above the MoU and TB contract were signed in July.

TB demonstrator µTCA card schematics should be ready end Sept. Review design beginning Oct. Changes since the last meeting: power distribution and its components, configuration of FPGA will use "Platform Flash XL" (recommended Xilinx soln. not same as on FEM which was too big for this board), adding more temperature monitoring (e.g. shutdown internal to board), added Atmel microcontroller connections and routed all available lanes to the backplane via the X-point switch. The board, double height and full size AMC, adheres to the TCA mechanical spec.

STFC will gladly take up Kay's offer of help w.r.t. IPMI programming.

HiTech Global is selling a dual 10GE FMC using a Network Logic PHY, but it is still intended to use the FEA version.

Need addressing:

- The number of PHYs needed should be reviewed – do we have enough.
- By the end of the year 2 more FMCs will be required for FEM testing.

The final form factor, µTCA or ATCA, was touched on. An ATCA project has started at STFC which will provide useful feedback. The discussion started at the last meeting was rather speculative.

11 FPGA firmware and Xpoint switch status – Rob Halsall

Over the last month have been working through feasibility tests using a series of development boards. Testing on the prototype FEM and TB demonstrator board are the next targets.

Programming of the DAQ firmware is being worked on. Configuring all peripherals using a simple 32bit bus readout has been done, can: start runs, transfer data through, funnel data from 128 asic FEM.

The following data transfer protocols were assumed in the initial TB design:

- FEE to TB: UDP (without retries as error rate ~10**-15bits) or custom
- Inside the TB: aurora
- Between TB and PClayer: initially UDP (without retries) and later TCP

Rob is working on the FEM to TB protocol which looks like “reliable UDP”, Rob called it “Local Link UDP” i.e. 8k transfers with retries and a simple XON/XOFF control and probably timeouts to identify no transfer when expected type error conditions – this is custom in the FEE to TB definition above. This is new and provoked some discussion. Aim is to take MB local link frames and transport them from FEM FPGAs to TB FPGAs which requires breaking the blocks into smaller packets (which could be UDP). Is the new protocol PGP? The expectation of using classic UDP has to be kept or do the other FEE now have to implement this, or do they have to provide there own UDP modules? As no conclusion was reached, Rob will continue and see whether the approach is tenable and what the implications are for the other FEEs. Why use a UDP wrapping protocol instead of using classic UDP? More discussion will be required.

Other questions that came up were the data reorganization capabilities to optimize the data arriving at the PClayer. Can the TB reblock the data from being module blocks to be image blocks.

The list of planned work was shown.

Conclusion: work progressing and on schedule for FEM and demonstrator. The FEE to TB transfer protocol work caused some discussion – the implications for the other FEE and PClayer might be interesting.

12 Software summary – C.Youngman

The software status has not moved significantly since the last meeting we are still trying to implement our software into a demo on two live systems XCAM and the single crate DAQ systems. Work continues.

13 Summary of meeting

The results of the meeting:

- The CC hardware implementation has been finalized and all groups involved agree. A single DAMC2+RTM system capable of controlling 1Mpxl is the initial target.
- An upgrade of the DAMC2 (including CC requests) is anticipated Autumn 2011.
- DAMC2 test RTM boards might be interesting for the CC group.
- The TR should be available end Oct.
- The DAMC2 should be available Nov/Dec.
- The single DAQ crate using xTCA is progressing
- Problems with 10GE PHYs exist. DSSC may have a damaged PHY on there PCB. The FEA FMC generated frame errors when used at STFC – parameter tuning is expected to solve the problem.
- FEE design is progressing (LPD FEM available end 2010, AGIPD interface PCB March 2011)
- The TB demonstrator is on schedule (end of 2010)
- The FEE to TB (and TB to PClayer) protocol is being worked on, caused and needs discussion.
- Groups needing to program board IPMIs are asked to contact Kay for support
- Power and other implementations for RTM can also be acquired from Kay.

14 Actions

The list of actions:

1. **Get consecutive digitisations measurements made by STRUCK.**
2. **Send the cost of the single crate DAQ xTCA for Physics equipment to Matthew – see text Section 3.**
3. **A decision is required from UCL on whether they can provide the firmware modules for sending and receiving over the telegram data and strobe lines.**
4. **An offline discussion and decision concerning the possibility using TB and CC for Medipix3 is needed.**
5. **Manfred should retransmit the list of number of PHYs ordered by which group. The groups should send back an update of the numbers requirted.**

15 AoB

The next meeting will be held at STFC on 20.Jan.2011 (date to be confirmed).