Minutes of the Train Builder meeting (18.2.2010)

AER 5.21, C.Youngman (last revised 22.2.2010)

1 Attendance list

WP76: N.Coppola, S.Esenov, D.Wilson and C.Youngman.
LPD+TB: B.Halsall and J.Coughlan.
AGIPG: P.Goettlicher and L.Steffens
DSSC: A.Kugel (telephone/EVO).
UCL: S.Cook, M.Postranecky and M.Wing.
FEA: I.Sheviakov and M.Zimmer.
KIT: M.Balzer and D.Bohrmann.

The minutes, agenda and talks are reachable via:
http://www.xfel.eu/project/organization/work_packages/wp_76/daq/2d_pixel_detectors/meetings/ .

Actions are rendered bold. Underlining of text is used to highlight: sub-sections, answers to actions, and points which are not actions.

If you do not have time to read the text fully, then skip to the actions section.

2 Introduction – C.Youngman

The following points were addressed in the introduction slides:

- Status of contracts. The contract with UCL for CC development was signed in Dec.2009. The contract, which replaced the in-kind funding mechanism, for the TB development is ready. The UK pull out as a EuXFEL shareholder at the end of Dec.2010 is a complication, a memorandum defining funding is being produced – both sides agree to proceed with development.
- Website. WP76's website http://www.xfel.eu/project/organization/work_packages/wp_76/ is new and usage tips are given on the entry page.
- Mailing lists. TB and CC related mail lists have been created: xfel-wp76-tb@xfel.eu, and xfel-wp76-cc@xfel.eu. These should be used for sending emails to the

addressees concerned. The lists are private (user subscriptions are not allowed), to get onto the list follow the instructions on the entry webpage. The address list can be seen from the entry webpage. **Please check that the mailing lists are complete and correct.**

- Single crate DAQ development. WP76 has started trying to organize the development of a single crate DAQ system for use with experiment and diagnostic instruments with lower DAQ performance requirements than those of the 2D pixel detectors. The slides show: a showcase experiment, similar developments for the LINAC machine, and some initial conclusions. Matthias Balzer and Dietmar Bohrmann, from Karlsruhe Institute of Technology, are currently investigating collaboration projects within the single crate DAQ development. Feedback to and from the 2D-pixel and single crate DAQ are likely, e.g. LINAC groups at DESY and SLAC are trying to standardize timing receiver and machine protection systems (time scale ~2 years?) which will be interesting. The single crate DAQ could also be a provider for VETOs, see comment immediately below. The next weeks should be used to clarify this development.
- The aim of meeting. As always: to review the status, check the time schedules, find and close open questions, etc.
    - One interesting point is that data from LCLS is now available for 1Mpixel detectors, e.g. CAMP. **N.Coppola will provide feedback w.r.t. non lazing pulses and other potential vetos and details of data reduction and processing (correction) from CAMP at LCLS. A brain storming meeting is being planned.** This is interesting for the 2D pixel detectors and for checking assumptions made in the computing TDR.
    - **UCL's requirements (when and what) for access to Timing Receiver boards has to reviewed as K.Rehlich does not have many and they have some interesting features.**

3 Actions list from last meeting

1. The ability to remotely download firmware (ASIC and FPGA) and reset systems when hung needs addressing – this capability should be a requirement for all detectors. All detector FEEs should send me a statement about how they currently plan to accomplish this in the next weeks.
This point is answered in the FEE status report below.

2. The LPD FEE group should state their requirement w.r.t. the input veto signal to their FEE. Either the old 5MHz yes/no, or 100MHz with bunch number encoding and a low (specified) latency requirement. As update work on the C&C specification is underway, the statement needs to be available within 2-3 weeks.
The requirements from the different detectors are:

- LPD want a synchronous fixed latency VETO clock, this can be 4.5 (yes/no) or 100 MHz (encoded bunch number).
- AGIPD want the 100 MHz VETO clock with encoded bunch number. They do not need it to be synchronous with the 4.51 MHz bunch frequency.
- DSSC want the 100 MHz VETO clock with encoded bunch number. They do not need it to be synchronous with the 4.51 MHz bunch frequency.

What the CC provides needs to be written into the spec so that the FEE groups can shout if incorrect.

3. The C&C group should quickly state what lower frequency bound they need – communicate this to the rest of us so that Kay can be informed. I assume that this has to be done within the next 2-3 weeks.
This is addressed in the CC status talk.

4. The FEE groups (ASIC…) are asked to make a statement about a whether 4.5MHz bunch clock is acceptable. Please send an answer to me by 6th Nov.
This was done and 4.51 MHz bunch clock is now an XFEL design number.

5. Martin and Dana will provide an updated definition of the C&C fast and network interface (protocols, content…) within the next 2-3 weeks.
This was done, see comments in the CC status talk. **The CC fast signal spec is now on the website.**

4 C&C status and fast signal definition – M.Postranecky

Fast signal definition and implementation changes since last meeting and video meeting:

- 4.513889 MHz clock is the bunch frequency
- 99.305558 MHz will be distributed to the FEEs (i.e. 22 fold multiplier)
- CC will provide individual programmable delays on fast signal lines, using the ODELAY feature of Xilinx FPGAs, for fine tuning. This applies to fast signals of fanin and fanouts. The ~500 microsecond delay range is sufficient as FEE magnetic-decouples are no longer used. Note that an overall, global, delay will provide the initial timing in of the detectors.
- Two signal coupling alternatives now exist:
  - AC coupling with Manchester coded signals.
  - LVDS repeater system (used by ATLAS down the corridor from Martin at UCL). This will be tested in the next 4 weeks – if OK it will be used.
- The START train message's 32 bunch ID content will be decided later, it can be:
  - Derived from the train number distributed by the timing receiver board, or
  - A incremented counter starting from zero (requires storing start train number ID from timing system at counter start)
- **Uncertainty still exists regarding the number of bits in the train number distributed by the timing system. The same applies w.r.t. the machine protection system – needs resolving**.
- The CC system is aiming for 100 picosecond timing accuracy.
- Fast signal commands VETO and a NOVETO exist. The VETO contains the bunch number to be vetoed. The NOVETO contains the current bunch number of the train.
- The fanin signal will be 100 MHz and it is foreseen that information can be encoded on it. The AC coupling scheme used will be the same as for fanout signals. The state is kept at the fanin side.
- The lowest frequency for the external clock will be 750 kHz.

Details of the prototype board being designed and the connectors to be used were shown. Testing of the PLL circuit using an ICS evaluation board is being made.

There was a discussion of the quality of the RJ45 cable to be used for the 5 m needed. The outer shield will be connected at the CC end (this needs to be inserted into the spec).

In conclusion, everybody agrees about the definition of the CC fast signals. A brain storming VETO meeting to understand what VETO generators there are and their latencies is planned. The VETO will be important at XFEL.

5 C&C work schedule update – M.Wing

The contract with XFEL has kept the starting date of Oct. 2009, but the contract was signed in Dec so some slippage has occurred. The advertisement for the engineer is out and the earliest that the position can be actively filled is 1st April. In the meantime work will continue without the engineer. Some rescheduling may be required w.r.t. to the original time schedule Master and Slave prototypes were envisaged at the end of 2010 – this is likely to slip till March 2011. We need to know if slippage in the detector rollouts will allow this. The answer was that this was probably the case – the FEE groups would check and give feedback. Chris and Mark will coordinate this during the next few weeks.

6 Software status – C.Youngman

An overview of the software being developed for 2D-pixel detectors was given. The tools used and the aimed at roll out (Step 1 "2D system" and Step 2 "XFEL wide system") were described. Look at the slides for details.

The DAQ and control system foreseen for the 2D-pixel detectors is characterised by:

- Sub-systems of the experiment communicate through a message hub, using reliable transport protocols, with a known content (e.g. XML…), a single message definition schema, and uses a publish/prescribe delivery model.
- Messages to and from external providers are interfaced via gateways.
- A local database is used to provide and store experiment specific configuration information. This database is periodically synchronized with a XFEL wide principle database.

A number of developments for Step 1 have been made:

- The connectivity architecture has been defined.
- The messaging system frame work to be used has been designed and implemented.
- The log4j logging system will be used.
- Work on connecting hardware has started.
- The configuration of the system using databases and the messaging system is designed and implementation work has started.

The following talks of Sergey and Dana address some of these points in more detail. The aim was to show a working test system at the meeting, unfortunately we were too late but hope to have it available shortly.

7 FSM, configuration and RC – S.Esenov

Details concerning the implementation of:

- the RC model,
- the XMS messaging system,
- the Finite State Machine (FSM),
- database connectivity, and
- connecting HV hardware,

Were given – check the slides for details.

8 AGIPD micro and software intergration – D.Wilson

Described work on the ARM micro controller with the AGIPD FEE people, the interest of WP76 in this is to get hands on experience of the FEE systems planned to be used and include at least a few of these in the software development explained in the previous two talks.

Based on the system requirements, Phytek LPC3250 evaluation boards were purchased. It is intended to use the system with Linux (= open source and flexible development environment) which will be network booted and use NFS to serve any file systems required. FEE side I2C and GPIO lines will be used to configure and readout controlled devices and communicate with the FPGA receiving the CC fast signal information, respectively. More details concerning the 3250 are given in the slides.

The following issues have been investigated:

- Setup and configuration of the linux system. Using TFTP (same subnet limited) the system boots from the network. NFS mounting of file systems was also tested successfully.
- Code development environment. LTIB and a cross-compiler are provided as part of the linux installation for coding.
- Interrupt handling and notification to user space programs. A compact kernel module was written to catch interrupts and the send_sig_info() kernel call is used to start a user space program to handle the interrupt initiated action. Typical interrupt-to-user latencies of ~200 microsecs were measured (using a signal generator and fast scope). The maximum rate of interrupt handling by the 3250 was 600 Hz – well above the 30 Hz requirement of XFEL operation. Operation with higher train rates (i.e. at LCLS) will need a modification in the working model.
- Network performance and context switching performance. The 100 Mbit/s Ethernet link was tested – no surprises were found and the throughput as a function of block size was as expected. The context switching times were measured using the Imbench suite – switching times of 150-200 microsecs with little dependency on number of tasks running were measured.
- Messaging and integration into the Step 1 software environment. During the last few days work has been done of porting Step 1 code to the 3250 – it offers a non Java environment. This work will be finished soon.

WP76 will use the 3250 as a testbed, but will perform no further development work w.r.t. AGIPD – at least until AGIPD are ready to test the FPGA-to-3250 connection (to drive the interrupt properly).

Points which arose during discussion:

- **The boundary where WP76 software development ends in the FEEs has to be defined**
- **The FEE groups have to be brought into the software development discussions.**
- Where are the boot- and file-servers located? On CC or RC CPUs.

9 LPD FEE status – J.Coughlan

The development towards a super module (= 1/16 LPD):

- Mechanical design on time
- ASIC submission in May with testing in August(?)
- Super module test with link planned Q4/2010

More realistically the March 2011 CC slippage could fit the super module availability – however some modules will be available for readout testing by the end of the year.

The FEE FEM interface card design is progressing – want to have the board available by the end of the summer so that it is debugged and working for the module tests above. Schematics and layout designs are being worked on. **The design of the CC physical interface is required to fully design the LPD FEM. The solution needs to be tested and accepted by all user FEEs – Martin will do this within the next month.**

Firmware download and reset functionality are now understood in principle. Firmware for the microprocessor, data processor… (i.e. where user updates may be required) will be updatable via the network and a reset by the CC fast signal line is foreseen. Network firmware updatability does not include IO only type devices. The LPD detector is guaranteed to power up into a workable state!

10 DSSC FEE status – A.Kugel (for T.Gerlach)

Thomas is ill and Andreas gave the presentation.

The marked in red items on the Ladder-Transceiver layout slide were question marked, the answers are the control network protocol should be TCP and the data link protocol can be UDP or custom FPGA-FPGA.

The possibility of generating an internal STOP when the maximum number of pulses to be stored (or which can be sent through the TB) is reached was discussed – it was not really possible to come to a definitive decision as the gain seemed unclear. It was left open to the FEE to decide what to do!

Coding of the FPGA to drive the DSSC 10GE link is ongoing – this development does not use Igor's work. Testing against a PC 10GE NIC using the system implemented for Igor could be made available – Thomas should get in touch to see what can be done for 10GE PC tests.

The CC fast signal specification note has not been objected to by any of the FEE groups. The modifications decided during this meeting to the content (NOVETO to include the current bunch number, specification of the bit order to be used in transfer) will be inserted and the note put on the website. Modifications to the implementation (LVDS repeater) will be published when made – hopefully in 4 weeks. This note can now be used as input to FEE FPGA programming.

Downloading firmware by the network interface is foreseen – firmware is uploaded into the "design Revision Control Logic". The status of handling the reset from the CC fast signal is not known.

11 AGIPD FEE status, micro, 10GE – P.Goettlicher, L.Steffens and I.Sheviakov

One file with three talks - contents are:

- Mechanical concept (PG). AGIPD may go to 16 for CC fast signal and 20 for Ethernet slow control. This modification is driven by the mechanical design of >1Mpxl detectors – is the maximum 8Mpxl?
- Clock rates (PG). No new requirements w.r.t. CC fast signals.
- A reminder: control concept (PG). A reset on the CC fast signal line is caught by the FPGA and will be sent to the micro (3250). A reset transmitted by an Ethernet message to the micro can be sent to the FPGA. The micro-FPGA exchange will use GPIO lines and an, as yet unspecified, protocol. The remainder of the slide is known.
- Slow control concept via Ethernet (PG). Downloads of user firmware can be expected per experiment. Download of configuration parameters might happen per run – at least a check must be made that the configuration (and firmware) are correct. All writable configuration information should be readable and therefore checkable.
- Firmware management for microcontroller via CC (LS). Operation of the micro requires: a DHCP server, a boot server and a NFS file (different directories per micro) server (i.e. by the CC or RC PCs). The file sizes for configuration are likely to be large (many tens of MB).
- Firmware management for FPGAs via CC (IS). The firmware downloading scheme of AGIPD was described. The bottom line is that the requirement of network downloadability will be provided although discussion is still required. Internally two parallel implementations exist: a SPI micro channel and a FPGA JTAG chain.
- 10GE status (IS) Some modifications to the connector pin allocations have been made to be compatible with recent evaluation boards. The first 4 FMCs should be delivered in the 1st half of March.

12 TB status – J.Coughlan

The status of the demonstrator board, a ¼ TB prototype, was presented. The baseline layout shown on Oct. has been reorganized: FPGAs and memory banks have been moved to provide space for the power and clock systems and improve cooling, and the cross-point switch has been moved to the backside and positioned to

allow short and long connections testing and more links to the FPGA. Serious layout work will start soon, most components are available onsite. Programming support for the final microTCA boards will be looked for and welcomed.

The memory rate measurements shown at the last meeting were summarized. The nominal maximum data transfer per FEE-TB link is 5.37 Gbits/s (= 1/16 (Mpxl) x 2 (B/pxl) x 512 (frames/train) x 10 (Hz)). Each input side FPGA receives 2 links, the FPGA's r/w IO memory rate is 4 x 5.37 Gbits/s (= concurrent r/w), use of 2 memory banks halves the total memory I/O required per bank to 1.28 GB/s, which is less than the 1.8 GB/s measured on an evaluation board. No show stoppers are seen. Including header information will reduce throughput slightly. Transferring small block sizes across the switch during formatting should be avoided by suitable frame formats.

Bottlenecks limiting throughput will arise in the following order: memory, input links, and finally the switch. The demonstrator board will allow tests of the final concept; no evaluation board exists with all the required features, including data formatting issues. Other comments: Vertex 5 = DDR2 and Vertex 6 = DDR3. 30 Hz XFEL operation = 512/3 frames per train throughput.

13 TB FPGA and cross point switch status – R.Halsall

Work continues using evaluation boards to test key aspects of the FPGA implementation, see work list in slides. Currently the XAUI-Aurora-Xpoint is being investigated. A PCIexpress/SFP+ board is ordered and will allow testing of XAUI to 10GE PHY connections. The demonstrator board will provide the final test environment including microTCA functionality including powering requirements.

Discussion: Expect Vertex 7 will have ARM hard cores rather than PPC. Using a Vertex 6 was considered, but will stick with the Vertex 5 (for now).

Devices requiring firmware for a TB board were shown… In summary no show stoppers are seen.

The memorandum for continued funding is required for financial year 2010, i.e. by 1st April.

14 Summary of meeting

The meeting has answered a number of questions:

- The definitions of the CC fast signals are now finalized and can be used (update of website needed)
- The CC to FEE fast signal coupling will be finalized within 4 weeks.
- Slight rescheduling required of CC rollout.
- FEE will update firmware over the network and use the CC fast signal reset.
- We have seen that the software is beginning to appear and a video conference with FEE users after Easter should be planned.
- The time schedule should be reviewed and more detail added.
- VETO generation should be address before the next meeting.

Many issues that will have to be addressed (not now but soon) exist:

- Schemes for handling serious malfunction by experts with appropriate tools must be available.
- Powering up and down the FEE – any restrictions, order of powering… requirements for interlocks both hardware and software. (DAMC2 board interlock usage?). detail needs sorting out – PG says for the next meeting.

15 Actions

All the bold highlighted points in the text are reprinted here:

1. Please check that the mailing lists are complete and correct.
2. N.Coppola will provide feedback w.r.t. non lazing pulses and other potential vetos and details of data reduction and processing (correction) from CAMP at LCLS.
3. A brain storming VETO meeting is being planned.
4. UCL's requirements (when and what) for access to Timing Receiver boards has to reviewed as K.Rehlich does not have many and they have some interesting features.
5. Uncertainty still exists regarding the number of bits in the train number distributed by the timing system. The same applies w.r.t. the machine protection system – needs resolving.
6. The boundary where WP76 software development ends in the FEEs has to be defined
7. The FEE groups have to be brought into the software development discussions.
8. The design of the CC physical interface is required to fully design the LPD FEM. The solution needs to be tested and accepted by all user FEEs – Martin will do this within the next month.
9. The CC fast signal specification note has not been objected to by any of the FEE groups. The modifications decided during this meeting to the content (NOVETO to include the current bunch number, specification of the bit order to be used in transfer) will be inserted and the note put on the website. Modifications to the implementation (LVDS repeater) will be published when made – hopefully in 4 weeks. This note can now be used as input to FEE FPGA programming.
10. The memorandum for continued funding is required for financial year 2010, i.e. by 1st April.

16 AoB

The next meeting will be held at UCL (London) on 11.May.2010.