Minutes of the Train Builder meeting (22.10.2009)

AER 5.21, C.Youngman (last revised 23.10.2009)

1 Attendance list

WP76: S.Esenov, D.Wilson and C.Youngman.
LPD+TB: B.Halsall and J.Coughlan (telephone).
AGIPG: P.Goettlicher.
DSSC: T.Gerlach.
UCL: Sam XX, M.Postranecky and M.Wing.
FEA: I.Sheviakov.

The minutes, agenda and talks are reachable via:
http://xfel.desy.de/project_group/work_packages/photon_beam_systems/wp_76_daq__control/train_builder/ .

Important points are rendered bold, if you do not read the text then read the actions.

2 Introduction

Sam XX and Dana Wilson were introduced. Sam will be working on the C&C development at UCL and Dana has started work on the WP76 – C&C – FEE micro-processor boundary.

The prime aim of the meeting was to finalize the specification for the C&C system, get updates from the components, and receive an update from the timing group.

As reported at the last meeting both Train Builder and Clock&Control projects are now being setup with direct contracts rather than as in-kind contributions. Progress is being made on the C&C contract, but a few weeks is still required before submitting to EuXFEL management. Thereafter the TB contract will be pursued.

The actions from the last meeting were reviewed.

- The order for 160 VSC8486XJB-11 PHY chips has been placed and delivery (16 weeks) is expected Jan/2010. The number ordered is sufficient for TB and three 1Mpxl detectors.
- Martin has selected a suitable PLL chip, see later.
- Actions relating to C&C specs are addressed below.

3 LPD FEE status – R.Halsall for J.Coughlan

Major elements of the Front End module (FEM): power, mechanics, memory and 10G data opto-interfaces (using DESY FMC 10GE mezzanine as on Train builder demonstrator) have been determined and schematics for the memory interface, power and clocking nearly completed.

Draft layouts of the FEM were shown. The I/O design has been improve by adding small FPGAs dedicated to ASIC modules I/O with new backplane connector (Samtec SEARRAY). ASIC also now planning to use LVDS I/O. Firmware waiting on revised specification of new triggered ASIC design. FPGAs for prototypes have been ordered, long lead times exist.

Next steps:

- Verify FEM to ASIC module signal integrity with terminations.
- Complete FEM schematics and PCB layout.
- Aim for manufacture 2 off end Q1/2010
- Implement prototype firmware design including handling of new ASIC Veto logic.
- Implement prototype embedded software for fast data management and slow controls.

No show stoppers at the moment. The FEM requires the FMC which is expected to be available beginning of Feb/2010 – this is driven by the delivery of the PHY chip.

4 AGIPD FEE status – P.Goettlicher

Based on the PLL IDT ICS527-01 chip selected by Martin, Peter reviewed the system clock frequencies which could be distributed by the C&C (nominally just under 100MHz at last meeting) and resulting divided frequencies that would be available for use in the FEE for the ADC system. The conclusion was that the PLL was acceptable – note the possible bunch clock frequency change discussed in Section 11.

The FEE quadrant control layer was described. Fast signals from the C&C are received by an FPGA and a micro-processor is used to handle booting, configuration, monitoring, run control, etc. I2C bus is used extensively, see slide. Started looking at micro-processor implementation using Phycore-3250 evaluation board running embedded LINUX from NXP 2.6.27.

New VETO handling proposal will generate bookkeeping information concerning which cells have been used, reused, etc. Proposal is to have the ability to send this type of information with the data and also to the RC system. Bookkeeping information is required synchronously which is a new requirement, all other monitoring information is slow and cannot be delivered for monitoring and debugging to the C&C PC.

The ability to remotely download firmware (ASIC and FPGA) and reset systems needs addressing – this capability should be a requirement for all detectors. Online debugging needs to be addressed.

5 DSSC FEE status – T.Gerlach

The layout for ladder (data readout module) and transceiver interface (sequencer, C&C inputs, 10GE output) based around the Vertex 6 FPGA was shown. A number of changes have been made: the number of connectors has been increased to 2 and Spartan 6 FPGA which stream data over the MGTs. The number of links required and available is very tight. The targeted Vertex 6 is not yet available, but should allow direct driving of the optical link (without the PHY).

JTAG interface is used for programming the ASICS. **How to reset and provide network downloading of firmware needs to be addressed.**

Prototype board for 10GE developed – production and assembly is underway and the board is expected Nov/Dec. A generic PRACE2 system will be used to test this. The FPGA firmware is being written which will allow testing against standard Ethernet software on a client PC. These are similar to the DESY FEA tests made developing the 10GE FMC board.

The development schedule was shown and is on time. A small number of minor issues are open: mechanical design, ADC data format (dram or sram), etc. Issues exist regarding the power of the drivers need to send data from the data chips.

The standard used for network control from the C&C PC needs to be defined - what is running where on the FEE side needs to be specified. How much can be done in a common framework.

6 FEA 10GE status – I.Sheviakov

The FMC design will be completed by the end of the year; it uses the new PHY chip. An adapter board is available to check the new design using hardware compatible with the old design – there may be a capacitor issue which should be remembered if other groups want to use it (LPD).

The first FMC mezzanines will be available for use by the other groups (TB, LPD…) ~Feb/2010. The date depends on the availabilility of the PHY chip.

7 TB status – R.Halsall for J.Coughlan

A newer cross point switch will be used on the demonstrator board: Mindspeed M21145 80x80 with up to 6.5 Gbps, this is twice the speed of the previous chip which promises to reduce the wiring by half. The schematics for the demonstrator are in progress. FPGA and cross points have been ordered – due to long delivery times. There is a problem with the thin memory chips sourcing them. The demonstrator as such will allow testing of ca. ¼ of the full board with double height AMC format.

Memory tests are being continued by John. The puzzle of why the throughput does not notably increase with increasing the number of DMA engines remains – there seems to be contention on memory bank access. The targeted 2 block solution seems to be OK, i.e. the throughput has increased in comparison with the July measurements. The measurements are above the target bandwidth of 1.8MB/s required. Trying to understand why the improvement is not more significant remains an issue.

The shown 5Gbps input corresponds to 476 frames of data which is close to the 512 required – an improvement should result from resolving the issues – this needs watching.

8 TB cross point switch status – R.Halsall

The cross point is being tested using a ML523 board and Mindspeed development boards. The key issue is what happens to the MGTs when switching (break and relock connection), this talk concentrates on this issue. The board setup allows 16 MGTs to be used for the tests where the 16 links are driven by 2 Aurora cores (TX and RX) which are fed data from a pattern generator core and send received data to a pattern checking core. A sequencer controls the tests made. Which TX is connected to which RX is determined by registers in the Mindspeed that are set by the sequencer, double buffering of registers allows data transfer to overlap with the preparing the next register configuration.

The measurements made are encouraging: no errors are seen and the behaviour is as expected. The performance is sufficient for the train builder application. A list of additional tests are work are foreseen.

9 Software status – C.Youngman

Software development has been slow since work on messaging and content in July. Sergey is currently working on FSM code. Hopefully the free months of Nov. and dec. will improve the situation.

The computing TDR was recommended by the XDAC review board and a host IT service contract with DESY is being prepared. The intention is to have offline analysis and storage servies hosted on the DESY site and have PC layer and data cache located on the Schenefeld site.

Dana Wilson started working for WP76 on 1st Sept. and has been working with Peter's group on the testing of the quadrant micro-processor. This defines the endpoint for WP76-C&C-AGIPD interaction. His task in the next few months will be to define the requirements and test that the foreseen implementation will work.

10 VETO discussion & decision

The proposal for a new definition of the VETO was distributed to FEE groups at the end of Sept. and presented at the XDAC meeting in Munich (the original note will be appended to the website.)

The proposal foresees multiple veto detectors (plus logic) which generate 5MHz trigger input to the C&C veto unit. The output of the veto unit is a ~100MHz (≤20bit) bunch number to veto. The latency of the bunch number to veto is no longer defined (to be short, e.g. ≤10 bunch crossing) it is almost asynchronous.

The C&C, AGIPD and DSSC groups will implement the new design. The LPD group require that the short latency be maintained. Both solutions will be provided by the veto unit - for LPD either the input 5MHz veto signal will be passed transparently through (with the correct delay) or a 100MHz bunch number encode result will be sent provided the veto detector latency is within the limit specified by the LPD group. **The LPD FEE group should state what they require.**

11 Timing board status – K.Rehlich

The status of the timing system design and the availability of the TR (Timing Receiver) board were reviewed.

Six timing receiver boards have just been delivered by the in-kind Swedish contributors. Initial tests have been performed successfully. The board contains both TX and RX, the onboard TX for testing was not planned at the Nov.2008 meeting (it had been requested!). The purpose of the board is to qualify chipsets to be used in the final TR board design.

The frequency of the non glitch synchronized to the 1.3GHz master that is distributed to the TR (and on to the C&C) is in the process of being fixed. The shown frequency of 100 KHz is low at least w.r.t. to the input frequencies that were expected by the C&C group. There was a discussion of what this frequency should be 600 KHz was a lower bound specified by the C&C group. **The C&C group should quickly state what lower frequency bound they need – and ensure that this is communicated to Kay.**

The bunch repetition (currently 5 MHz) rate is also being discussed. During the last few days an old request for setting the value to 4.5 MHz (the FLASH value) has been restated. **The FEE groups (ASIC…) are asked to make a statement about whether this change is acceptable by 6th Nov.**

12 C&C status – M.Postranecky

Martin's talk reviewed the status of the C&C. The main thrust, however, is to specify (payload, start/stop bits, parity/checksum…) the fast signals and suggestions were given – see slides. **It was agreed that Martin and Dana would produce (with input from the FEE groups) a specification document within the next 2-3 weeks. Once ready the note would be distributed for comments**.

13 C&C signal and message spec discussion

The action point from the previous section made this discussion item superfluous. **Clearly the specification document should include the network message (protocol, content…) as well.**

14 Actions

1) The ability to remotely download firmware (ASIC and FPGA) and reset systems when hung needs addressing – this capability should be a requirement for all detectors. All

detector FEEs should send me a statement about how they currently plan to accomplished this in the next weeks.

2) The LPD FEE group should state their requirement w.r.t. the input veto signal to their FEE. Either the old 5MHz yes/no, or 100MHz with bunch number encoding and a low (specified) latency requirement. As update work on the C&C specification is underway, the statement needs to be available within 2-3 weeks.
3) The C&C group should quickly state what lower frequency bound they need – communicate this to the rest of us so that Kay can be informed. I assume that this has to be done within the next 2-3 weeks.
4) **The FEE groups (ASIC…) are asked to make a statement about a whether 4.5MHz bunch clock is acceptable. Please send an answer to me by 6th Nov.**
5) Martin and Dana will provide an updated definition of the C&C fast and network interface (protocols, content…) within the next 2-3 weeks.

15 AoB

The next meeting will be held at DESY on 18.Feb.2010.