Minutes of the Train Builder meeting (5.5.2011)

Location: Rm 4.14, AER 19
(12.5.2011 - CY)

1 Attendance list

WP76: N.Coppola, S.Esenov (am), B.Fernandes, B.Heisen (pm) and C.Youngman.
LPD+TB: J.Coughlan and R.Halsall
AGIPG: P.Goettlicher
DSSC: T.Gerlach.
UCL: S.Cook, E.Motuk, M.Postranecky and M.Wing
FEB: F Krivan, I.Sheviakov, Qingqing Xia and M.Zimmer
MCS4 and WP18: P.Gessler.

The minutes, agenda and talks are reachable via:
http://www.xfel.eu/project/organization/work_packages/wp_76/daq/2d_pixel_detectors/meetings/ .

Actions are rendered bold. Items of importance are underlined.

If you do not have time or do not want to read the entire document, then skip to the summary and actions.

2 Last meeting actions and purpose of meeting – C.Youngman

Last meeting actions status:

- **1.** *It was agreed to organize, in the near future, a meeting (EVO…) with Markus Kuster (WP75) to coordinate TB, CC and detector test requirements.*
  The updated detector time schedule, see slide 6, was generated by Markus. It was agreed that the ATCA demonstrator board can be used for testing with cameras in 2012-2014. **A number of other issues are still in the pipeline: WP75 and 76 reorganization, note defining WP76 interface for pnCCD detector, update of number of detectors foreseen and their sizes.**

- **2.** *A working group on data formats should be initiated with the detector groups*
  The group was constituted at this meeting, see summary.

- **3.** *Producing a short 1-2 slide roadmap note for input into the next XDAC should be aimed at (JC, CY and MK WP75).*
  The roadmap for building larger train builders shown at the XDAC, slide 8, led to the referees suggesting using the demonstrator board as the TB building block. This would avoid complicated backplane solutions and not require new developments. This conclusion ties in well with the direction indicated in the TB status talk below.

- **4.** *It is necessary to plan the production of finished FMCs, this must be organized as an action.*
  This was done and 50 FMC are now being manufactured, see FEA status talk.

- **5.** *Erdem should be placed on the DESY FPGA expert email list and attend the meetings.*
  This was done.

- **6.** *Document data format as understood now for discussion at the next meeting.*
  See point 2 above.

The aims of this meeting are listed below, see summary of meeting for results and other points arising:

- Agreement on TB road map
- Launch data format work group
- Check TB demonstrator (Q4/2011) and CC prototype (Q4/2011) schedules
- Check VETO development
- Conference contributions

3 TB status – J.Coughlan

The status of the ATCA format demonstrator and an update on TB scalability was given.

PCB layout work on the demonstrator, slides 1 and 2, has started concentrating on the front end inputs. For, possible, image manipulation each channel will have a QDR memory which will be used to test image manipulation (spatial organization at the pixel level, 8MB for 1 or 2 channels?). A front plate RJ45 for network has been squeezed onto the front panel to allow standalone testing. Circuit schematics are ~90% done and the demonstrator is on schedule for submitting to manufacture Q3/11, with testing starting Q4/11.

TB size scalability using the demonstrator as the building block was described. The slides shown in January (used for the XDAC roadmap) showed solutions using various passive and active backplanes configurations, these are too complicate and depends on technology developments. Using the demonstrator as a building block requires less development and the following configurations exist:

- 1/4 Mpxl with single demonstrator board (4 input and 4 output links, cross-point switch active on board).
- 1/2 Mpxl with 2 demonstrators boards (board 1: 8 input links and 2: 8 output links, cross-point switch active on one board, fixed on other) linked with two cable Z3 connections (ERmet ZD Wafer Cable), slide 7. Control synchronization would be one boards master FPGA using a few LVDS lines over the cable.
- 1 Mpxl with central switcher cards (in a pizza box) located in the ATCA rack but not in ATCA format, see slide 8. The switcher card contains a cross-point switch based on the same family used on the demonstrator. The system must be compatible with

the existing demonstrator board and would require a RTM with parallel optical (copper might be possible) connections to the switcher, candidate compact optical drivers are being looked at.
- 2 Mpxl with pizza box can be implemented using a bigger, or multiple stacked switchers. Above 2MB the constraint is depth of memory on the output board.

The above scalability solutions were discussed at length (timing, separate data and control paths, etc.). Using the demonstrator as a building block is certainly easier than following more complicated backplane solutions. The use of a switcher does not introduce new technology as large versions (or multiple of the demonstrator) of the demonstrator's switch can be used and no problems (timing, control, etc.) are expected.

Next steps in the TB development:
- Complete the TB ATCA demonstrator (this has the highest priority)
- Test 1GB DDR2 VLP SODIMM memory and look at larger memory banks
- Develop ideas on control plane
- Evaluate optical modules for RTM
- Produce proposal document for XDAC which must include all factors (header data size, memory depth using other SODIMMS, etc.).

Using the demonstrator building block and a switcher will allow 2Mpxl TBs to be built. This is to be compared with the 1Mpxl baseline camera design, increasing to the 4Mpxl target (M.Kuster) a few years later, which opens the time window for taking on board other design compatible developments (increase memory depth, high link speeds, V7…). Above the limit size additional train builder will have to be done in the backend PC layer.

4 TB FPGA programming – R. Halsall

Rob described the LPD FEM and TB FPGA development work.

The FEM is being used as a test bed for developing UDP firmware. A Local Link (LL) Bus monitoring module has been developed to allow monitoring the transfer protocol used. Matlab with a UDP receiver process, in the back ground, is used to drive the test bench. This is useful for basic testing, but will not run at full speed. The UDP module developed is working although not fully tested.

There was a discussion of other protocol implementations. TCP and iWarp could be developed. The UDP module took 1-2 months work over a 6 month period. The priorities are: UDP FEE to TB, then UDP TB to PCfarm, and then look at exotics like TCP and iWarP. TCP could be done with a limited stack implementation. **The possibility of using collaborating developers for additional FPGA development should be looked into.** Developing reliable UDP (UDP+) is not on the development path (there is not enough memory in the FEE for retries), but this may not stop it being done.

Next steps for the train builder development
- Convert Aurora-Xpoint test bench to LL-Aurora-IP Block
- Complete Simple LL-UDP-IP Block (Receive Side)
- Complete LL-XPOINT-IP or bigger LL-MUX-IP
- Develop a LL-RDMA or PLB-RDMA IP Block
- Develop LL-UDP+(!)/TCP/iWarp-IP block
- Build a dev board version of design for tests
- Build final version of design for TB

- Test…

5 FEA status – M.Zimmer

50 FMC are being manufactured by DESY-ZE. Connector delivery was slow but has now been completed and enough components are onsite. The FMC should be available after functionality testing by Igor end June. **The LPD group need a few FMCs as soon as possible, in June, and should get the first that come of the production line.**

The status of the DAMC2 (used by CC) generic digital board was described. The board was delayed and no user modifications other that those of the CC group have been received. This means that the requested Autumn/2011 modification/production run will be delayed.

The development of user friendly FPGA coding framework (within the FPGA expert group initiative) is continuing. This concentrates on using ISE to develop modules around the II bus (similar to LL), see slide 6. Some effort has been spent looking at using EDK with the Microblaze soft core, but resources are quickly exhausted and this approach may not be useful unless there is a very specific usage (stepper motors in the TPS system). The CC will not use EDK.

6 Status of DESY firmware expert group – P.Gessler

The firmware expert group is aimed at pooling development by having a well defined framework. It should provide a source code repository and try to minimise the number of supported platforms and use RTMs to decouple signal handling differences.

The project start up has concentrated on the DAMC2 platform and using II Bus wishbone (similar to LL) developed by DESY and a Polish group. A number of modules are being developed (some ready): PCIe interface to II bus, timing, DDR2 memory, etc., see slide 3 and 6. Rob pointed out that everybody has their own internal bus, which will also change when Vertex7 arrives (LL replaced by AXI stream), so a possible transition should be planned..

The repository is SVN based and an initial version (structure) is available from outside DESY. Issues exist like versioning which are in discussion. The STFC groups use SVN, but there are many open issues (versions for project, design tools…). Questions like how other WP76 and firmware software can be versioned in a common system should be looked into. Interested people are CC(Erdem and Sam), STFC(Tim).

Wiki documentation is on: https://xfel-fpga.desy.de/Main_Page . A complete API documentation of the II bus is in the pipeline. John pointed out that groups often commit to using similar bus ideas, but then they are under supported.

A number of development tools have been written to ease usage (mapping tools), see slide 7.

7 Status of Timing Receiver board – P.Gessler

The CC and WP76 groups received the last version of the 1st generation board in January. The second generation double size version will be available at the end of the year as a prototype.

The bus connection and telegram content and delivery mechanism was described, see slides 8 and 9. These showed a basic problem that exists with the communication with the TR developers. How can we be sure that the definitions that we requested are indeed still known and applied – Patrick agreed to check our CC requirements (from the Sept/2010 meeting) to ensure that all are still in place.

Note that the CC requested 4.51 (generated from FPGA) and 99.31MHz (onboard PLL) can be generated and are glitchless. All frequencies generated are guaranteed to be glitchless as long as above long as the frequency is above ~100kHz.

Note that the Harlink (impedance and cross-talk problems) will be replaced by RJ45 on double height version (watch out for internal cross-connection differences on different versions of RJ45).

The status of firmware and next steps were shown on slides 12 and 13. By the end of May TR standalone firmware will be available for use with the 1st version board. This will allow generation of standalone test sequences (including telegrams) which should ease CC testing.

It was agreed that Erdem and Martin would recheck that the requirements of the CC which we agreed to last September would be checked.

The expected jitter on the TCLKA and TCLKB distributed clocks should be updated and transmitted to FEE groups.

8 C&C status – E.Motuk

The current status of CC development was described.

The PC3461M PCB which provides simulated CC fast signals (clock, command, veto and status) with AC coupling for FEE developers is manufactured and tests successfully. **FEE developers who need the PC3461M CC fast signal generator with XUPV5 and ML50x development boards should ask for it.**

The DAMC2 and TR boards delivered have been installed and simple tests have been run in the MTCA.4 crate. Both boards were detected by IPMI tools and simple tests of the PCIe functionality of the DAMC2 board were performed.

The RTM schematic design is finished for the 1 Mpxl prototype design. Real estate on the board has been used to provide extra prototyping functionality. The assembly drawing is shown on slide 8. The RTM is currently in the layout phase at Rutherford Lab.

The CC has joined the firmware expert group at DESY, see section 6, which will allow reuse of modules being designed by other developers, at least for the CC DAMC2 board. Firmware that can be used are: standard PCIe core, II bus interface and telegram data transfer module. Using the II bus the block diagram now looks like – see slide 12. CC modules which had been written will be modified to use the expert group framework, these are the fast data transfer and veto logic.
The VETO development has come out of hibernation with the appearance of the Toroid Protection System which has some potential for use as a VETO source, other sources are the APDs from the single crate DAQ system. TPS hardware is designed to measure in real time the current of each bunch in the XFEL bunch train. The TPS system is conceived

as a protection system, unexpected loss of bunch current between TPS stations distributed along the beam line is used to prohibit further beam injection. Nicola Coppola has analysed bunch current fluctuations in data taken at LCLS. During periods of normal operation 1-2% of bunches have lower currents, more than 3σ, from the mean. The percentage can be larger during periods of non normal operation. Measurements of bunch currents from TPS stations could therefore produce a meaningful VETO signal, albeit with low veto rates. TPS stations before and after the undulators are the most useful as the photon generation point is the last (closest to the experiments, lowest latency) where electron bunch properties measured are meaningful for the corresponding pulses seen at the experiments (bunch properties measured after this point has no meaning for the photon pulse observed). The aim is to address the large number of issues exist (what source protocols are used, fan-in and fan-out handling…)**. A TPS VETO feasibility document should be produced which should address the overall VETO design.**

Next steps are:

- May – RTM manufacture
- Early June – RTMs testing
- May thru June – Firmware development (II Bus integration, drivers)
- June thru August – RTM + DAMC2 in crates tests (standalone mode, with TR, fast signals with PC3641M)
- May – VETO TPS feasibility document

The prototype CC 1Mpxl master is still scheduled for Q4/2011.

9 LPD FEE status – J.Coughlan

The first two FEM boards, arrived January, have been tested and all major components are working. Initial version of firmware needed for module testing has been implemented and test bench of reading out ASICs to PC via FMC 10Gbps mezzanine are prepared.

Next steps:

- Test with single ASIC test card
- 2 sensor tile tests
- super module tests

Another two FEMs have arrived and are being tested. More 10Gbps FMCs needed.

10 DSSC FEE status – T.Gerlach

The IO board has been redesigned to imrove signal quality by inserting more grounding planes. A number of different solutions for the power switching have been tested with the aim of providing error safe power switch and the best solution chosen. IO board prototyping is almost finalized.

Investigations are being made concerning aggregating sensor data per quadrant rather than per module, which would remove the requirement of an external crate for module link boards. This does not violate the TB requirement of one 10Gbps link per module provided four links per quadrant are produced, but the proposed QSFP+ links may not be compatible with the SFP+ and would need fibre reorganization.

Next steps:

- May – finish the IO board layout and routing
- May – start DAQ TM schematics

11 AGIPD FEE status – P.Goettlicher

No significant changes have been made since the last meeting. There is an ongoing discussion of pipeline storage times and digitization rates.

12 Software status – B.Heisen

The software being developed to provide a homogeneous software framework for beam line control, DAQ, data management and scientific computing was decribed. The toolkit of support tools is in an advanced state of development and is based on high quality open source and industry standards (boost, XML, XSD) and is used for the communication, configuration, etc. functionality needed to implement a DeviceServer/Device pattern.

Tests using software emulations (e.g. two motor slit) have been carried out and test with hardware will be made soon. For more details see the slides.

13 Summary of meeting

The understanding of TB road map is that the ATCA demonstrator will be the baseline building block. Data transmission protocol implementing FEE to TB (UDP and custom) and TB to PC layer (UDP) must be available with the demonstrator prototypes. Other developments (protocols, switchers, etc.) should have lower priority until the demonstrator prototypes are available. Additional FPGA programming capacity is available and should be used.

Launch of the data format group. To define what the FEE are providing, define internal data formats used and defining what is sent to the backend. The following group participants were nominated: P.Goettlicher, R.Halsall, C.Youngman, T.Gerlach and M.Kuster. **The data format group should provide an initial definition note for the next meeting.**

The TB demonstrator and CC master prototype are on schedule for Q4/2011.

Work on the VETO system has restarted with the preparation of the TPS VETO feasibility document.

Conference contributions to NSS in Valencia were coordinated. The CC group are planning a conference contribution and will include a few slides on the TB. The TB group will not contribute to NSS. DSSC-FEE will contribute and should refer to the CC contribution for CC and TB. Markus has submitted an overview of detector development (one slide on rates) at XFEL and the detector groups are also submitting contributions which are detector specific.

Manfred will cost 300 PHYs, which replace those used in the current FMC production run.

14 Actions

The list of actions:

1. **WP75 and 76 milestone reorganization, note defining WP76 interface for pnCCD detector, update of number of detectors foreseen and their sizes.**
2. **The possibility of using collaborating developers for additional FPGA development should be looked into.**

3. **The LPD group need a few FMCs as soon as possible, in June, and should get the first that come of the production line.**
4. **It was agreed that Erdem and Martin would recheck that the requirements of the CC which we agreed to last September would be checked.**
5. **The expected jitter on the TCLKA and TCLKB distributed clocks should be updated and transmitted to FEE groups**.
6. **A TPS VETO feasibility document should be produced which should address the overall VETO design.**
7. **The data format group should provide an initial definition note for the next meeting.**
8. **Manfred will cost 300 PHYs, which replace those used in the current FMC production run**

15 AoB

The next meeting will be held in Hamburg on 28th Sept 2011 (date to be confirmed).