

# Draft Minutes of the TB and CC meeting (12.7.2012)

Location: Rm 5.21, AER 19  
(21.7.2012 - CY)

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## 1 Attendance list

WP76: D.Boukhelef, N.Coppola, P.Gessler, S.Esenov and C.Youngman.

WP75: M.Kuster (pm)

MB: A.Schwarz

LPD+TB: Ed Freeman (new member taking over from S.Taghavi – layouting, f/w...), J.Coughlan, R.Halsall (previous two days TB setup) and T.Nicholls (EVO)

AGIPD: P.Goettlicher

DSSC: T.Gerlach (EVO)

UCL: M.Wing, A.Joy and E.Motuk

FEB: I.Sheviakov and M.Zimmer

The minutes, agenda, links to documents referenced and talks are reachable via:

<https://docs.xfel.eu/share/page/site/xfelwp76/documentlibrary#filter=path/Meetings/TBAndCC/Archive>

and choose the appropriate folder. If you do not have access, send me an email!

**Actions are rendered bold.** Items of importance are underlined.

If you do not have time or do not want to read the entire document, then skip to the summary and actions.

## 2 Summary of actions from last meeting – C.Youngman

Last meeting actions status:

1. *Front air intake and output on the side of 2U crate – implications for racks?*  
Open – crate status addressed in section 3.

2. *Expect 6 ordered DAMC2 boards in 2-3 months.* Done – the updated version of the DAMC2 will be used which will arrive later. The schedule was outlined in section 4.
3. *AC coupling is on the receiver side – UCL should check that this is indeed correct.* Done, it is correct, see section 8.
4. *Is Wiener/Iseg the standard solution - needs resolving and an agreement in place to.* Open – nothing done.
5. *Sergey Esenov will prompt Tim regularly about the status of the TB lib.so interface to the XFEL control system which will be based on the LPD development.* Done – the implementation is delayed until after the summer break.
6. *VETO specifications issues were addressed, but do we have a final understanding of what is being provided by both sides regarding GOLDEN and protocol latency!* Done – the post discussion version 0.5 VETO specification document was agreed to, see section 3, it contains a detailed description of detector behaviour.

### 3 Summary of TB, CC and FEE FPGA meetings– P.Gessler

The minutes of the bi-weekly meetings are in:

<https://docs.xfel.eu/share/page/site/xfelwp76/documentlibrary#filter=path/Meetings/FPGA&page=1>

The agreed to version 0.5 VETO specification can be found in:

<https://docs.xfel.eu/share/page/site/xfelwp76/documentlibrary#filter=path/Projects/VETO%2520System&page=1>.

Nikhil is currently finalizing the low-latency link (LLL) protocol to be used by the VETO system to transfer information. **A LLL description note will be provided with the f/w modules by Nikhil.**

The CRISP 10GbE and beyond workshop

<https://indico.desy.de/conferenceTimeTable.py?confId=6084> (24-25.5.2012) reviewed 10, 40 GbE technology for Ethernet, infiniband and PCIe, on-going projects (TB, fast frame rate cameras, etc.) and future 100GbE plus developments. Rob's future technologies (FPGA, links, etc.) summary talk was a highlight! A conclusion of the workshop was that an immediate move to TCP on the TB output to the PCL should be postponed as it will require more time than originally assumed. The workshop was appreciated by the participant and a follow up is definitely needed.

The prototype small (2U) crate was delivered and has cooling problems 60-80°C board temperature measured. The designers have been informed and a solution should be reachable by end of year. **An update of the 2U crate cooling problem will be given at the next meeting.** The mounting of the crate in standard (non XFEL tunnel racks) bottom-top airflow rack was discussed as these crates will be used outside of the tunnels (experiment and laser installations). Problems were described – **a statement is required concerning whether 2U crates can be used other than in tunnel racks.**

## 4 FEA status– M.Zimmer

The rollout schedule of the revised design (see slides for features) DAMC2 board was outlined (assumes board passes acceptance tests):

- prototype boards delivered first week July
- finish testing ~end July
- friendly user testing phase
- order of initial 100 boards ~end Sep.
- arrival of boards ~end 2013 (including the 6 we want)

In total 400-500 boards are required for the e-machine. **An estimate of the number of DAMC2s needed by PBS needs to be available mid-2013.**

The plans for the next generation of the DAMC2 were shown. These include: Kintex 7 FPGA, SFP+ and 4 x 10Gb outputs on front panel, Ethernet on the backplane (supported on new bus specs.), PCIe up to gen3. Aim is to be pin compatible to the current DAMC2.

## 5 AGIPD FEE status – P.Goetlicher

Prompted by on-going discussion of detector data formats, Peter reviewed the bunch and pixel ordering produced by the front end module.

Image order is guaranteed to be in bunch order as requested.

Discussion has started with the ASIC designers with the aim of defining the best possible ASIC pixel readout ordering so that front end output module pixel ordering can be as close as possible to the top-row-to-bottom-row left-to-right-column-within-row (seen by the sample) requested can be produced by the board FPGA. **A statement should be provided at the next meeting on what ordering can be achieved by the AGIPD FEE module.** The aim should be to get the highest level of ordering done at the FEE leaving less work to be done at the TB (also eases reformatting needs when the FEE is connected directly to a PC). Currently no statement is required from WP76 to the AGIPD management supporting this request.

## 6 LPD FEE status – J.Coughlan

The 2 tile single FEM desktop box detector is being used for f/w, control s/w... development. Control is via 1GbE and is working well. An LPD quadrant system is being prepared for tests at Diamond and possibly LCLS. Resubmission of the ASIC in July to improve radiation hardness, fix features, etc. The LPD phase 1 project finished, now moving to phase 2.

The pixel ordering produced by the ASIC was described. The plan is to implement bunch crossing ordering in the FEM and do pixel reordering in the TB. The latter will require appropriate use of TP FPGA, switch and QDRs and estimates show that this should be possible. **An update on the feasibility of the LPD ordering plan (bunch and pixel) should be given at the next meeting.**

## 7 DSSC FEE status – T.Gerlach

Tests and verification of the IO board modules is in progress. A redesign of the IOB is planned for August. **The data format group should send Thomas a description of the current status of the format definition by mid-August.**

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## 8 Clock and control status – E.Motuk

Using a higher power, large voltage swing, MLVDS driver chip soldered to the PCB (few flying cables) allows 30m length CAT 6 STFP cable can be driven with the design AC coupling circuit. The cable length investigation will be stopped as we can reach 25m. Tests should be made later at FLASH.

Tests of TCLKA distribution with the single width AMC timing receiver have problems (also seen by other groups) f/w or h/w fault in the X1. Standalone firmware for the receiver is available since yesterday which allows triggers, events and telegrams (TRN, bunch index ID, etc.) generation. These will be used to test telegram handling f/w and a generic module for telegram handling will be added to the FPG group library.

Design of the final CC RTM will start soon. The schematic for the new revision of the DAMC2 is required. Before production of the final CC RTM tests need to be made with detector FEE modules (only the LPD FEM is available) to validate operation of the CC. **In the CC fast signal specification the FEE status line to the CC carries with a 99MHz clock onto which information can be encoded. What information is encoded by LPD and the other detectors?**

The current time line is:

- Summer 2012: final schematic for CC RTM
- Summer-Autumn 2012: prototype RTM tests with FEEs
- Winter 2012: production of final revision of CC RTM

## 9 Clock and control s/w status – A.Joy

The proposed design was shown. A clear decoupling of s/w blocks (usage) is needed:

- GUI for testing – the standard GUI (Kerstin Weger) exists and should be used for test GUIs and control of the CC device.
- Device s/w – the s/w seen by the control system which implements messaging with the control system broker, the CC FSM, etc. many devices have been implemented and a suitable template should be used.
- API - library package providing device and any test s/w an interface to the CC f/w (and h/w). The API may depend on lower level libraries like the PCIe library.

**A CC s/w meeting is planned for early August (~6.8.2012) to define interfaces to sub-systems used:**

- Configuration of timing module set configuration.
- VETO configuration.
- Debug handling.

Who participates: Patrick, Erdem, Tim, Ashley and Chris.

Imperfections in PCIe library exist and DMA is not provided.

## 10 TB status – J.Coughlan

A demonstrator board has been delivered to XFEL (2.12) and a smooth handover was achieved. Two of the boards 10GbE links are connected directly to exflst402 and using the scripts provided data (content: incremented numbers) has been sent (packetized with Rob's UDP trailer format, Jumbo...) and received by Djelloul's PCL receiver application (with wire speed = Inter Frame Gap = 0). Next steps at XFEL:

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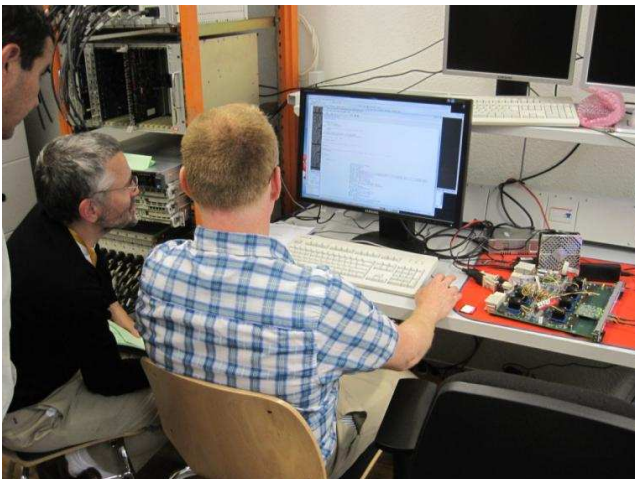
- Additions to the driving script and f/w (cycle, lists of targets...)
- Provision for downloading data blocks (LCLS data with our data format)
- Move board to crate in CC on Patricks return
- Develop control system device s/w (Sergey and Tim) by end Sept.
- Use board to drive data into slice test (in Oct before XDAC)

Current TB development highlights: 4 demonstrator boards have been manufactured (components in hand for 2 more). No problems found so far, but not all functional testing (see slides) is finished. Python control s/w (via 1GbE) and associated f/w working, many test scripts. Power used with all components on board is 120W. Two train builder demonstrators (1/2 Mpxl) connected with a Z3 cable have been tested OK (= 1/2 Mpxl). Data generator f/w foreseen for: FPGA generated incremented numbers, video generator and playback data, former currently available.

Next steps at RAL:

- Cross-point switch tests
- DDR2 and PPC engines
- QDRII tests
- Then phase 2 h/w RTM for larger TBs

XFEL server room



TB demonstrator



## 11 LPD and TB s/w interface status – T.Nicholls

The python s/w used with LPD FEM and ASIC f/w tests was described (class architecture). The WP76/LPD meetings need to be resurrected so that the final API can be specified. **A meeting before the end of July should be organized for planning what/when regarding the FEM/TB API.**

## 12 TB f/w interface – J.Coughlan for R.Halsall

The 10 GbE UDP f/w status was reviewed – in advanced state allowing wire speed 10GbE usage in FEM and TB tests. Recent improvements to the UDP trailer protocol concerning padding needed to avoid non send of packet were explained.

Next steps:

- Test Farm Mode (= TB to PCL via switch) with 10G switch
- Modify receive channel to work with trailer mode

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- Add checksum/crc checking to Rx Channel
- Complete port of design to virtex 6
- Release to XFEL

### 13 Slice test and software status – D.Bourkhelef

The slice test comprises a complete slice through all the architectural layers of the XFEL DAQ and DM architecture. The aim is to prove all aspects of the final system (readout, processing, formatting and storage) on the slice. Currently the slice width is a ½ Mpxl 2D camera which will be driven by a single TB demonstrator board (currently emulated by PC nodes). The on-going h/w and s/w developments were reviewed.

The current status h/w status is that PCL, switch and GPUs their host machines are onsite and working. In the week following this TB+CC meeting the storage system also were delivered.

An update of the 10GbE network performance measured with the equipment was given, initial results were shown at the last meeting. Full wire speeds are measure with concurrent r/w on the two ports of the PCL hosts NIC. Considerable work was invested in understanding the tuning required and in reproducible configuration for link usage (buffers, queues, NAPI driver, CPU affinity, Jumbo frame, hyper threading...). Packet loss is low and occurs only during the first few packets of a transfer test – the PR number for packet loss probability with static routing through the switch is  $\sim 10^{-9}$ . **Slice tests with dynamically switch links are required to ensure that packet loss remains acceptable when train data passes through the switch, in particular trains with smaller numbers of images that 512 are transferred.**

Hardware summary:

- Full link bandwidth: 9.93Gbps
- Plain vanilla UDP with acceptable packet loss
- Yesterday started testing PCL software (readout) using TB board input
- Additional long-run test with software emulator and/or TB

Software summary:

- Software under continuous development to test the impact of concurrent processing on read and write
- Device model is implemented
- On-going work to use DeviceServer, GUI within our PCL software
- Software configuration (automated)

Next steps:

- Dynamic route switching tests
- Processing performance measurements
- Data aggregation and formatting implementation

### 14 Data formats – C.Youngman

The current status of the data format discussion was reviewed. Data format meetings are held bi-weekly since March, concentrating initially on h/w near bottom-up issues now top-down,. Minutes and input documents on:

<https://docs.xfel.eu/share/page/site/xfelwp76/documentlibrary?file=FPGA#filter=path/Meetings/DataFormat&page=1>

Bottom-up discussion started with LPD, then AGIPD, and then commercial cameras (A.Parenti), DSSC will be brought in next. Top-down discussions with scientific computing and data base experts.

A HDF5 efficient data format (array based) is aimed for (also favoured by LCLS), see slides. Due to pixel ordering and reformatting limitations on 2D camera FEEs two distinct contents will exist: FEE output and TB output. Emulation s/w will be needed to create TB output content for non TB operation with FEE modules. The image content ordering aimed for is:

- Bunch ordered images
- Pixel ordering top-bottom and left-right as seen from the sample

Next steps:

- Compliment bottom up design with top down (catalogues and database)
- Finalize HDF5 api (work in progress)
- Simulate in slice test
- Produce a conceptual design document

## 15 Discussion of readiness for 2D detector tests with WP75

The readiness of WP76 and WP75 sub-systems needed for ¼ Mpxl LPD detector WP75 tests starting January 2013 was discussed and the table below of who does what when was produced – involved parties should provide feedback if they do not agree!

what	needed	when needed	who	Comment
¼ Mpxl	detector	Jan 2013	STFC	Detector delivery?
cooling	System control	end Dec 2012	STFC	Need input from LPD
slow control (sc)	HV, LV...	end Dec 2012	STFC	Need input from LPD
cooling+sc	Device s/w	end Dec 2012	Nicola Sergey	Need input from LPD
FEM	f/w	end Sept 2012	Rob	
FEM	C++ interface lib.so	end Sept 2012	Tim	
FEM	device s/w	end Sept 2012	Sergey	
CC	DAMC2 board	available (old rev.)	N/A	
CC	DAMC2 f/w	end Oct 2012(?)	Erdem	
CC	RTM	available (old rev.)	N/A	
CC	C++ interface lib.so	end Oct 2012(?)	Ashley	
TR	Timing board	available (old rev.)	N/A	
MTCA	2U(?) crate	end Nov 2012	Patrick	Reserve if not available
PC	control PC	end Nov 2012	-	broker, GUI... in rack?
PCL	2 host each dual NIC (2U)	available	N/A	old PLC machines
PCL	Device s/w	end Nov 2012	Djelloul	
PCL(?)	Local storage	End Dec 2012	Janusz	
TB	demonstrator	end Nov 2012	N/A	
TB	f/w	end Nov 2012	Rob	
TB	C++ interface lib.so	end Nov 2012	Tim	
TB	Device s/w	end Nov 2012	Sergey	
ATCA	Crate (15U?)	end Nov 2012	Patrick	Smaller if possible
1GbE	Switch	end Nov 2012	-	Control network
10GbE	Switch	end Nov 2012	-	optional
Rack	>20U (from above)	end Nov 2012	WP75	
Sci. comp. s/w	framework	end Dec 2012	Burkhard	
Sci. comp. s/w	algorithms	end Dec 2012	Stefan	

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DM services	Catalogues, HDF5, dirs....	end Nov 2012	Krzysztof	Need input
DM	File format	end Nov 2012	Krzysztof	

#### Observations:

- The use of a TB demonstrator does not require a switch if static routing used
- The “when needed” allows for test to start in Dec 2012, but Jan 2012 may not be a hard deadline.
- A detailed check of h/w as additional items will have to be purchased – existing test h/w cannot be committed long term (e.g. 2 TB demonstrators were requested for the slice test and 1 can be used short term for the ¼ Mpxl test, but additional boards are required)
- **A review of the ¼ Mpxl schedule and related h/w availability is required.**

## 16 Summary and actions list – C.Youngman

#### Actions list:

1. **A LLL description note will be provided with the f/w modules by Nikhil.**
2. **An update of the 2U crate cooling problem will be given at the next meeting.**
3. **A statement is required concerning whether 2U crates can be used other than in tunnel racks.**
4. **An estimate of the number of DAMC2s needed by PBS needs to be available mid-2013.**
5. **A statement should be provided at the next meeting on what ordering can be achieved by the AGIPD FEE module.**
6. **An update on the feasibility of the LPD ordering plan (bunch and pixel) should be given at the next meeting.**
7. **The data format group should send Thomas a description of the current status of the format definition by mid-August.**
8. **In the CC fast signal specification the FEE status line to the CC carries with a 99MHz clock onto which information can be encoded. What information is encoded by LPD and the other detectors?**
9. **A CC s/w meeting is planned for early August (~6.8.2012) to define interfaces to sub-systems.**
10. **A meeting before the end of July should be organized for planning what/when regarding the FEM/TB API.**
11. **Slice tests with dynamically switch links are required to ensure that packet loss remains acceptable when train data passes through the switch, in particular trains with smaller numbers of images that 512 are transferred.**
12. **A review of the ¼ Mpxl schedule and related h/w availability is required.**

## 17 AoB

The next meeting will be held in Hamburg on 8<sup>th</sup> Nov 2012.

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