

Draft Minutes of the TB and CC meeting (19.4.2012)

Location: Rm 5.21, AER 19
(11.6.2012 - CY)

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1 Attendance list

WP76: D.Boukhelef, K.Wrona, N.Coppola, B.Fernandes, P.Gessler, S.Esenov and C.Youngman.

LPD+TB: J.Coughlan and R.Halsall

DSSC: T.Gerlach.

UCL: S.Cook, M.Postranecky and E.Motuk

FEB: I.Sheviakov and M.Zimmer

The minutes, agenda, links to documents referenced and talks are reachable via:

<https://docs.xfel.eu/share/page/site/xfelwp76/documentlibrary#filter=path/Meetings/TBAndCC/Archive>

and choose the appropriate folder. If you do not have access, send me an email!

Actions are rendered bold. Items of importance are underlined.

If you do not have time or do not want to read the entire document, then skip to the summary and actions.

2 Summary of actions from last meeting – C.Youngman

Last meeting actions status:

- 1. The final timing CDR document needs vetting by us, and other parties, before approval.* Done but the CDR never appeared officially.
- 2. Long term plan for CC test system needed.* Additional DAMC2 ordered to remove bottleneck.
- 3. Front air intake and output on the side – implications for racks? Open.**
- 4. FEE-CC fast signal cable length tests using prototype CC board in a realistic environment.* Lab tests done – length 15m (Cat6b), 20m (Cat7), see Section 4 discussion.

5. *The status of the additional order of DAMC2 boards and an update of the modifications agreed to at the 14.12.2011 meeting should be distributed. Done expect 6 boards with all agreed to modifications in the summer, see Section 3.*
6. *A finalized set of requirements for LV and HV for the AGIPD milestone in the project plan should be provided. Done – but it may change later.*
7. *WP76 is expected to provide an interlock solution/concept and AGIPD the requirements. Again LPD and DSSC must be compliant with this solution – or suggest a better one! Statement not an action!*
8. *The conclusion was that the correction (calibration, cell leakage correction...) will be done initially in the PCL: WP76 provide the calibration framework and WP75 will organize the algorithm for the detector. Work has started.*
9. *The updated VETO specification was distributed after the meeting on the 21.12.2011 all FEE experts (and others) are requested to read it and provide feedback at the next FPGA meeting(?). Done, see Section 8.*
10. *We need some coordination to ensure that data transfer and formats converge for the slice tests, issues: with and without vendor specific features, train specific metadata added to the image data, etc. Started, see Section 12.*

3 Input from bi-weekly FPGA meetings – P.Gessler

The DAMC2 updated design (includes CC requirements: 99.3MHz clock distribution from CC...) is finished and going to manufacture. **Expect 6 ordered boards in 2-3 months.**

Timing board description note with our request included has been produced, however the conceptual design report (CDR) has not appeared and many points of interest to the user are not completely defined, e.g. definition of event content. Patrick is a member of the overall design group – this remains our lever.

The currently available prototype board is being replaced by the final(?) double AMC height version and should be available at end of year. The new board includes additional functionality (our changes PLL for TCLKA/B, a RTM transmitter SFP repeated) and should be cheaper by moving to a base design onto which additional functionality can be plugged (mezzanine) as required.

Fast signal cable length, FEE-CC, measurements were made during the last meeting. 15m is measured with no modifications, 20m with a modified receiver side – see Erdem's talk and measurement reports (in document repository, <https://docs.xfel.eu/share/page/site/xfelwp76/documentlibrary#filter=path/Projects/MicroTCA/RTMs/Clock%2520and%2520Control/Measurements>) for details.

The 10GbE and future developments in Ethernet, PCIe and FPGAs workshop is scheduled for 24-25.5.2012.

The MTCA.4 crate developed following Patrick's specs: horizontal board orientation, small (2U upwards), front-side cooling, EMI better power supply, etc. Expect to use this family of crates in DAQ and control environments.

4 Clock and control status – E.Motuk

Results of jitter tests are available in two reports (12/2011 and 2/2012

<https://docs.xfel.eu/share/page/site/xfelwp76/documentlibrary#filter=path/Projects/MicroTCA/RTMs/Clock%2520and%2520Control/Measurements>). The major jitter source on the fast signals is the DC-DC converter (400-500ps rms), using external 3.3V supply or additional filtering on the RTM this reduced to 60ps best case. New power/ground plane layout and improved filtering designs will be implemented on the next RTM production.

Cable length tests in the lab (24hr, 22bit commands interspersed in long periods of 0 and 1 traffic): 15m Cat6b. 20m is reached with Cat7 SFPB cable – here the biasing resistors had to be removed.

Discussion: Is the driver fan out chip too low power performance? **Martin will check higher power fanout chip and report in the FPGA meeting** If same pin allocation for a higher power could do an on board replacement. For planning 15m will be used, but we should have a safety margin 20-25.

Modifications to the DAMC2 hardware allowing the distribution of TCLKB have been made (MMC controlled setting of DAMC2) allowing the CC master to provide synchronous 99MHz clock to slaves.

Other status items:

- The f/w development using the DAMC2 startup project framework continues.
- Tests of the CC using the prototype timing board and a DOOCS jDDD controller should start soon.
- Ashley will start soon the CC interfacing to the XFEL control system.
- VETO distribution f/w will need to be developed.
- **The AC coupling is on the receiver side – Martin should check that this is indeed correct.**

Schedule:

- f/w tests including TR: May-June
- Final version developmet: Summer 2012
- Testing the RTM with an FEE: ?

5 AGIPD FEE status – P.Goetlicher

An update of the FEE design was given.

Power updates: sensor HV is now –ve; 2A per ASIC (500A for 1Mpxl); changed number of channels and their currents; and showed a solution with Wiener and Iseg. **Is Wiener/Iseg the standard solution - needs resolving and an agreement in place to ease later purchasing?**

Digital developments were reviewed based on the Medipix3 development which will be ready earlier than the AGIPD board, but is an extension of it.

Schedule:

- expect prototype interface FEE board Nov. 2012,
- overall mechanics summer 2013,
- and first prototype single module ASIC-FEE Jan 2014.

6 LPD FEE status – J.Coughlan

Manufacture of 20 FEMs is complete enough to build a 1Mpxl detector, but expect a complete 1/4 Mpxl "quadrant" detector with ASICs on site by the summer for use at LCLS. The 2 tile system was delayed but should be ready in the next weeks. Tim is currently working on interfacing the f/w and the intension is to get a 2 tile system at XFEL for us in s/w and f/w development. The f/w development by Sam implementing CC and VETO type protocols continues.

Sergey Esenov will prompt Tim regularly about the status of the TB lib.so interface to the XFEL control system which will be based on the LPD development – he will only start when he gets a positive go-ahead from Tim.

7 DSSC FEE status – T.Gerlach

The DAQ setup was described.

Some bit errors are seen during IO board tests of the control communication protocol (~2x10⁻⁹) used to internally sequence DAQ operations. The cause is being investigated, but is probably associated with connecting the PC to UART and JTAG interfaces.

Details of the IO board connections to the ASIC readout controller, MPRACE-2 board and sequencing f/w, and Patch Panel transceivers (QSFP+ to TB) were shown. Scope measurements of clock and other signals were shown.

Conclusion and next steps:

- driven by upgrade of IO board with manufacture Jan.2013
- ASIC test with ASIC test board May.2012
- Further f/w development
- Delivery of Kintex-7 evaluation board.

8 VETO specification and discussion – P.Gessler

The purpose of the discussion was to see if the VETO specification note could be accepted (version 0.4 from 28.3.2012). Issues discussed:

- adds the concept of a GOLDEN flag to VETO and NOVETO not in the original veto description contained in the clock and fast signal specification (2.10.2010 <https://docs.xfel.eu/share/page/site/xfelwp76/documentlibrary#filter=path/Projects/MicroTCA/RTMs/Clock%2520and%2520Control/Specifications>)
- variable delay protocol will be kept in.

Note that this discussion is restricted to LPD, DSSC and AGIPD. These detector's implementation of the specification may be restricted in comparison to with non 2D detectors. The post discussion, version 0.5 <https://docs.xfel.eu/share/page/site/xfelwp76/document-details?nodeRef=workspace://SpacesStore/b21416f5-0777-404d-819b-2404ff6a9e2f>, specification document contains a detailed description of detector behaviour. The per detector implementation view is:

LPD implementation:

- GOLDEN handling: GOLDEN or NO_VETO flagged pulse data are treated as identical and kept, VETO pulse storage locations are reused. The definition of which flags are kept (GOLDEN only, VETO only, or both) is configurable at the FEM and should also be configurable at the VETO unit (e.g. actively depreciate GOLDEN to NOVETO).
- Protocol: Fixed latency input is required.

DSSC implementation:

- GOLDEN handling: The GOLDEN flag is ignored and handled as if a NOVETO.
- Protocol: Fixed latency input is easier to handle, but variable latency could be implemented.

AGIPD implementation:

- GOLDEN handling: Can be handled in the detector head FPGA, but recommend that this be done in the VETO unit.
- Protocol: Variable and fixed latency input can be handled. Variable latency should not be dropped.

Thus 2D detectors prefer:

- GOLDEN handling in the VETO unit, depreciating GOLDEN to NO_VETO
- Keeping both fixed and variable latency protocols.

VETO specifications issues were addressed, but do we have a final understanding of what is being provided by both sides regarding GOLDEN and protocol latency.

9 Slice test and s/w status – D.Boukhelef

Hardware is being purchased and has started to be delivered which allows tests of data handling (processing and transfer) in a DAQ slice from FEE to offline storage. The h/w list on slide 5 is already out-of-date, the GPU h/w is now (May) working and the storage equipment to be purchased is now upgraded with delivery ~June.

The delivered h/w has been used to get a baseline understanding of standard setup configurations (buffer sizes, cpu affinity...) UDP and TCP throughputs and packet lost (UDP) various configurations were tested. First measurements wire (line) speed UDP with low packet loss ($\sim 10^{-9}$ for 8k packets, more measurements required!) .

The s/w used in the test are CLI tools (iperf, nperf...) and exfelSuite s/w framework devices. Rob's trailer mode transfer protocol is used for UDP s/w tests.

Schedule:

- Testing will continue using the delivered h/w.
- Perform tests with realistic (XFEL) time profile.
- Integrate additional h/w into tests as h/w arrives.

10 TB status – J.Coughlan

The first 2 ATCA demonstrator TB boards were delivered 29.3.2012. The boards have been powered, boundary scan performed successfully, and JTAG download of f/w to the 6 FPGAs performed. Component functionality testing is started. Senerath (layout) has now

retired but has written an extensive h/w design description which his replacement is now using. Currently no show stoppers are seen regarding the operation of the prototype boards. Enough components are available for 4 boards.

Schedule:

- Functional tests and f/w development at RAL (next months using Tim's s/w interface)
- Aiming for 1 board in Hamburg 7.7.2012
- Rate soak tests
- Continue with Mpxl system designs

11 TB slice and FEM firmware – R.Halsall

Test of the 10GE f/w developed are on-going, see slides for the configurations used. Work has started on the slice test demonstrator f/w required.

Schedule:

- Complete 10GE transfer test scenarios.
- Create and test data generator (video pattern) for slice test.
- Continue working on data formats, reordering, of data , etc.

12 Data formats – C.Youngman

Specifying data formats has started! First, with input from LPD then AGIPD and finally DSSC. Current concepts, issues and first guess formats were shown.

Schedule:

- Bring AGIPD into discussion
- Specify data transport protocol (for UDP Rob's trailer protocol)
- Specify data format DF-A out of FEE, DF-B out of TB (at PCL)
- Bring DSSC into discussion

13 Summary and actions list – C.Youngman

Last meeting actions status:

- 1. Front air intake and output on the side – implications for racks? Open.**
- 2. Expect 6 ordered DAMC2 boards in 2-3 months**
- 3. Martin will check higher power fanout chip and report in the FPGA meeting**
- 4. The AC coupling is on the receiver side – Martin should check that this is indeed correct.**
- 5. Is Wiener/Iseg the standard solution - needs resolving and an agreement in place to ease later purchasing?**
- 6. Sergey Esenov will prompt Tim regularly about the status of the TB lib.so interface to the XFEL control system which will be based on the LPD development.**

7. VETO specifications issues were addressed, but do we have a final understanding of what is being provided by both sides regarding GOLDEN and protocol latency.

14 AoB

The next meeting will be held in Hamburg on 12th July 2012.