Minutes of the Train Builder meeting (22.9.2011)

Location: Rm 5.21, AER 19
(24.5.2011 - CY)

1 Attendance list

WP76: N.Coppola, B.Fernandes, P.Gessler, B.Heisen (~pm), K.Wrona(~pm) and C.Youngman.
LPD+TB: J.Coughlan, R.Halsall and T.Nicholl (EVO)
DSSC: T.Gerlach.
UCL: S.Cook, E.Motuk and M.Wing
FEB: I.Sheviakov and M.Zimmer

The minutes, agenda, links to documents referenced and talks are reachable via:
http://www.xfel.eu/project/organization/work_packages/wp_76/daq/2d_pixel_detectors/meetings/ .

Actions are rendered bold. Items of importance are underlined.

If you do not have time or do not want to read the entire document, then skip to the summary and actions.

2 Last meeting actions and purpose of meeting – C.Youngman

Patrick Gessler has joined XFEL as team leader of the joint Detector (WP75) and DAQ and control (WP76) electronics group which has been formed to pool resources and improve coordination. See introduction talk slides for more details.

Last meeting actions status:

1. *WP75 and 76 milestone reorganization, note defining WP76 interface for pnCCD detector, update of number of detectors foreseen and their sizes.* **Information known but note(s) not produced, keep on actions list.**
2. *The possibility of using collaborating developers for additional FPGA development should be looked into.* Partick Gessler will coordinate FPGA work in his bi-weekly electronics development coordination meetings, see section 3.

3. *The LPD group need a few FMCs as soon as possible, in June, and should get the first that come of the production line.* Delivered
4. *It was agreed that Erdem and Martin would recheck that the requirements of the CC which we agreed to last September would be checked.* Checked and no show stoppers uncovered.
5. *The expected jitter on the TCLKA and TCLKB distributed clocks should be updated and transmitted to FEE groups.* Was this done? The jitter on TCLKA/B will reduce when the MCH switch is improved.
6. *A TPS VETO feasibility document should be produced which should address the overall VETO design.* The TPS VETO feasibility note (5.5.2011) was produced, see section 1 link, which showed that TPS VETO latency at the experimental hutches would be in the range 10-15 bunch intervals. The overall VETO design is being reviewed by Patrick and Erdem and requires input from the FEE developers, see section 5. The aim is to finalize the implementation and allow develop work to continue as the work load associated with the main CC reduces.
7. *The data format group should provide an initial definition note for the next meeting.* Not done, see section 8.
8. *Manfred will cost 300 PHYs, which replace those used in the current FMC production run.* 320 PHYs have been ordered, see section 10.

The aims of this meeting are listed below, see summary of meeting for results and other points arising:

- Check component status and delivery scedules
- Check work plan given the imminent availability of CC and TB prototypes
- Launch data content and format specification
- Launch configuration and s/w interfacing work
- Launch consolidation of VETO implementation

3 Update of timing, MTCA crate, FPGA programming for XFEL, etc. – P.Gessler

Commercially available MTCA crates were reviewed; 6U six vertical-slot and 8 or 9U twelve vertical-slot crates are available from Schroff and ELMA. Interesting for us, due to the small physical size but sufficient slot count, is a 2U six horizontal-slot crate which should be available soon provided negotiations with powerBridge distributer converge. Common problems (noise, airflow and filters, large ripple from power supply) are gradually being solved – the original Telco application environment was a closed computer centre, not a lab. Latest generation CPUs (i7) with on board HDD are now available (higher performance, lower power consumption, real hot plugability…). Low jitter MCH clock distribution on-going. The number and type of MTCA commercially available cards is increasing, e.g. TEWS lookalike DAMC2 boards, etc.

XFEL timing system board update:

- The X1 timing board firmware (1 at UCL, 1 at AER) now allows standalone running, but currently only with wrong frequency. When modified can be used for CC tests.
- Next steps regarding timing system: documentation CDR is specified end Oct. 2011
- A VHDL module is now available for work with CC development.

- The TR CDR is important as our requirements, which are known/approved by the TR group, must not disappear from the CDR. As Patrick is on the review board and attends the meetings, our input should not be forgotten. **Patrick should update us regularly on timing system CDR status to allow feedback.**
- X2 version will be double height and developed by the same group (MCS4 and Uni Stockholm). No changes are required by us - current status.

The FPGA expert group discuss/decide on issues relevant to MTCA development at DESY/XFEL on topics like: interfaces, tools, modules and organizational, etc.

- **There is a bi-weekly FPGA expert group meeting, all people interested should be on the email list, if you should be then send email to Patrick.**
- **Patrick will organize an additional bi-weekly EVO meeting to coordinate and track development discussions (interface definition, use of same modules, etc.) concerning CC, FEE and TB. The suggestion is Wed 11:00 CET.**
- Tools: now upgrading to Xilinx 13.2 and code repository is SVN. Policy all projects saved on central SVN repository (not the one used by exfelSuite).
- There is a worldwide accessible Wiki http://xfel-fpga.desy.de, ask Patrick for account and password.
- Rob's suggestion for tracking on top of SVN, called ~Track (TRAC) might be useful.
- Doxygen can be used for inline source documentation.

4 C&C status – E.Motuk

The status of firmware after refactoring to use the FPGA groups II-bus interface design was reviewed. All blocks (fast message, PCIe, etc.) needed for the CC are now implemented using II-bus, fine tuning will be required. **Need to check the LPD test module requirements for the prototype CC board.** The telegram data structure has not been finalized by the XFEL TR group, but a decoding module for decoding is programmed. This module will be made available to the rest of the FPGA group when TR group finalize definition.

The (first) prototype RTM board was shown (bravo!), initial power problems traced to a faulty DC-DC converter meant that 2 boards were delivered only this Monday. At XFEL additional power management tests were made yesterday with Vahan (MCS4) and I2C access works. However, the DC-DC converter gave only 1.8V and was fried during additional testing. Need to take component off and understand the problem, it could be that all versions of this component at the component mounter are faulty. Applying 3.3V directly to the rail worked showing all other components are OK. An external supply can be used whilst the problem is being fixed, main function tests will continue on return to UCL.

The CC schedule was reviewed, important points to note/do:

- RTM testing with an FEE (Jan.2012 on), final RTM hardware (Q2/2012),
- **When and what is needed for CC-FEE tests needs coordinating – at Patrick's bi weekly meeting?** LPD need CC for full 1Mpxl tests Q4/2012, they need a super module system, when?
- A test workflow and schedule for standalone operation based on LCLS type operation needs to be organized. **M.Kuster should specify when CC systems will be needed at external light sources.**
- Do we have enough, current version, TR and DAMC2 modules in view of increased test requirements? A quick count resulted in 6 additional, current version, DAMC2 units required (+LPD, +AGIPD, +pnCCD, +VETO, +2contingency.) **Manfred should**

work out details of supplying 6 additional DAMC2s and give us the suggestion a.s.a.p.

- **Final CC RTM hardware design is scheduled for Q2/3, how does this fit with the DAMC2 functionality update list? The CC side functionality DAMC2 update list has been given to the FEA, but no other group has submitted their requirements, we should review our list and submit again, expecting to receive the updated DAMC2 for the final RTM hardware stage. Manfred should outline the when/how solution.**

5 VETO specification update – P.Gessler

The talk addressed the following points:

- What is VETO for?
  - listed potential VETO signal sources
- How will VETO work?
  - showed schematic of how this would be implemented board/crate level and connections
- How is the VETO protocol defined?
  - Reviewed the in place specification defined in the CC Fast Signals definitions note “Clock and control fast signal specification” from 2.3.2011, see link in section 1.
  - Described the hardware interface (connectors, levels), the physical layer (data rate, source synchronous) and the two protocols for control and VETO.
- What has been done?
  - The status of the VETO work already done by the FEE developers needs to be established. A summary table of drawbacks and advantages, max latencies allowed will be generated and the VETO part of the original document updated as a VETO specific document**.** Maybe one can remove one of the protocols. **LPD and DSSC do not need the 1 bit 4.5MHz VETO decision notification message, they need the 99.31MHz encoded version only. AGIPD should confirm whether they need it or not.**
- What is missing?
  - Ideas for improving the protocol (VETO, GOLDEN, NO_VETO), whilst maintaining backwards compatibility, for current and future DAQ/detector systems were discussed. This point will be detailed in the next VETO specification note.
  - The fan-in/out implementation has not yet been specified. Using SFP+ serial links is a possibility. There is a DESY developed board (LLRF group?) with 16 SFP+ ports which could satisfy our requirements. The RJ45 battery used on the CC RTM could provide shorter range connectivity (fan-out).
- Next steps
  - **After feedback, from FEE developers, generate an updated VETO specification and work plan.**

6 TB status – J.Coughlan

The talks addressed the following points:

- Demonstrator ATCA card status

- Manpower – Senerath (layout/routing) retires March 2012, his replacement Edward Freeman starts November and has ATCA experience. An additional FPGA programmer is now added to the team.
- The layout is really finished; next step is routing requiring ~6 weeks.
- Clarifying long lead component delivery times is underway, order early and avoid delay
- It has been possible to add QDR2 memory to the layout, this could be useful for image manipulation (formatting…) and needs investigating
- control s/w – h/w interfacing being work on by T.Nicholl's group. Control via 1Gbps link on front panel, also available on the backplane bus.

- Delivery schedules
  - 6 PCB to manufacture Nov, boards on site for assembly in Dec.
  - Aim to deliver first board to XFEL April 2012 for slice test
    - **WP76 need 2 demonstrator board for slice test, i.e. one more!**
  - Prepare firmware in parallel
    - **The demonstrator firmware requirements needed for the slice test must be specified.**
- Plans for scalable multi-Mpxl systems
  - Using the demonstrator as a base unit the following multi-Mpxl systems which are currently possible (memory, transfer rates, etc.) are:

Detector Megapixels	Nr FEE Links	Nr TB ATCA	RTM & Switch Board	Memory Buffer per FEE MBytes	Data Rate GBytes/sec
1/4	4	1	NO	128	2.5
1/2	8	2	NO	256	5
1	16	4	YES	512	10
2	32	8	YES	1,024	20

  - A 4Mpxl unit requires larger capacity memory chips to be available in the allowed space allowed, use of more powerful FPGA, higher link speeds, etc. What does one do with all the data remains an interesting problem.

7 TB firmware – Rob Halsall

The talk addressed the following points:

- The 10Gbps test setup and f/w including monitoring modules.
- Described the UDP packet format and data content sent on the link from the FEM to the TB. Module specific information concerning the cell usage by frame, time in the storage cell, sent first followed by image data.
  - LPD's advance stage of development mean that they are driving the packet and data content format, but care must be taken to design the simplest and most elegant solution for all FEE types and TB users.
  - An iterative packet and data content design development was agreed to:
    - First step is to verify the use of the in place ordering requirement:
      - frame (contiguous blocks) ordered trains
      - Is frame description data interleaved with frames, at end, or beginning of train block?

        - ❖ Where is train description data – one block at beginning?
      - Then to verify/understand the contiguous frame blocks,
        - ❖ row major…
        - ❖ the pixel format: what to do with descriptive bits like AGIPDs 3 gain bits, for the different FEEs
      - Test that proposed solutions can be implemented within the FEE and TB resources available for LPD, AGIPD and DSSC.
- Note that the Chelsio T4 NIC can write received data directly into user address space at 95% of the 10Gbps UDP payload's theoretical throughput without packet loss, with correct setting of system side buffers.

8 Software status – C.Youngman

The talk addressed the following points:

- The current status of the software
  - ➢ A brief review of the software described in detail in the last meetings presentation was given
  - ➢ Device control software is currently being implemented for a number of show case hardware installations: Andor camera, Wiener/Iseg MPOD power supply, IPMI crate control, Beckhoff motor, APD single crate DAQ.
  - ➢ Feedback from the showcases will be used to verify the design, drive necessary modifications, etc. The test phase runs till end Oct. followed by 2-3 weeks of review, cleaning and modification.
  - ➢ <u>The device software development for CC and TB can start mid-to-end Nov.</u>
- Slice test status update
  - ➢ The slice test aims at verifying the DAQ/DM/SC architecture design by implementing a 1Mpxl wide slice for use from 1.1.2012 on
  - ➢ The 2 TB demonstrators required will act as input to the slice, initially they can be emulated by a PC/blade system.
    - Need to define control device, f/w and s/w interface
    - Need data format definition: real data input and block data
    - Device s/w and demonstrator needed Q1-Q2/2012
    - Need a contact name to define interface and work, Tim was nominated.
- Data formats and configuration as an introduction to the following discussion
  - ➢ **The requirement of specifying data formats and configuration requirements was detailed. This applies to all sub-systems: FEEs, TB and CC and will be coordinated by WP76.**

9 Firmware/software interfacing requirements/discussion for CC and TB

The discussion was relatively short and confirmed the action defined in the previous section.

10 FEA and AGIPD FEE status – M.Zimmer

The talk addressed the following points:

- 320 PHYs ordered and are scheduled by the manufacturer to arrive 21.10.2011.
- 50 10Gbps dual SFP+ FMC manufactured and tested: 3 at RAL, 1 ZE, 1 FEA and 45 can be picked up by RAL.

- A comparison of Copper v's LWL was made to look at cost saving potential. Moving switches to experiment and using DAC could reduce the cost, but more thought and research is required.
- The DAMC2 current and updated version issue was discussed in section 4.

11 AGIPD FEE status – M.Zimmer for P.Goettlicher

The talk addressed the following points:

- Clock Question and Rumour
  - Statement from Patrick: a continuous 99.31MHz on TCLKA will be delivered by the CC, and the 9/3MHz rumour has no effect on XFEL FEEs or CC.
- Analogue storage cell leakage impact
  - **The measured storage cell loss at AGIPD is sufficiently large to require correction, which means that the storage time of data per cell will have to be sent with the data. The best way to do accomplish this has to be defined in discussion on Peter's return.**
- Digital Readout (Igor) the design/prototyping is on schedule.
- How many detectors and when (very approximate) was described
  - One module requiring CC and PC data readout is scheduled for end 2012
  - Dual 1Mpxl detectors are now planned as first day installations for FXE, etc.

12 LPD FEE status – J.Coughlan

The talk addressed the following FEE FEM DAQ points:

- Status:
  - 2 more FEM DAQ boards were delivered in May, now 4 available.
  - GbE interface for Slow Controls now working.
  - Additional components tested: Temp monitor device. EPROM device
  - Embedded Processor Dual PPC running in SRAM
  - 1 GByte DDR2 module running at target data rate.
  - FEM working with single ASIC Test module.
    - ASIC controlled via local RS232 interconnect from PC.
    - ASIC data processed and readout via 10GbE link to PC.
    - Capturing up to 3 Images in single shot mode.
  - 10 GbE UDP/IP Tx FPGA firmware implemented and tested
  - Initial tests made with C&C test card
- Next 6 months:
  - Assemble remaining 2 FEMs (v1).
  - Minor changes for FEM PCB v2 (4 signals to change)
  - Manufacture 20 FEMs (v2) for larger systems.
  - Test FEM in "Shoebox" dual sensor system
  - Test @ 99 MHz XFEL clock (LVDS)
  - Extend FPGA design for final system operations:
  - Integrate ASIC readout with Embedded Processor block for continuous frame mode.
  - Implement dynamic vetoes from C&C system.
  - Migrate from local RS232 based controls to 1GbE Slow Controls system.

13 DSSC FEE status – T.Gerlach

The talk addressed the following points:

- DAQ: Concept, Prototyping and ADC Signal Timing
  - A max latency must be defined for veto w.r.t. the bunch being vetoed, it should be ~64 bunches.

- I/O Board: status and FPGA Firmware
  - Glue vapour bubbles formed on flex-lead during component soldering, special attention to handling the fle-lead is probably required.
- DAQ Test Environment: overview, FPGA firmware
- Patch Panel Transceiver
- Next Steps

14 Summary of meeting

The meeting was successful, the first prototype of the CC RTM capable of driving a 1Mpxl detector was shown and the TB demonstrator development is progressing well. Missing UDP packet and data formats and configuration requirements of the various sub-systems were addressed, it was agreed to produce specifications for these. A review of the VETO system was started and an updated specification will be produced. No show stoppers are seen.

The immediate time schedule looks like:

- Expect timing specification CDR from XFEL timing group end Oct. 2011
- Submit TB demonstration PCB for manufacture Nov. 2011
- Update VETO specification by Nov. 2011
- Start implementation XFEL side of CC and TB device s/w mid Nov.2011
- Next TB and CC meeting Dec. 2011
- Clarify DAMC2 and TR availability
- Begin testing of CC RTM prototype with LPD FEE, Jan 2012
- Deliver TB demonstration prototype boards Apr. 2012
- Finalize CC RTM hardware design Q2-Q3/2012

15 The Actions

The list of actions:

1. *WP75 and 76 milestone reorganization, note defining WP76 interface for pnCCD detector, update of number of detectors foreseen and their sizes*
2. *Patrick should update us regularly on timing system CDR status to allow feedback.*
3. *There is a bi-weekly FPGA expert group meeting, all people interested should be on the email list, if you should be then send email to Patrick.*
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6. *When and what is needed for CC-FEE tests needs coordinating – at Patrick's bi weekly meeting?*
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has been given to the FEA, but no other group has submitted their requirements, we should review our list and submit again, expecting to receive the updated DAMC2 for the final RTM hardware stage. Manfred should outline the when/how solution.

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15. *The measured storage cell loss at AGIPD is sufficiently large to require correction, which means that the storage time of data per cell will have to be sent with the data. The best way to do accomplish this has to be defined in discussion on Peter's return.*

16 AoB

The next meeting will be held in Hamburg on 8th Dec 2011. If you have problems with this date please notify CY by the end of September.