XFEL 2D Pixel Clock and Control System

XFEL Meeting, DESY

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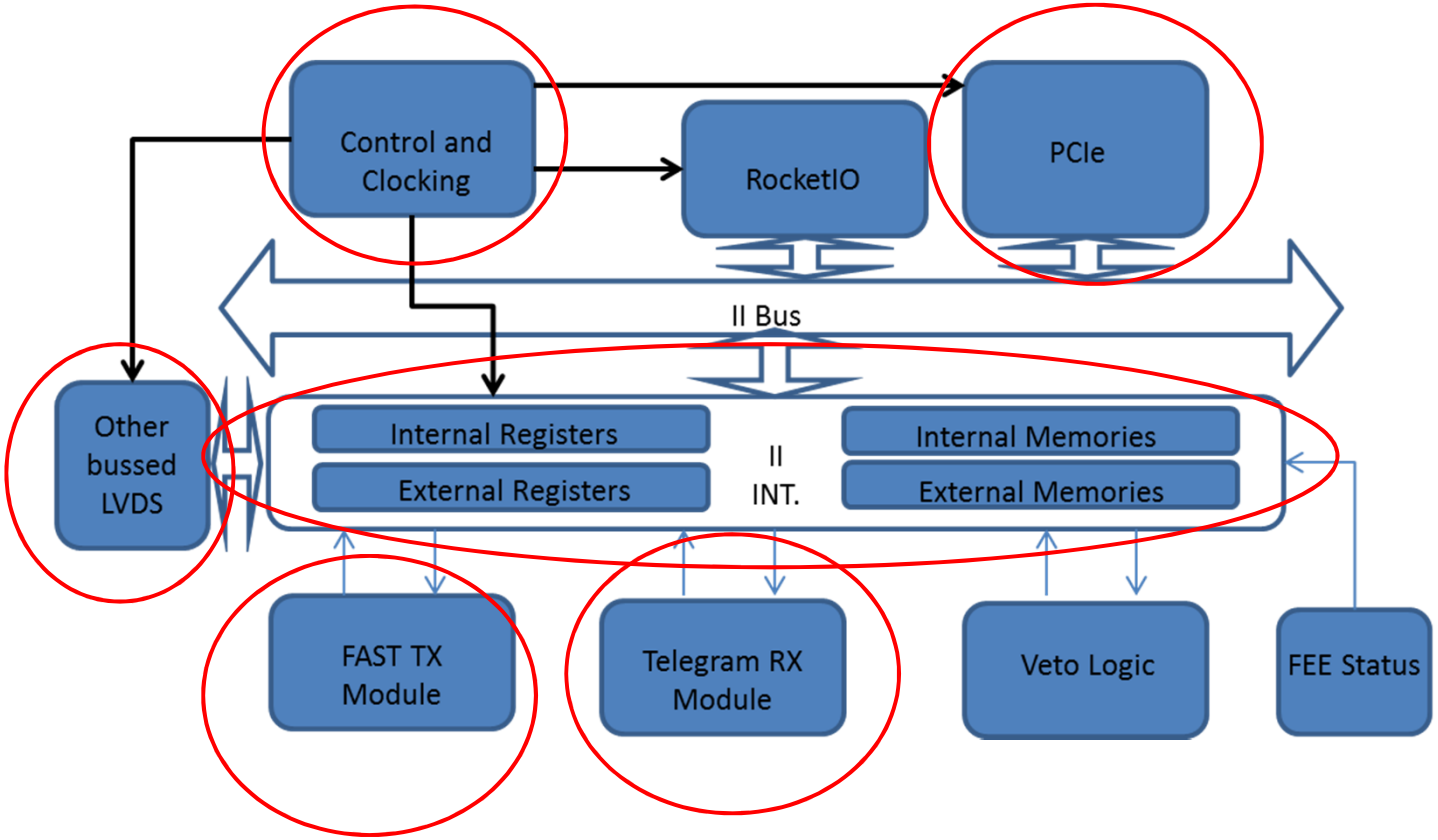
OUTLINE

UCL

- General status – Firmware
- General status – RTMs
- Schedule

General Status - Firmware



. No big changes in the firmware structure

General Status - Firmware

- Added some code to test the RTM modules
  - PRBS testing
- Minor changes to FAST message module
  - Capability of shifting the output clock
- Telegram module is going to tested
  - According to the latest TR specification and the firmware
- Control and clocking module's basic structure is implemented
  - Needs further fine tuning/improving with the RTM hardware
  - Also to be improved according to the FEE hardware

General Status - Firmware

- VETO logic part is still pending
  - CC firmware currently is not going to implement VETO selection/processing
  - VETO functionality will be fanout
  - To be implemented as 4.5MHz level and encoded 99MHz signal based

General Status - RTMs

- The powering on problems with the RTMs are solved
  - The very first board had a soldering problem with the DC/DC converter (by the manufacturer)
  - The second board had a soldering problem with the I2C address resistors (by us)
    - Input capacitance on the 12V input to the RTM is increased for more reliability
- An different external DC/DC converter circuitry is added to the first RTM
- The basic functionality of the RTMs were tested
  - Observing the clock from the onboard oscillator
  - Observing the clock from the backplane (MCH PLL)

General Status - RTMs

- Connectivity with the DAMC2 board over the RTM is verified
  - Various clocks and test signals generated by the RTM observed in the FPGA
  - DAMC2 set the multiplication factor for the 9 MHz clock
- FAST clock and data generation and transfer are tested
  - Connected the RTM to the dev board + test board through Ethernet cables
  - Correct FAST data and clock reception observed on the receiving FPGA (Chipscope)
  - All the output channels from the RTM tested
- Additional PRBS tests were done on the FAST data and clock links
  - Both methods of clock generation (onboard/backplane) tested

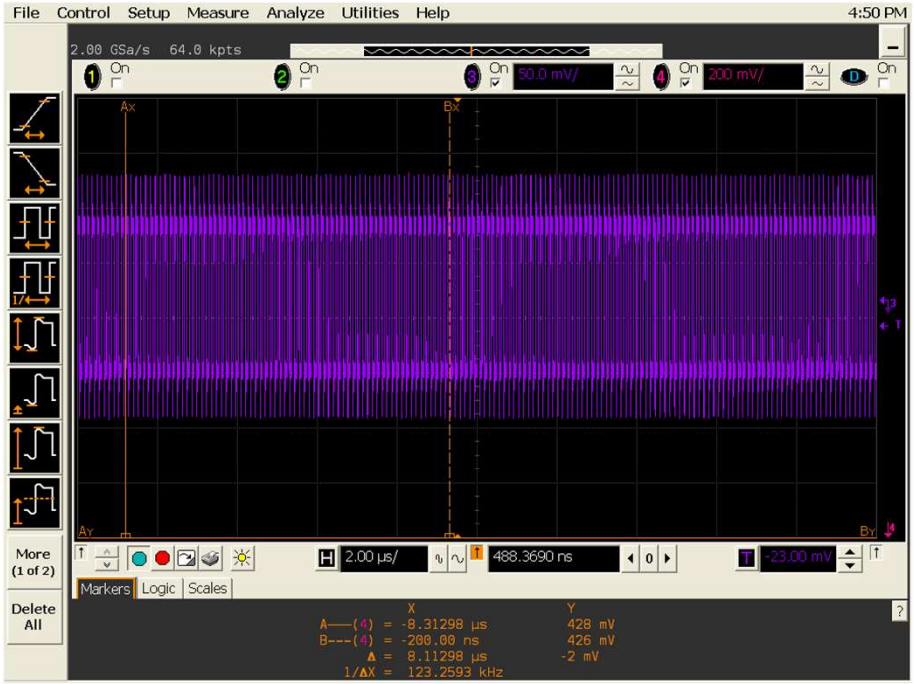
General Status - RTMs

- The tests showed no errors over a long period (~7 hours)
- The tests involved two dev boards as receivers on separate channels

- Two more RTMs were manufactured
  - One RTM for the DSSC team

General Status - RTMs

- Currently the generated clock quality is being evaluated
  - Tests in UCL and DESY to determine the clock jitter
  - Some observations so far – useful for the next revision of the RTMs
  - Scope probes showing some unreliable behaviour
    - ~ 67 KHz periodic noise
  - Observed the RMS jitter on the output clock as ~500 ps in DESY
- Wiki pages for the CC system were generated
  - A page for how to use the CC RTM
  - A page for the changes for the nest revision
  - A page for requirements for the next revision of DAMC2

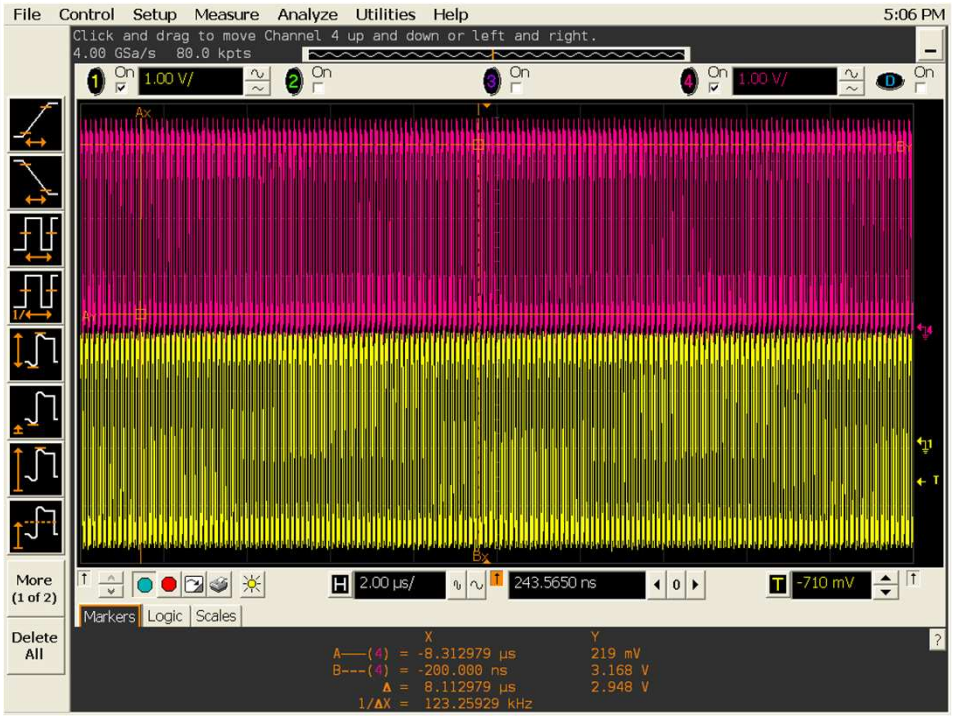


TCLK1 on DAMC2 output (8.192 MHz)

TCLK1 on the RTM (8.192 MHz)

Pink – After clock MUX 1 (non-PLL)

Yellow – After clock MUX 2 (PLL)



Schedule

- More tests on the clock quality *Now – End of December 2011*
- Testing and modification of the firmware in the light of the new TR CDR *Now – January 2012*
- Development of the next revision *From Q2 2012*
- Testing the RTM with an FEE *From January 2012*