LPD FEE Status

- **LPD status, DAQ related**
  - ASIC due for 130 nm shared wafer submission in May
  - FEE (FEM) prototype (fully functional) manufacture (2 boards) August
  - 1 x Super Module (1/16 = 1 FEE link) to test with readout Dec 2010

- **FEE (FEM) card design (Saeed Taghavi, Chris Day)**

- **Firmware & Embedded S/W (Rob Halsall, Sam Cook, John Coughlan)**

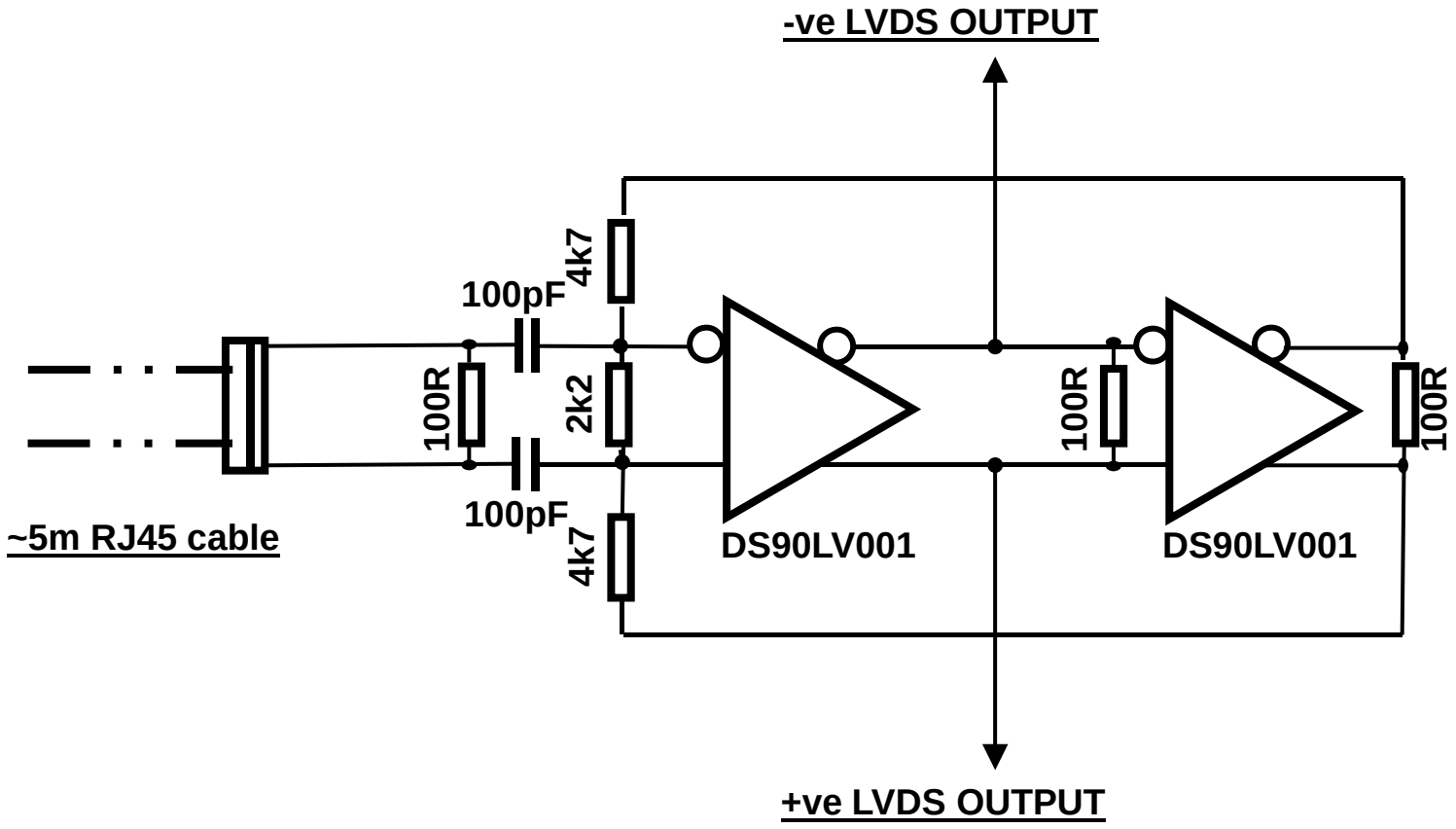
LPD FEE (FEM) Hardware

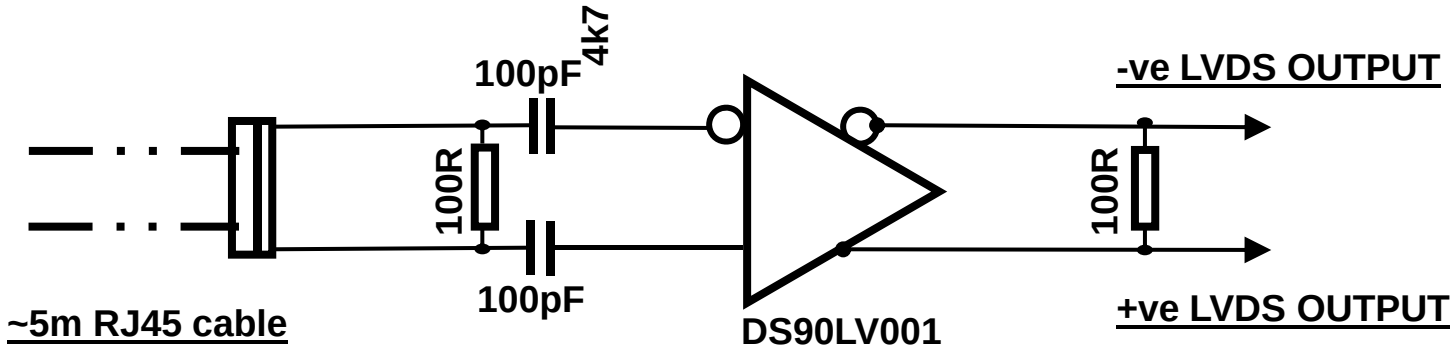
- Schematics Design review
- Implemented changes

- Integrate with backplane power cards
- Larger SRAM for PPC code
- Added C&C interface (keeps option of Manchester encoding)

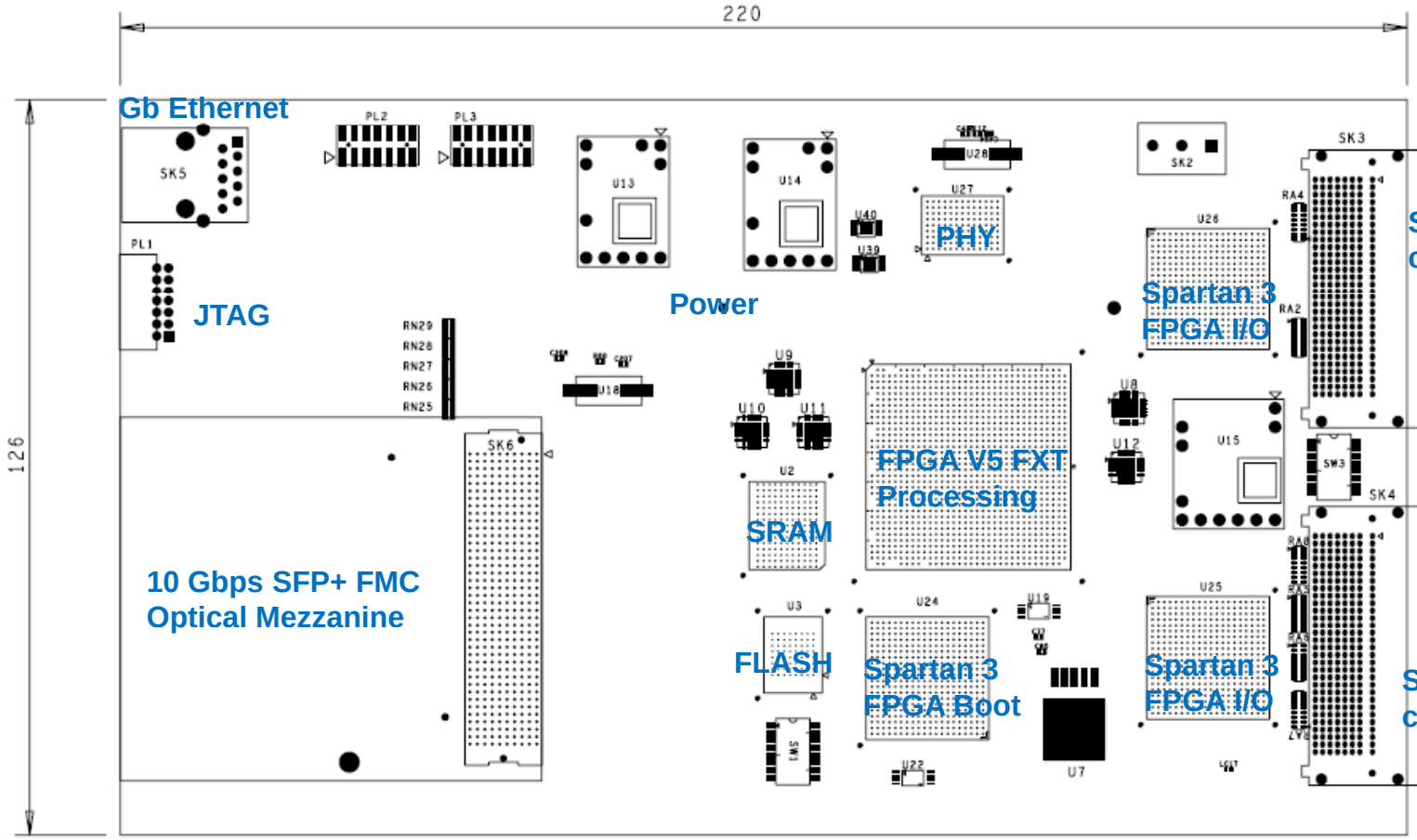
- PCB design

- Layout and Routing now in progress (delayed by ~ 1 month to do backplane and feedthrough cards)
- Taking particular care with DDR2 memory interface

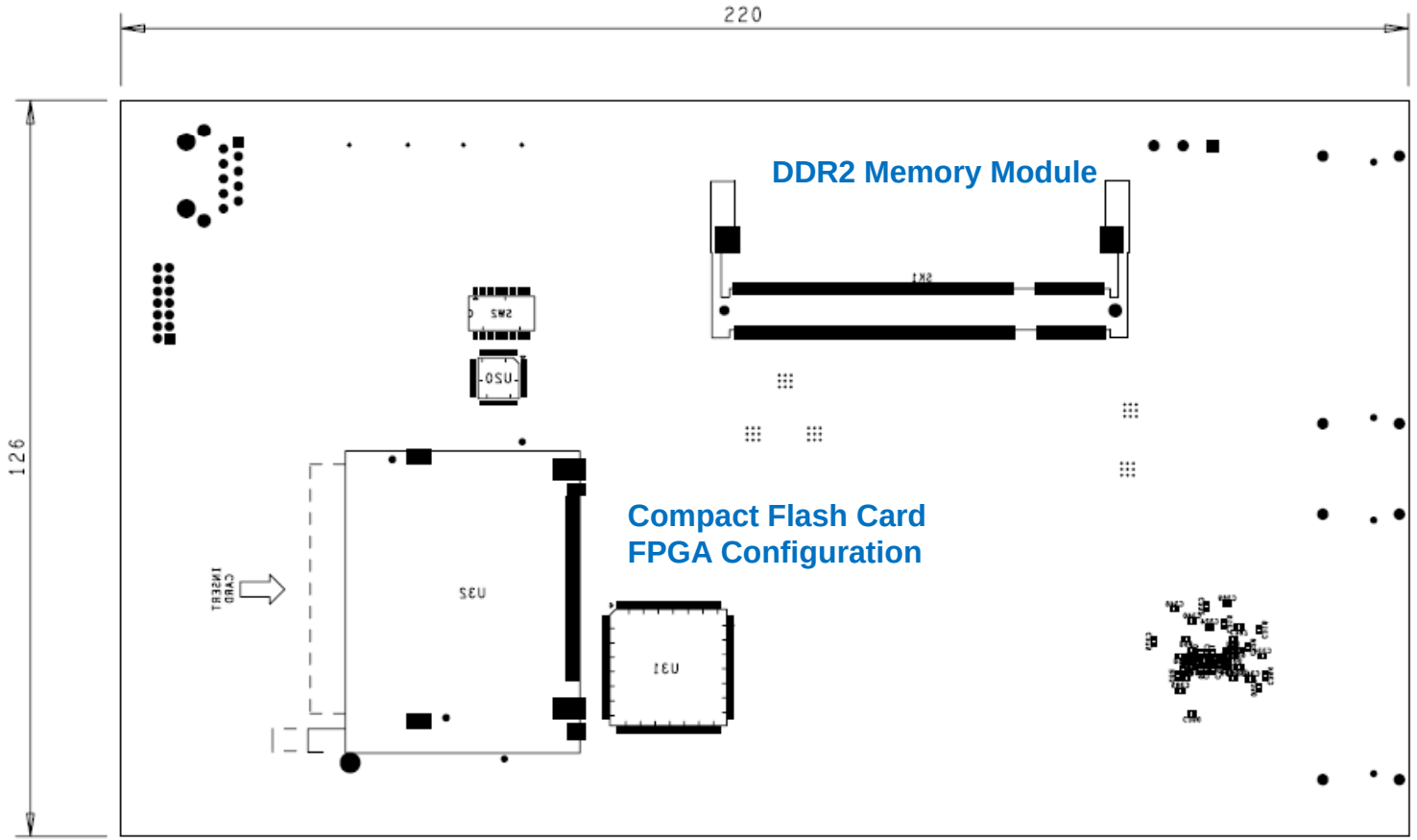




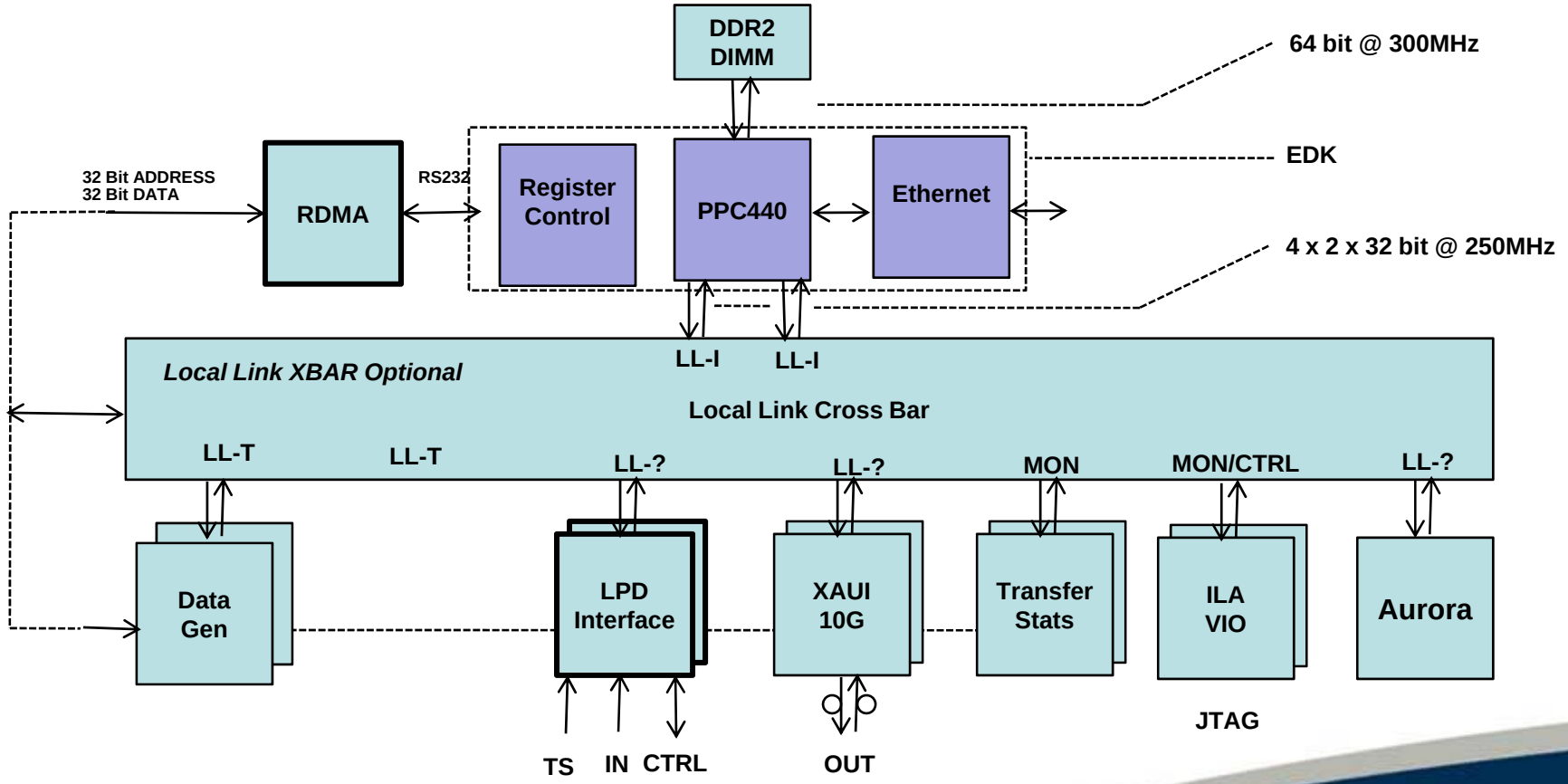
LPD FEM Layout in progress. TOP



LPD FEM Layout in progress. BOTTOM



Top Level Firmware Design - 1



Framework reused on Train builder

LPD Interface Firmware

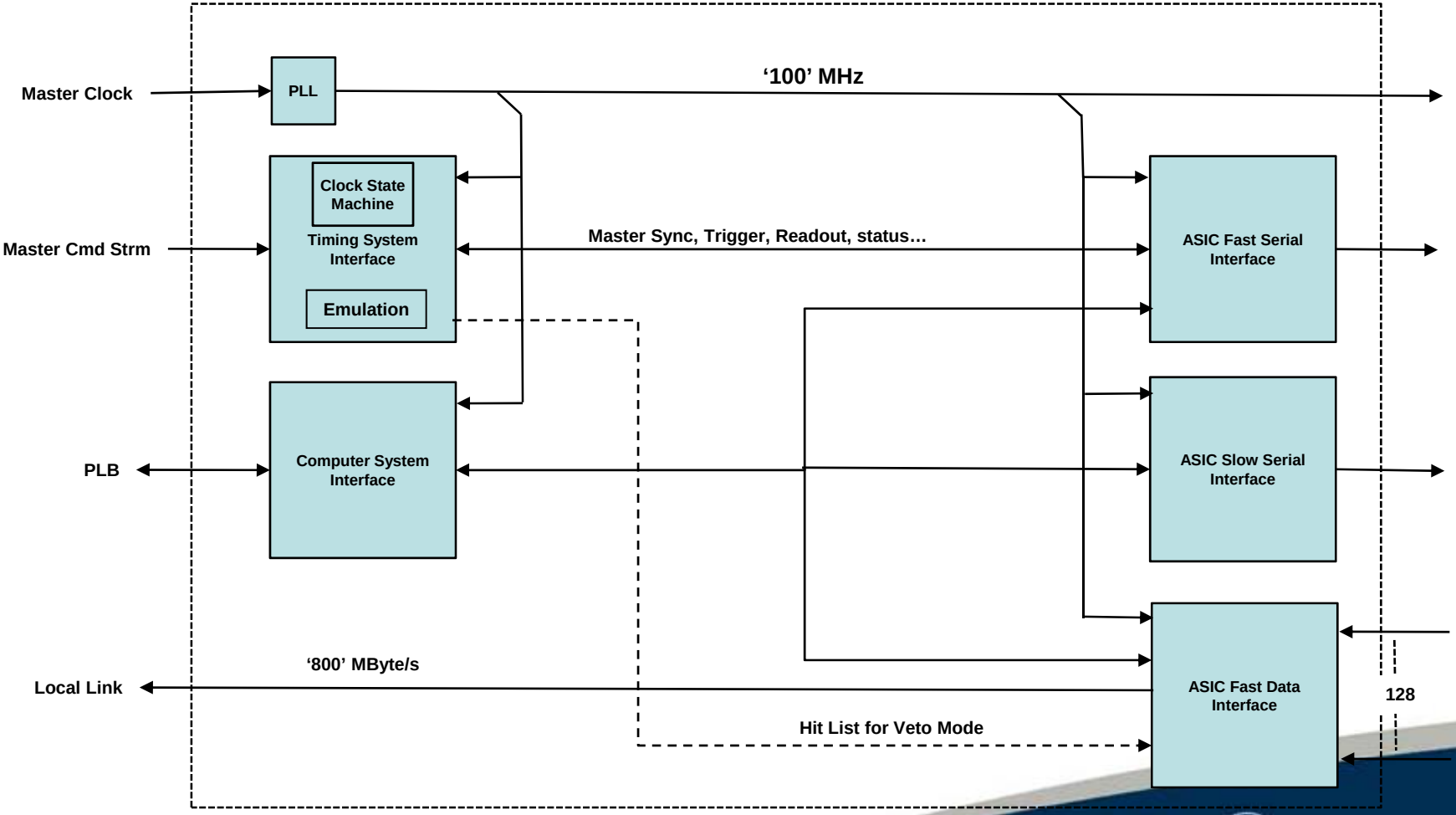
- ASIC Data processing. Rob
  - Simplest 1 of 3 gain selection.
  - No reordering of ASIC pipeline.
  - Keep Raw data mode for test.
  - Simulated ASIC data for test.

- C&C Interface. Sam
  - Cmd Decoder
  - ASIC cmd generator
  - C&C simulator for test

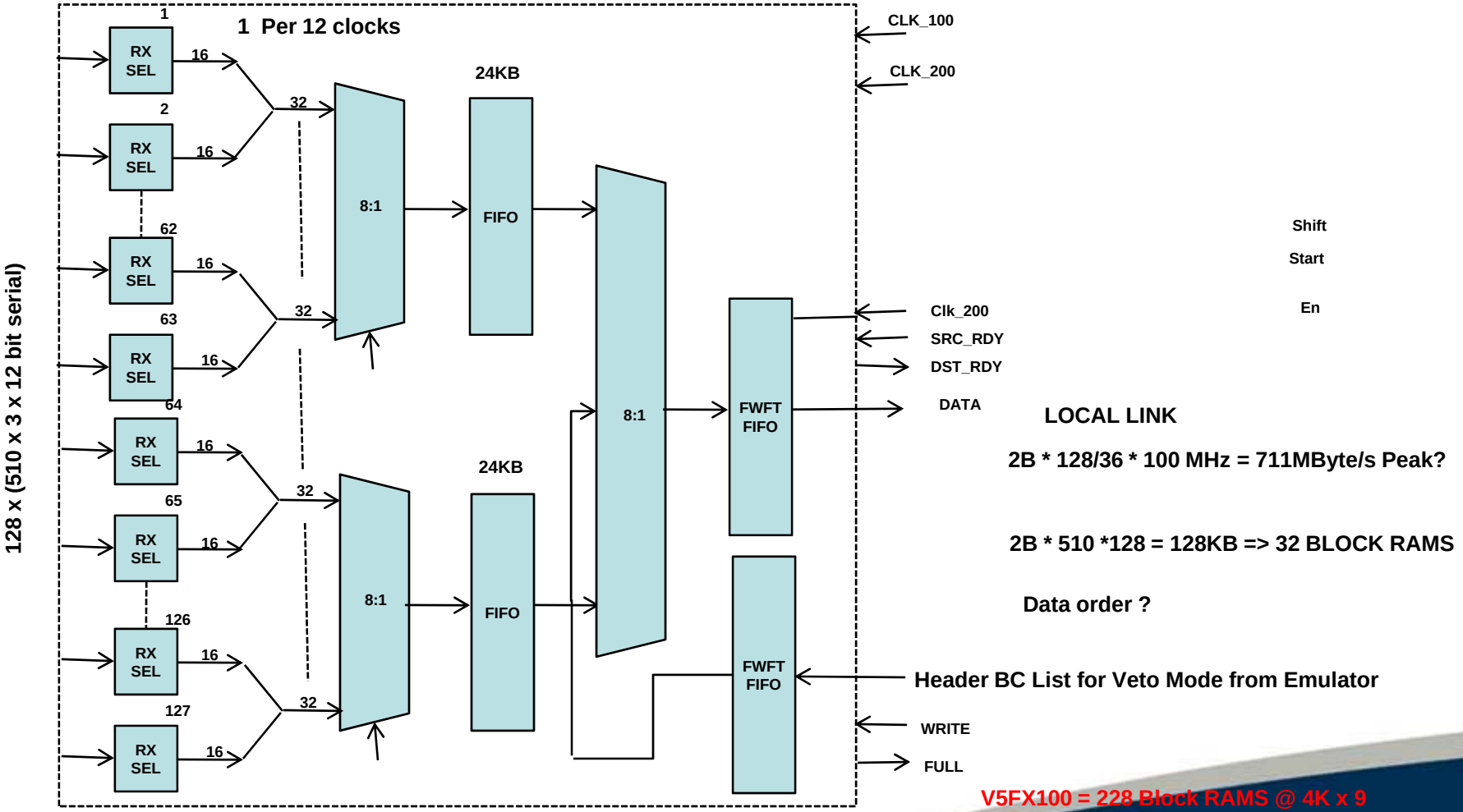
- PPC Embedded S/W. John
  - DDR2 Memory
  - Internal Register control (RS232 channel)
  - Ethernet control & monitor.
  - Keep interface compatible with Offline S/W work package (Tim Nicholls)

- Standalone FEM Firmware for testing prior to integration with LPD, C&C etc
- Firmware Framework to be reused on Train builder

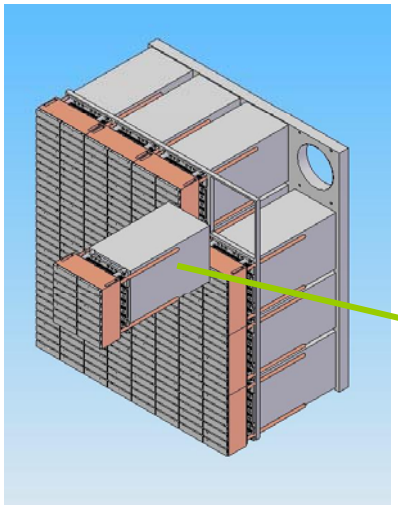
ASIC Peripheral: Overview



ASIC Data Rx Block: top



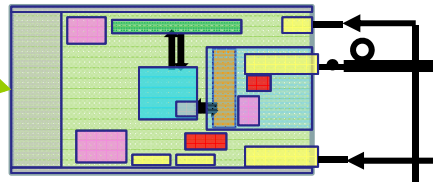
Spare Slides



LPD Detector

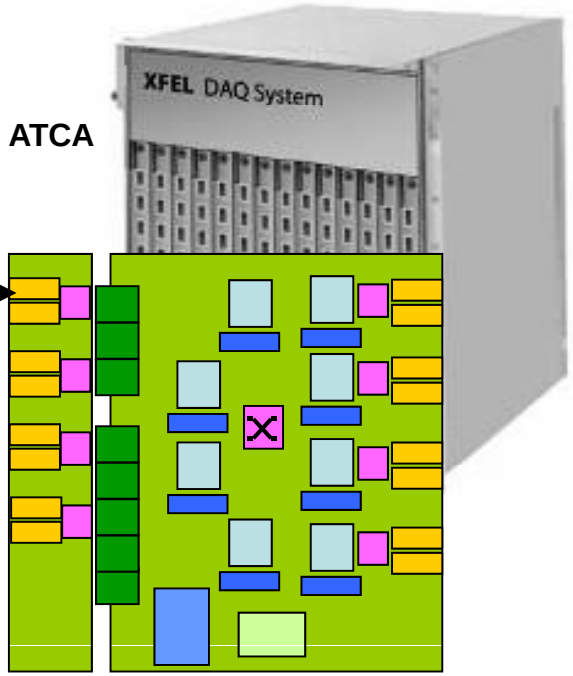
Front End DAQ

FEM (x16 modules) with
10Gb SFP+ Optical FMC



10 Gbps Optical Link

ATCA



C&C Fast
Timing
Signals

Gb Ethernet
Slow
Controls

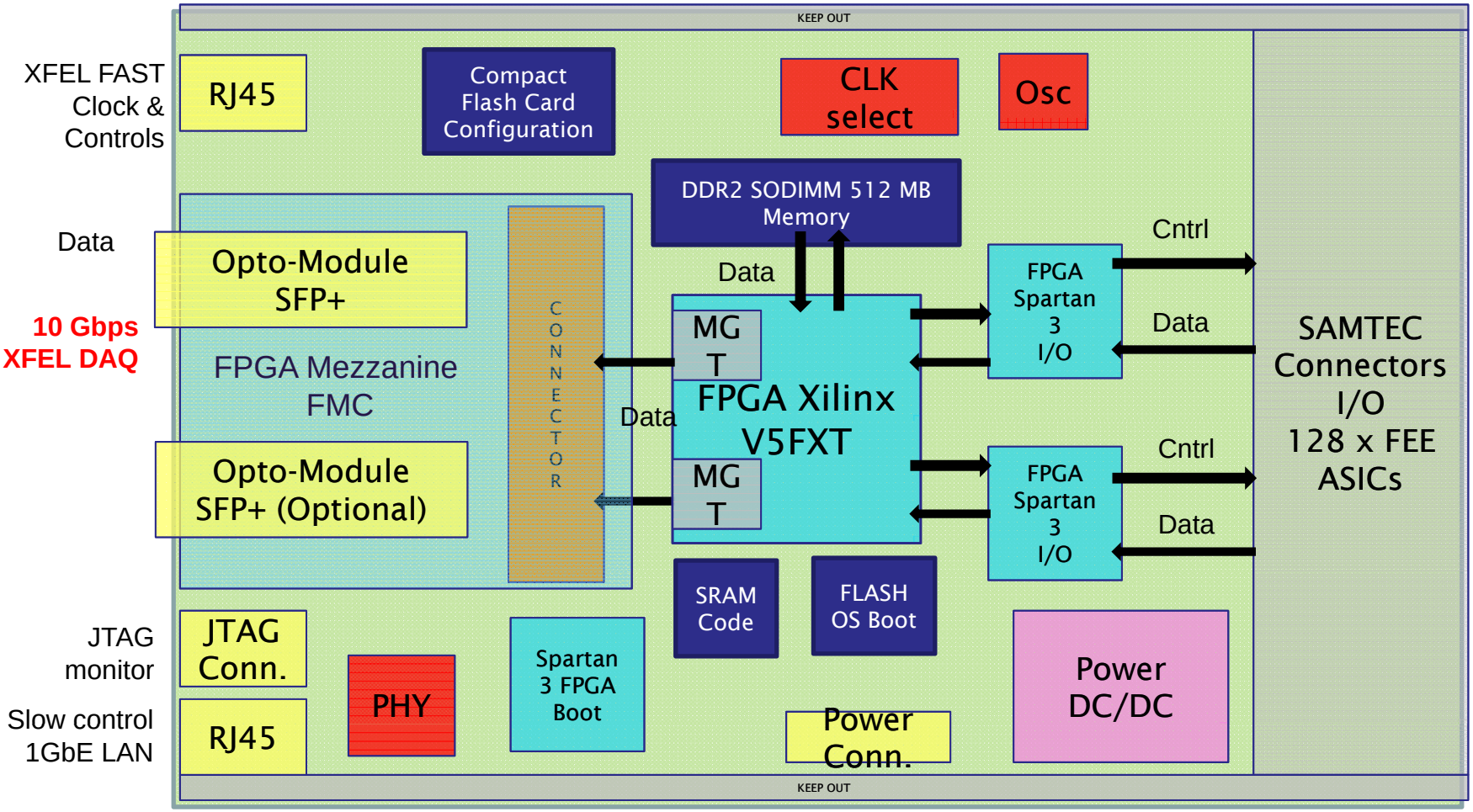
XFEL Common
Clock & Controls

MicroTCA

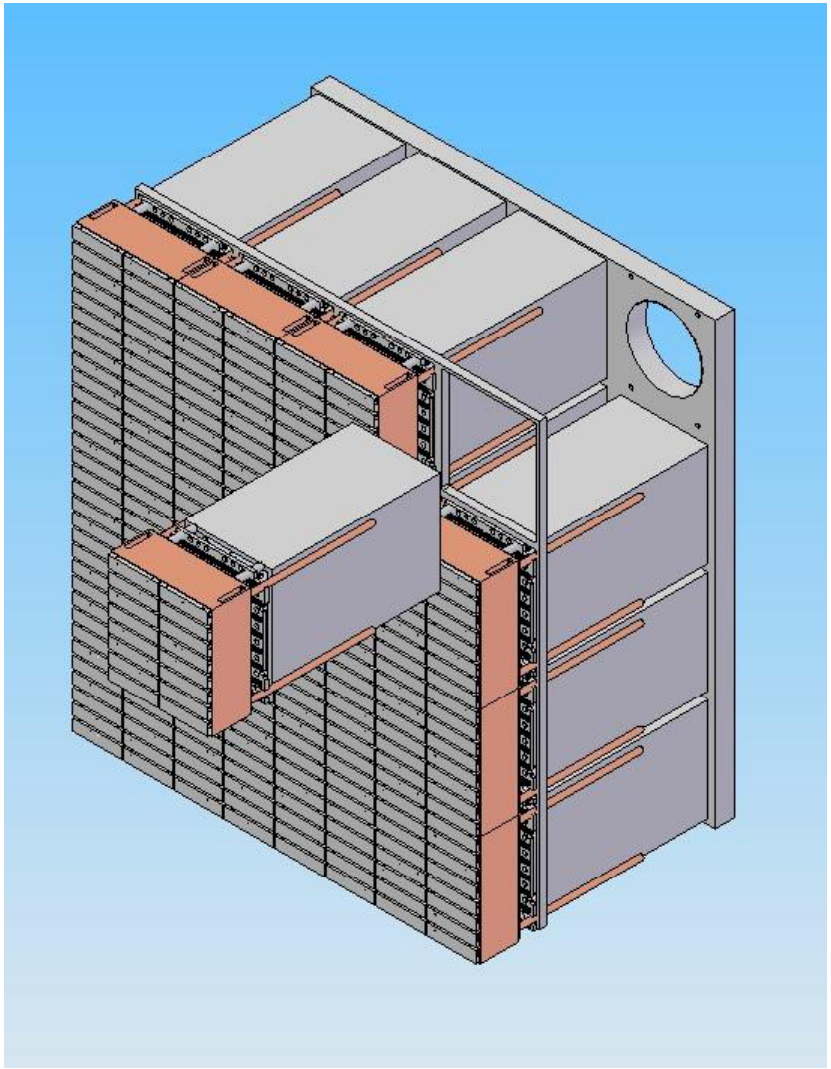
XFEL Common Readout
Train Builder switch

Science & Technology Facilities Council

LPD FEM Components



New LPD mechanics for Flat Panel geometry



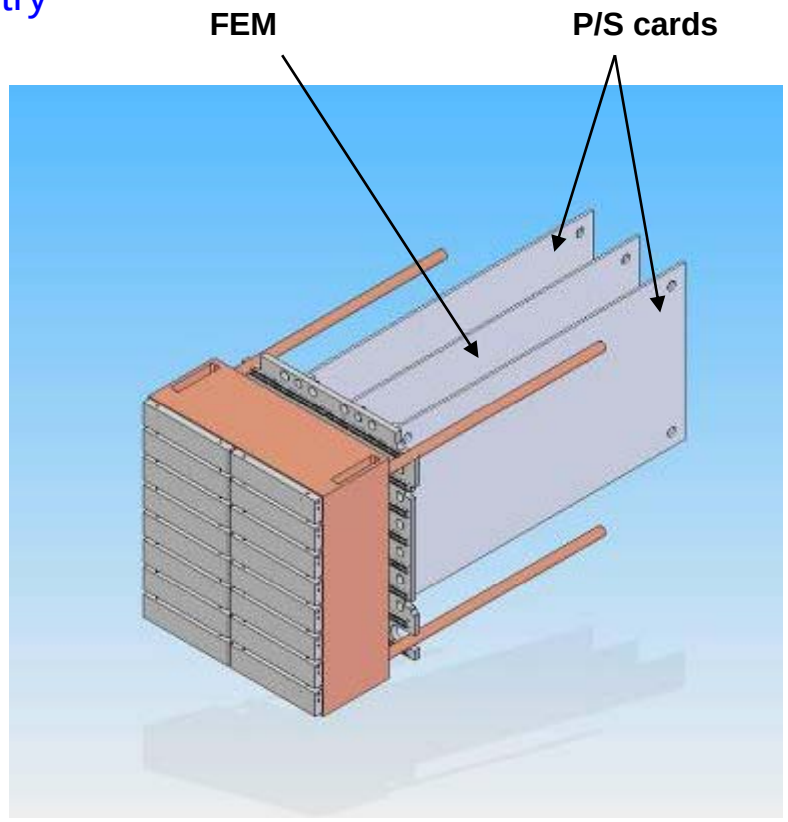
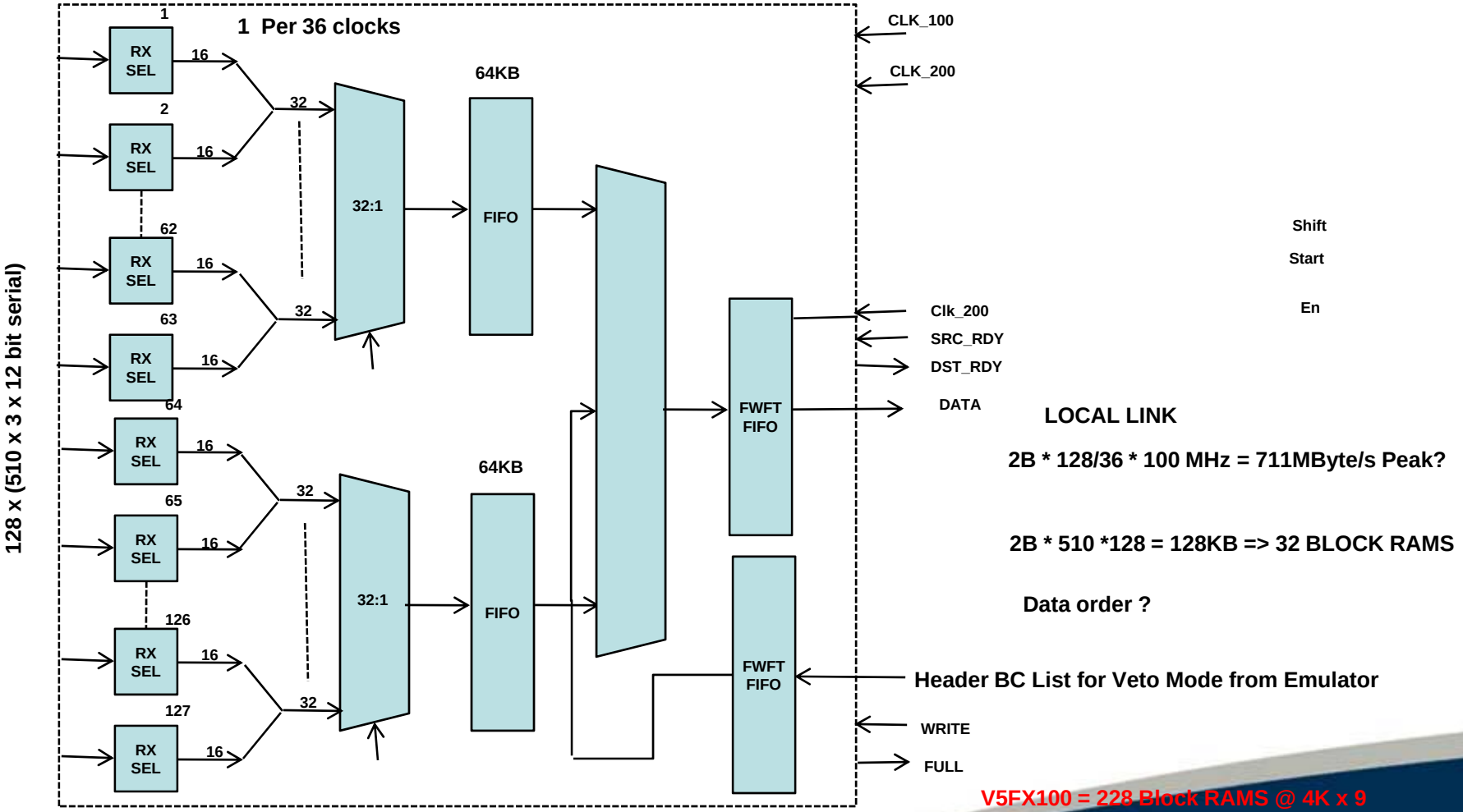


Figure 24: Front view of proposed super-module design

ASIC Data Rx Block: top



LOCAL LINK

2B * 128/36 * 100 MHz = 711MByte/s Peak?

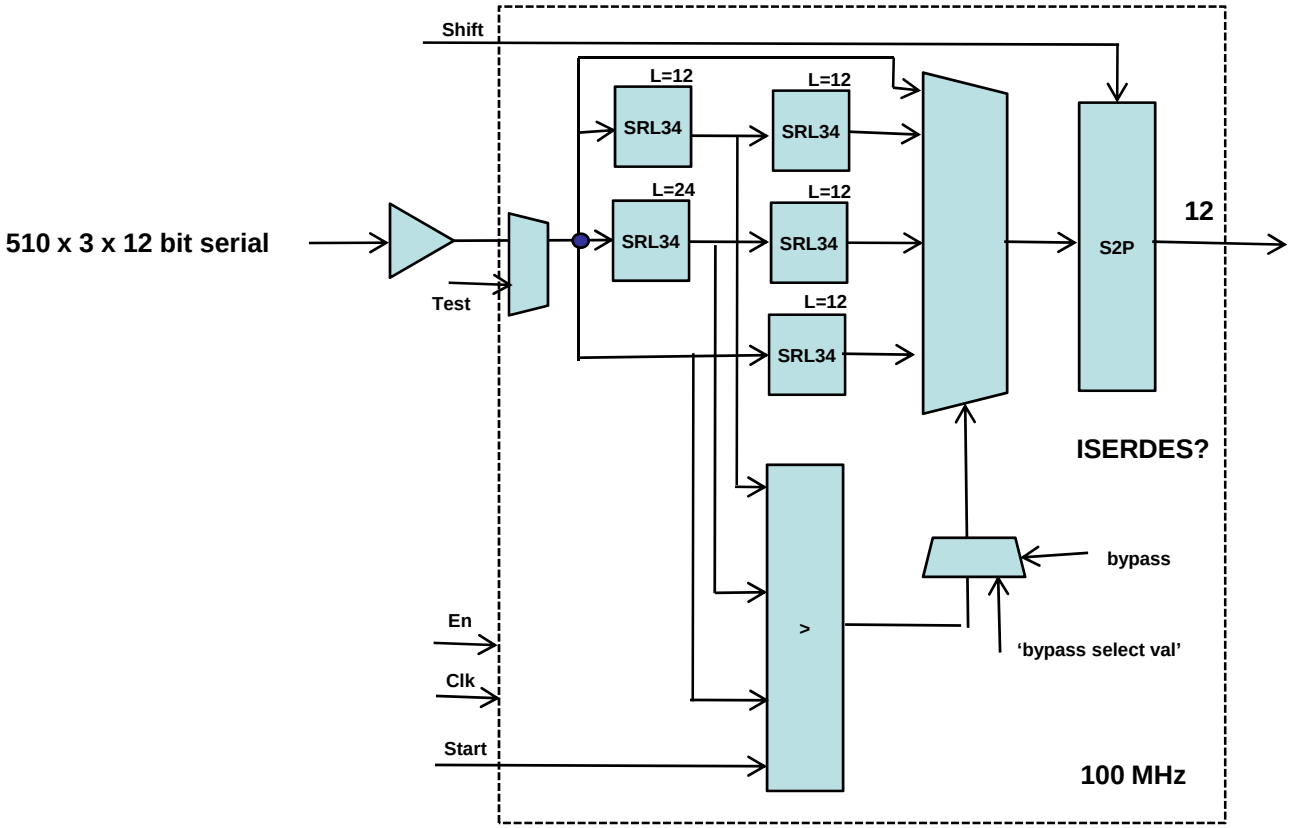
2B * 510 *128 = 128KB => 32 BLOCK RAMS

Data order ?

V5FX100 = 228 Block RAMS @ 4K x 9

3 * 2B * 510 *128 = 384KB => 96 BLOCK RAMS

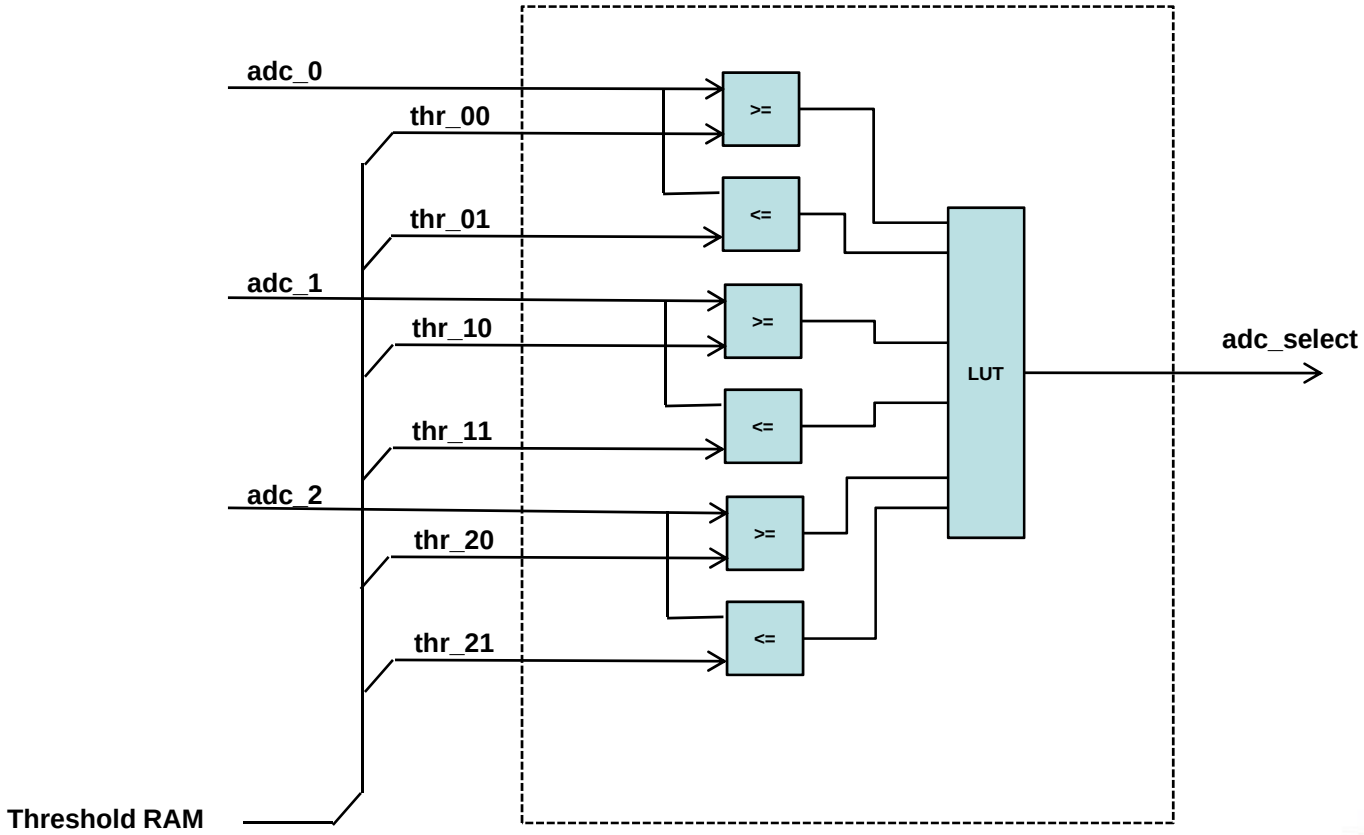
ASIC Data Rx Block: Serial Comp



1 result every 36 clock cycles or
2 result every 36 clock cycles or
3 results every 36 clock cycles

Low FPGA slice count = 9

ASIC Rx Block: ADC Gain Select



Thresholds for the full pipeline => 512 x 128 x12 bits => 21 block RAMS per threshold

Gain range decision - simple