XFEL 2D Pixel Clock and Control System

Train Builder Meeting, DESY

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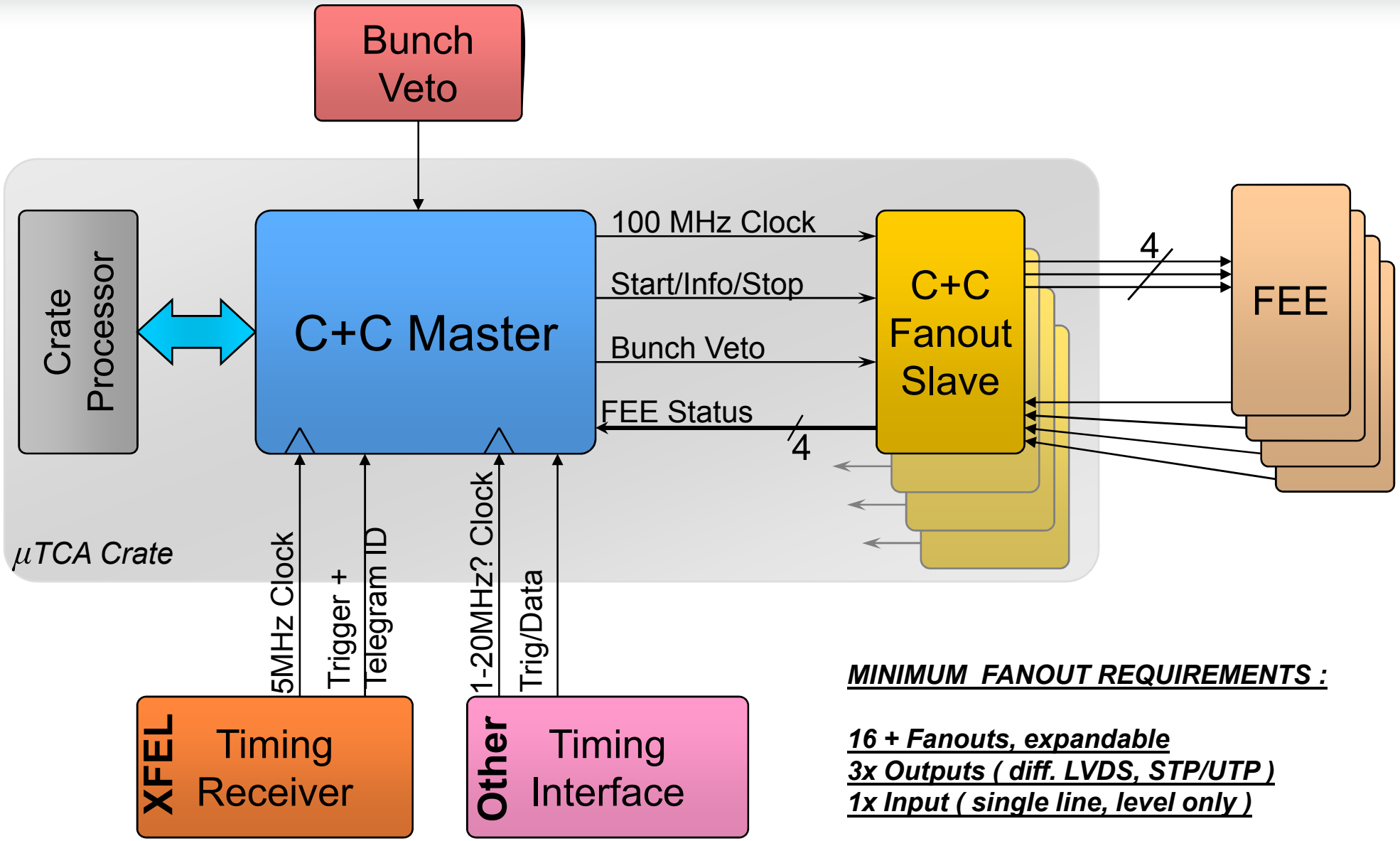
EDMS Nr.: D0000000001535951 Rev: A Ver: 1 Status: Released Dat.: 25.10.2009



MINIMUM FANOUT REQUIREMENTS :

16 + Fanouts, expandable
3x Outputs (diff. LVDS, STP/UTP)
1x Input (single line, level only)

Fast Commands -1-

UCL

Three Fast Command Lines :

- Fanned out to all FEEs via C&C Fan-outs
- Same cable lengths
- No individual adjustable delays
- AC coupling on FEEs : Opto/magnetic or Balanced codes ???

1) ~100 MHz CLOCK :

Integer multiple of the incoming ~5 MHz clock from T.R.

PLL-ed to the incoming 5 MHz clock

Un-interrupted

Fixed phase relationship to the 5 MHz clock ???

Fast Commands -2-

UCL

2) START-TRAIN / TRAIN-ID / BUNCH-STRUCTURE-ID / STOP

Synchronised to the 100 MHz clock

Fixed phase relationship to the 5 MHz clock ???

a) START : 110 = 3 bits

Start pulse to start about ~ 15 msec (programmable in 200 nsec steps ???) before the train arrives

b) TRAIN-ID : = 32 / 64 bits ??? - CheckSum / Parity ???

[from 'XFEL timing system' - K. Rehlich :

The train number is a unique number. From the DAQ point of view it should never repeat and should continuously count (e.g. Event number = GPS time divided by something) even if it requires more that 32bits.]

- Does this include Trigger Type ???

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Fast Commands -3-

UCL

c) BUNCH-STRUCTURE-ID : = 16 bits

– CheckSum / Parity ???

[from 'XFEL timing system' - K. Rehlich :

The bunch pattern format has to be defined, but it will be more than just an on/off bit per bunch as it must include beamline information (not all bunches go to all beamlines), etc…

- Assume maximum 3000 bunches per train

d) STOP : 101 = 3 bits

Stop pulse

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Fast Commands -4-

UCL

3) VETO BUNCH : ???

Synchronised to the 100 MHz clock

Any phase relationship to the 5 MHz clock ???

a) VETO PULSE : 11 = 2 bits

b) BUNCH-ID : = 12 bits (max. 3000 bunches/train)

c) -reserved- : = < 6 bits ???

[From new 'C&C Veto Definition' :

The output signal satisfies the following : The output is a 100 MHz clock allowing 20 bit payload. 12 bits are used for bunch number encoding, additional payload bits are reserved for later use. The output is synchronised (by the VU) for use at the FEE to the 5MHz bunch clock in the same way as other C&C fast signals]

NOTE : We may only have 19 or 18 bits available ???

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Fast Commands -5-

UCL

1) ~100 MHz CLOCK

2) START-TRAIN / TRAIN-ID / BUNCH-STRUCTURE-ID / STOP

a) START :	110	=	3 bits	}
b) TRAIN-ID		=	32 / 64 bits	} ~86 bits =>
c) BUNCH-STRUCTURE-ID		=	16 bits	} 860 nsec max
d) STOP :	101	=	3 bits	}

3) VETO BUNCH

a) VETO PULSE :	11	=	2 bits	}
b) BUNCH-ID		=	12 bits	} MAX. 20 bits
c) -reserved-		=	< 6 bits ???	}

FEs Status Feedback

- ***STATUS FEEDBACK from all FEEs :***

  Each FEE plugged-in & powered-up

  Status only : OK = ?? MHz clock

  ERROR = high / low / floating...

Network Messages from C&C

UCL

- RUN CONFIGURATION

As received from T.R. as raw “Telegram” :

- Trigger Number - same as Train ID (32-64 bits) ???

(does this include Trigger Type ???)

- Bunch Pattern

- ???

- ???

Questions -1- :

- *Is there any RESET from C&C Controller (blade)*

  e.g.. to be sent as FAST COMMAND on START / STOP line to FEEs

- *Run Configuration*
- *Snapshot(s)*

  are not C&C generated messages – should come from "Run / DAQ Controller"

Veto Unit Questions / Comments -2-

Presume 5 MHz Clock and "Train-Start" (?) are common to Veto Detector and to Veto Unit

2 scenarios :

1) **Veto sent synchronous to bunch it vetoes**
   - Don't need to decode bunch-id bits if fast enough
   - Synchronised to 5MHz
     - No start-bits etc for serialised bunch-id
   - Inputs bunch/train phase aligned using delays
     - Synchronised to 100 MHz clock
     - 10ns steps for bunch alignment (?)
   - Single bunch-id counter used on all inputs
   - Time-in one input using common "Train-Start" or "Test-Veto" signal
     - Veto Detector sends veto on bunch 0
     - VU counts delay/offset between "Train-Start" / "Test-Veto" and "Veto-0"
     - Can time in all other inputs to first one
2) **Veto un-connected in time with bunch**
   - Send vetoed bunch-ids ASAP
     - On any 100MHz clock
       - Needs start-bit
   - Timing-in can be done independently for each input
     - Complicates duplicate checking logic a little
   - Could use start-stop line for this

Note : At some point proper timing in with a single bunch will need to be done …

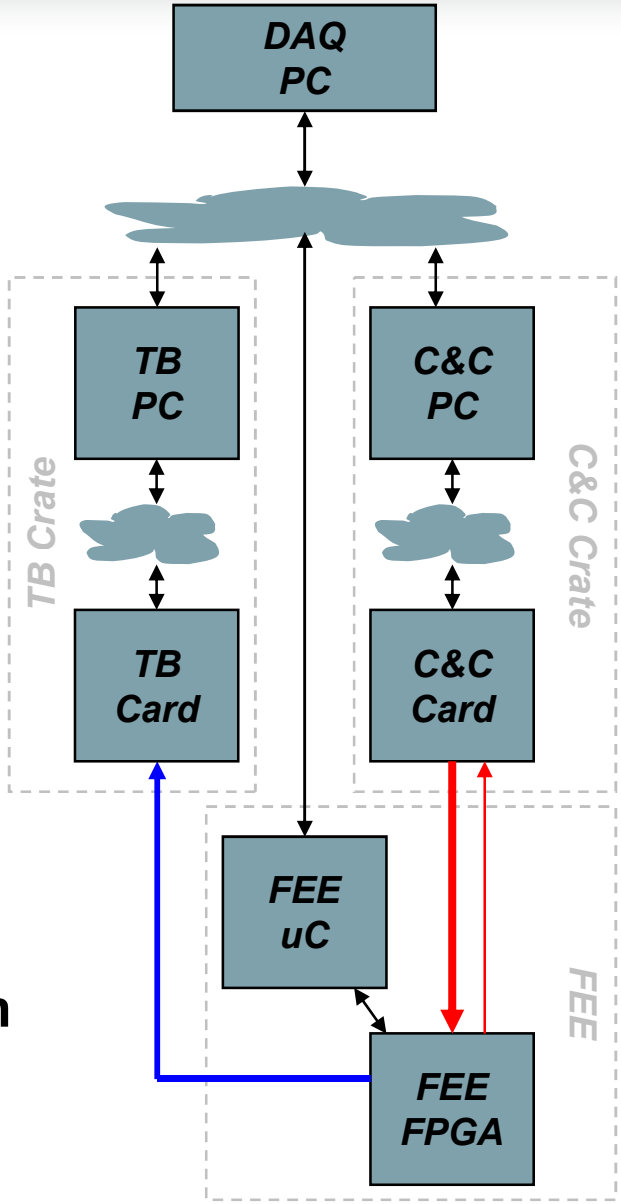
ARM CPU / Network messaging

Summarise our understanding of the system :

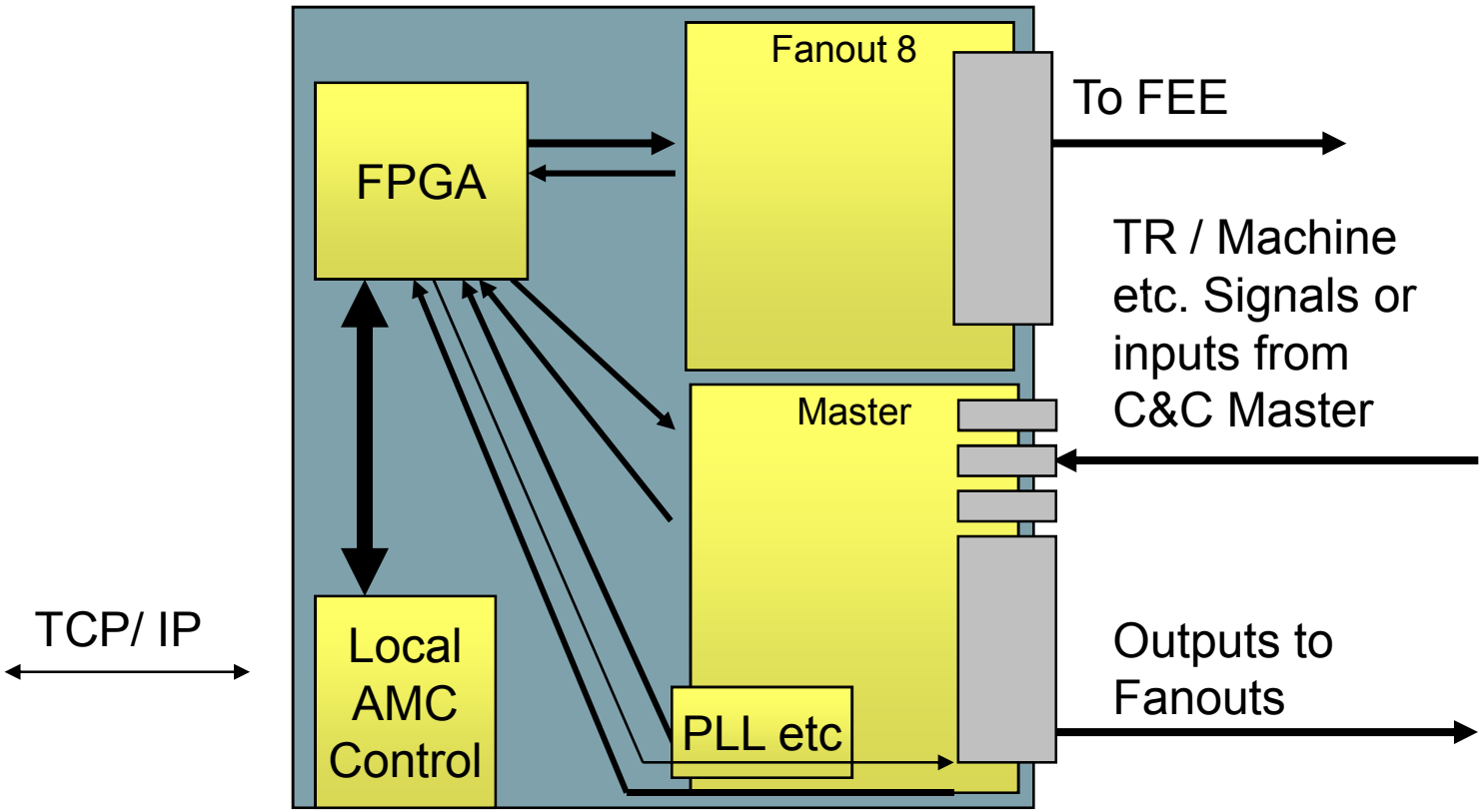
- Control in centralised, but not on the C&C PC
- C&C PC takes care of requesting/accepting/fetching info from C&C Card/s
  - This includes snapshots and train info from TR
- DAQ PC requests/accepts/fetches info from C&C PC
- C&C Card communicates with FEE FPGA

Outstanding Questions :

- Should the C&C have a command for resetting the FEE uC ??
  - Or should this be a special power-supply line reset ??
- The doc implied the FEE requesting a snapshot from C&C – really ??



c) Single integrated card



End…..