AGIPD

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- Clock frequency
- AGIPD Internal slow control
- Bunch reject
- Summary and question communication AGIPD-C&C

System clock frequency

Considerations: - bunch clock ≤ 5MHz
A bit larger should be not forbidden by the design

- AGIPD: ADC-clock ≤ 50MHz (not larger)
ASIC (slow-reject, etc.): ≥ 100MHz
(preliminary)

Proposed PLL: IDT: ICS527-01

$$CLK_{generated} = CLK_{input} \frac{N_{fdW} + 2}{N_{rdw} + 2} \qquad N \in [0,127]$$

System clock frequency

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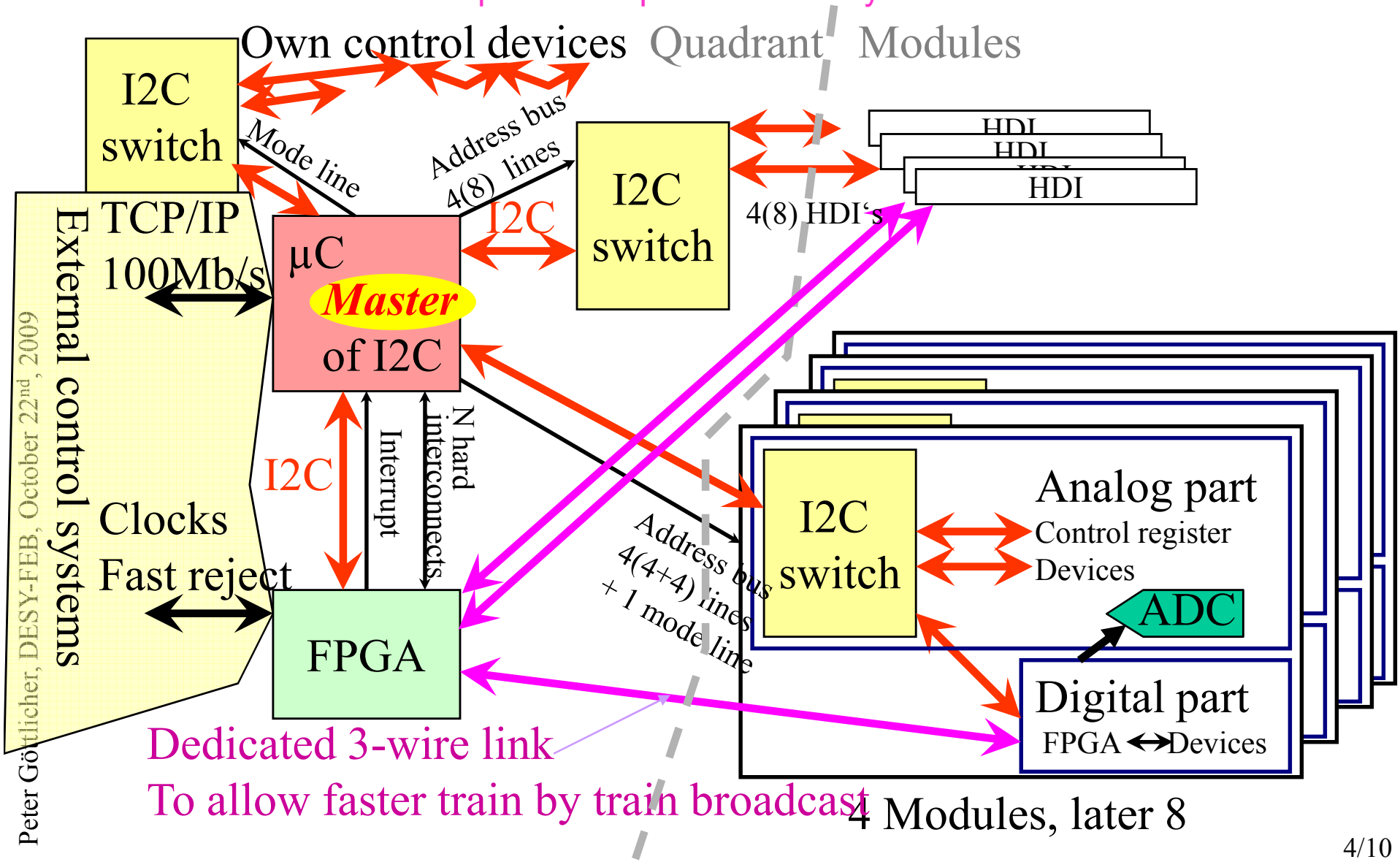
Frequency of Sys-clk If F_{in}=5Mhz	Multiple of Input clk	N_{fdw}	N_{rdw}	Possible division in detector head examples	Possible ADC-frequencies [MS/s] Examples with multiplier
90MHz	18	34	0	2,3	45,30 important, if>5MHz
100MHz	20	38	0	2,4, 5,10	50,25
105MHz	21	42	0	3	35
120Mhz	24	44	0	3,4	40, 30
135MHz	35	68	0	3	45 important if>5Mhz

With a little freedom: Flexibility for XFEL and for detector head
AGIPD: Decision, which sample frequency will be late

Control concept - internal

- Main based on commercial I2C standards with segments
- Some links on custom protocol: special bunch sync.



Micro controller: ARM9 with LINUX

Investigating on evaluation board:

Module: phycore-LPC3250

Details:

- PCM-040(60x58mm, 320pin)
- Chip: NXP LPC3250m ARM926EJ-S
- Core frequency: 208MHz
- RAM: 64MByte
- FLASH: 64MByte

Operating system:

embedded LINUX from NXP 2.6.27

People: WP76 Dana Wilson

AGIPD Lothar Steffen

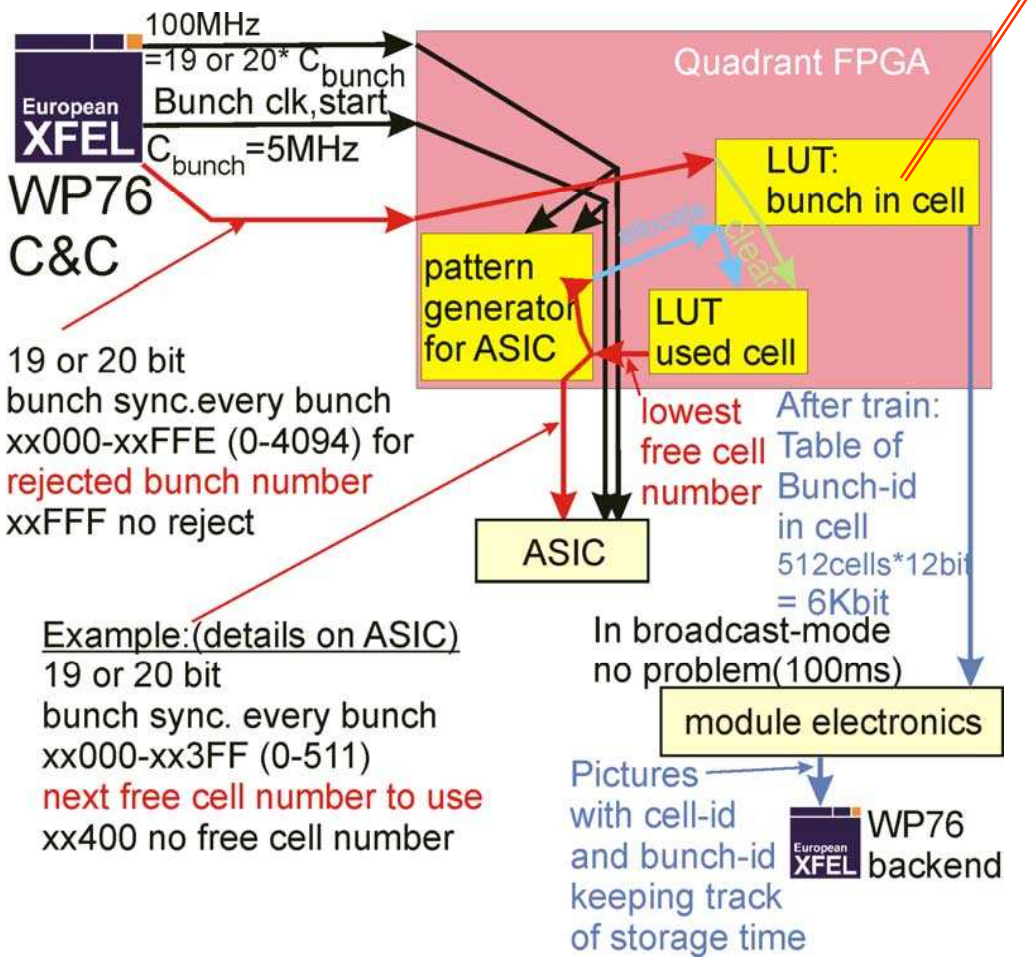
Micro controller: Tasks

- Monitoring: - Sensors, no need per train,
  < few 10 per readout-module and quadrant
  Currents, voltages, temperatures
  4 x I2C-bus with brunches
  - Bunch reject tables, status-bits: (debugging)
  Tables (~10kByte) to be loaded
  from FPGA per train: parallel bus (ADDR,DATA,CTRL)?
  Interrupt for train synchronized activity ?
- Booting: - downloading parameters (~MByte for ASIC?)
  (less for PCB's of detector head)
  - Firmware for FPGA's (to be investigated)
- Debugging: Via CPU of C&C? extra link?

Bunch reject

Readout of full table 10kB/train

To C&C? always/debug? To train builder?



Needs:

- registers, state machine in ASIC
- VDHL code in quadrant
- VHDL code in module
- anyway in proposal for book keeping to backend

Allowance:

Reject every bunch while the whole train

Addressed to next C&C

19 or 20 bits
"tolerances" on clock
soft: VHDL-coding

Communication to C&C – Summary and Questions

Control: 100MbE, TCP/IP

Flexibility/Debug?

Debug: Records to file? Separated hardware link ?

Train synchronous:

Now: Only reject tables, status bits

Clock: Flexibility in the frequency setup

Bit stream per bunch from C&C top detector head

Not at bit limit: sys-clk/bunch-clk

16 bit/bunch?