AGIPD for C&C

Peter Göttlicher, DESY

Reminder of detector head

Details:

- Slow monitoring

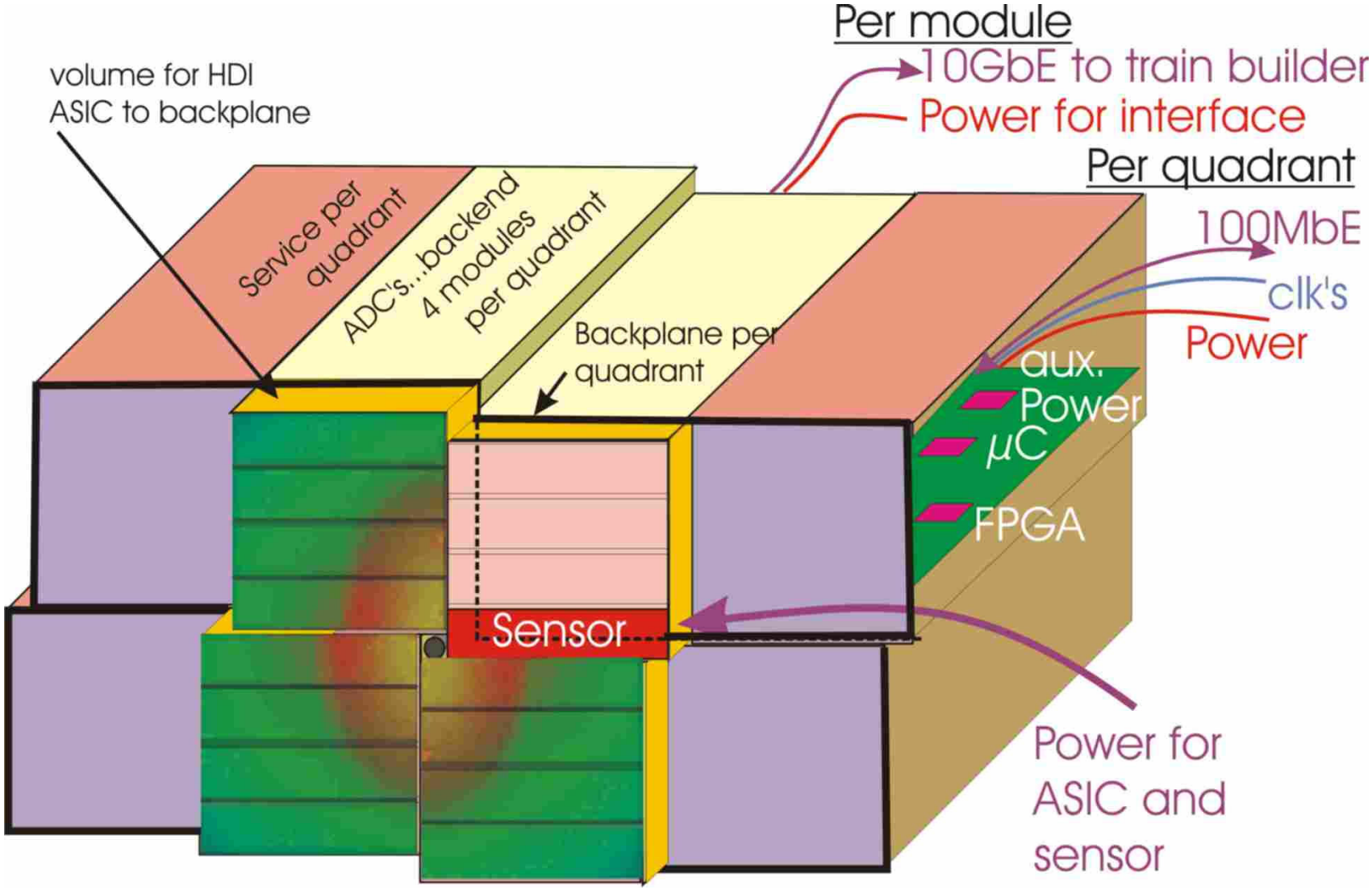
- Ideas for fast isolators

- Power

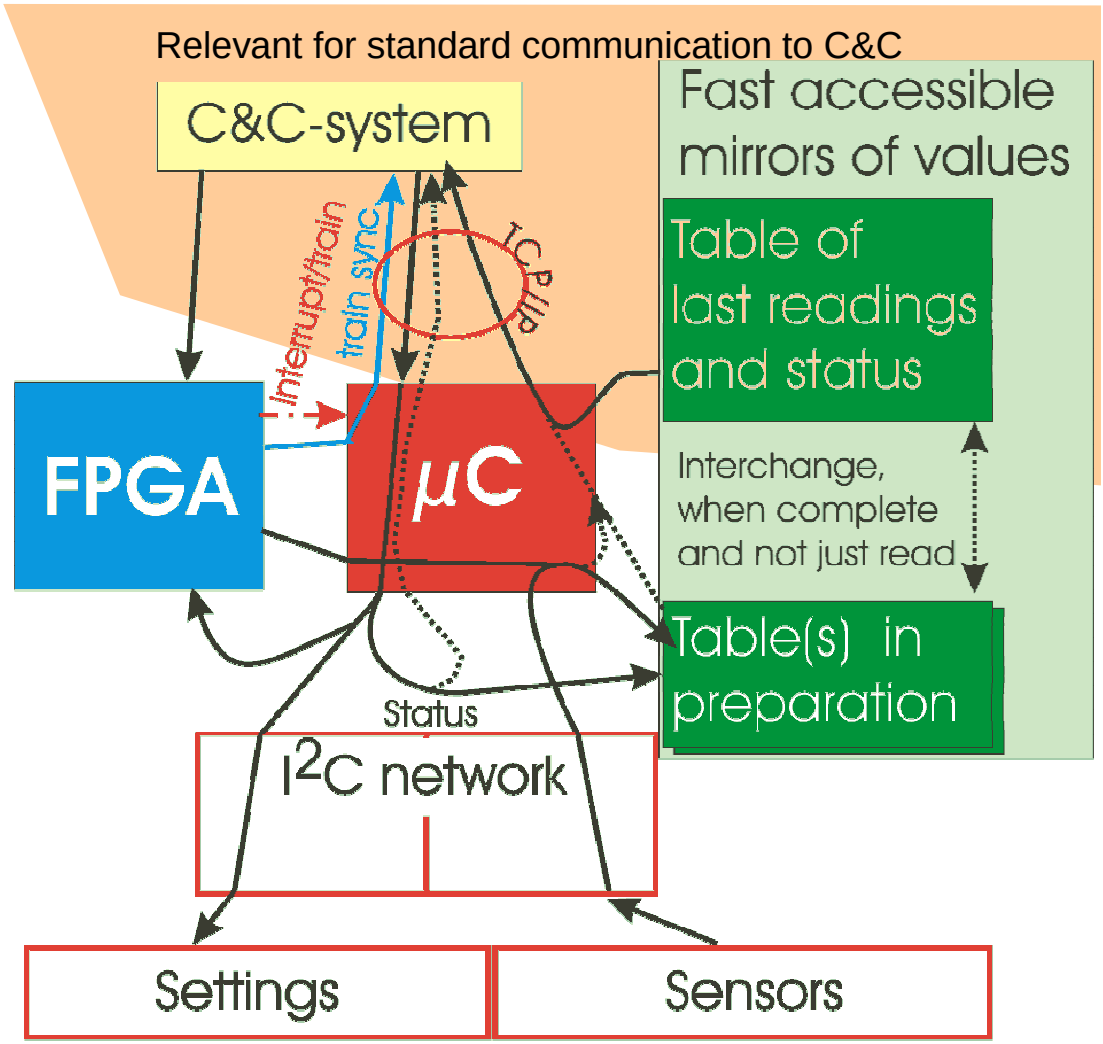
HELMHOLTZ ASSOCIATION

DESY

Reminder: Detector head



Slow Control



Read requests

Handled from internal RAM
- Time independent from internal structure
- Blocks and not individuals

Set commands:

- How to acknowledge
  As flag in read-table?
  or do you like more:
  As reply, when finished
- Setting in blocks and/or individuals

Only for debug:

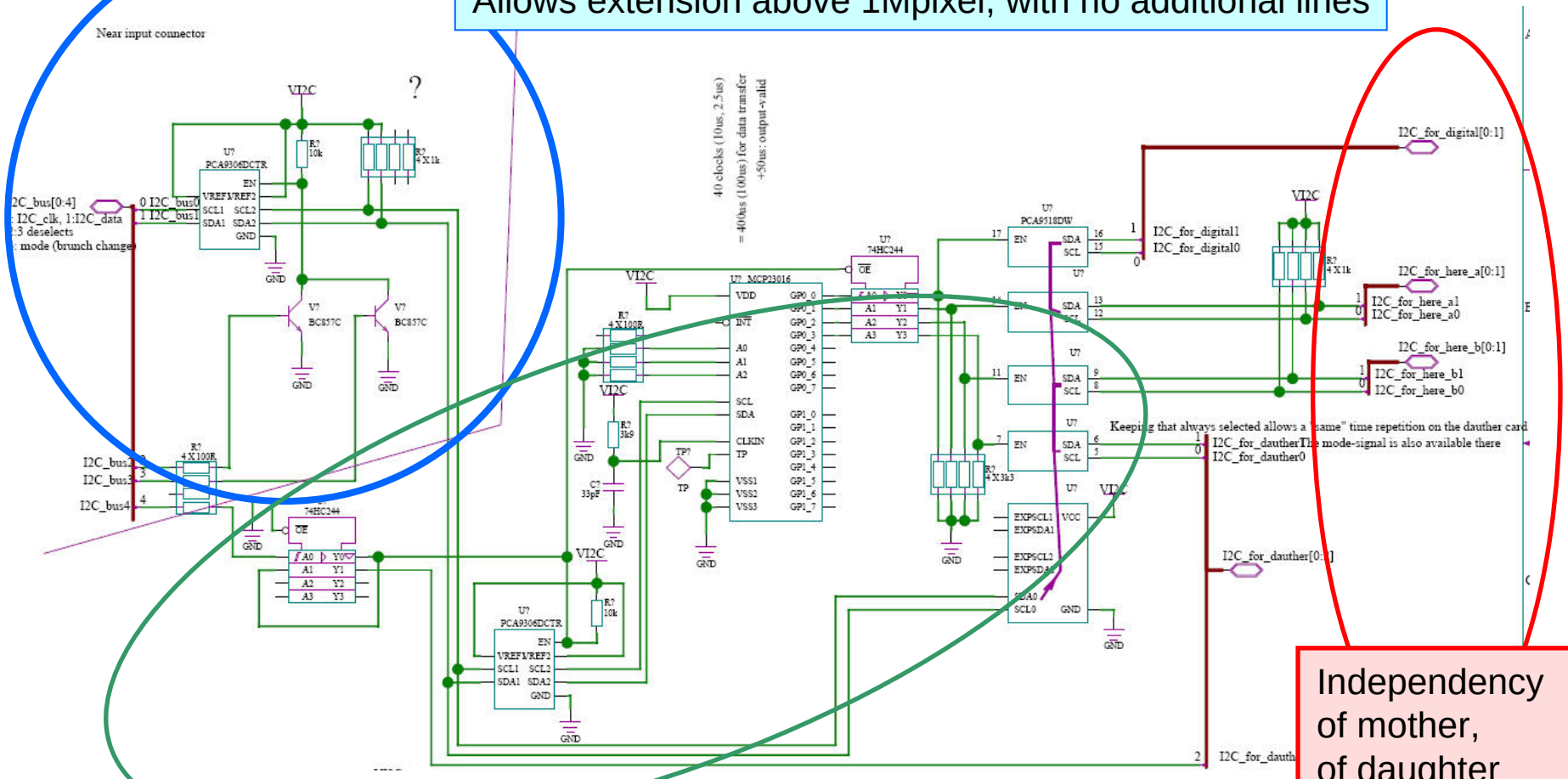
- direct access to sensor
- access to internal tables

FPGA:

- Slow control, like sensor
- Fast: bunch/train sync.

I2C network

Module selector with 2 bits:
Allows extension above 1Mpixel, with no additional lines



Independency
of mother,
of daughter
and digital part

Mode bit allows to
Set internal brunches for
more internal chips, different logic levels/speeds
different od duplication of hardware

Price:

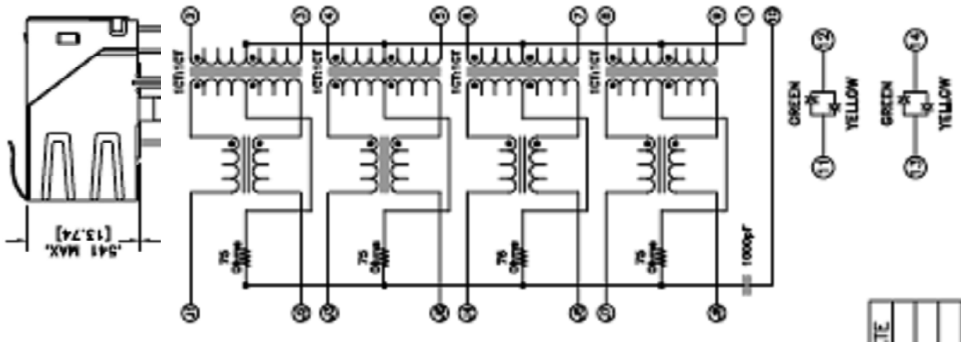
Time for addressing !

Ideas for fast isolators

LAN: 10/100/1000Mb

Isolator inside RJ45

e.g. WUERTH ELEKTRONIK, 7499111441

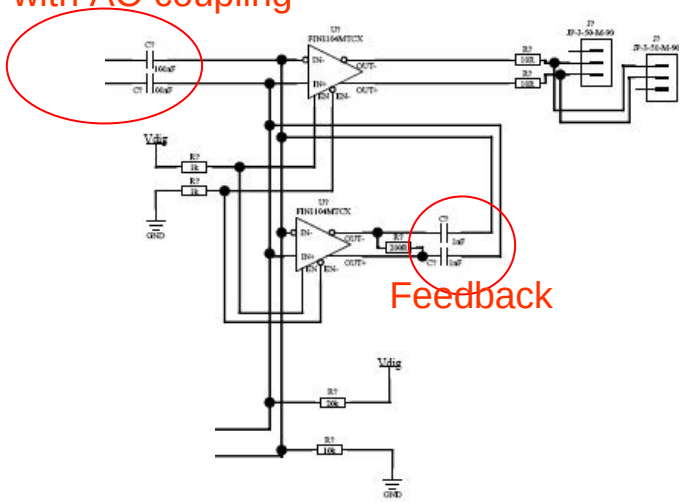


Isolation + current balancing

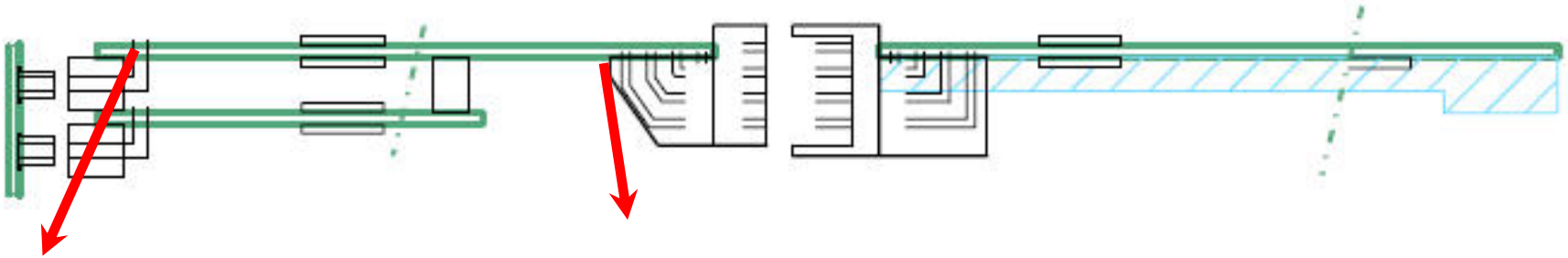
FAST-CLK's

- Example from NIM_to_LVDS, mono-flop
  proven to be OK.
- For here: feedback with resistors
  rate independent, but need first edge
- Better to put bottom receiver behind top,
  but no problem seen
  First to output the result, second to drive feedback

INPUT with AC-coupling



Module electronics: analogue part: Power



- Receiver/filter/ADC-driver needs pos. and neg. voltage

Power budget:	U	I	
ADC:	1.8V	2*32* 50mA = 3.2A	possible to cycle with train
Receiver…	2.5V	2*32*10mA = 0.7A	possible to cycle with train
	-2V	…. 0.7A	

- *Common mode for termination of ASIC: 2.5V into 50Ω, difference voltage to drive: 1V?*
  *2.5V 2*32*20mA = 1.3A cycling?, feedback to ASIC?*
  Is 470Ω to 0.9V not OK + differential 100Ω.

I2C-SC	2.7V	low	permanent
ADC-clk	2.5V	<300mA	possible to cycle with train
LVDS buffer	3.3V	2*32*11mA= 0.7A	digital quality,from dig. Part

- Two supplies: greater ~ +3V, and ~ -3V(?) + 1 for digital part (~12V) + quadrant + ASIC's

Total power w/o cycling analog part: ~ 20W/module, to be added some spare

Use voltage differences for buffering and cycling the power with avoidance on noise and feedback to power supply.

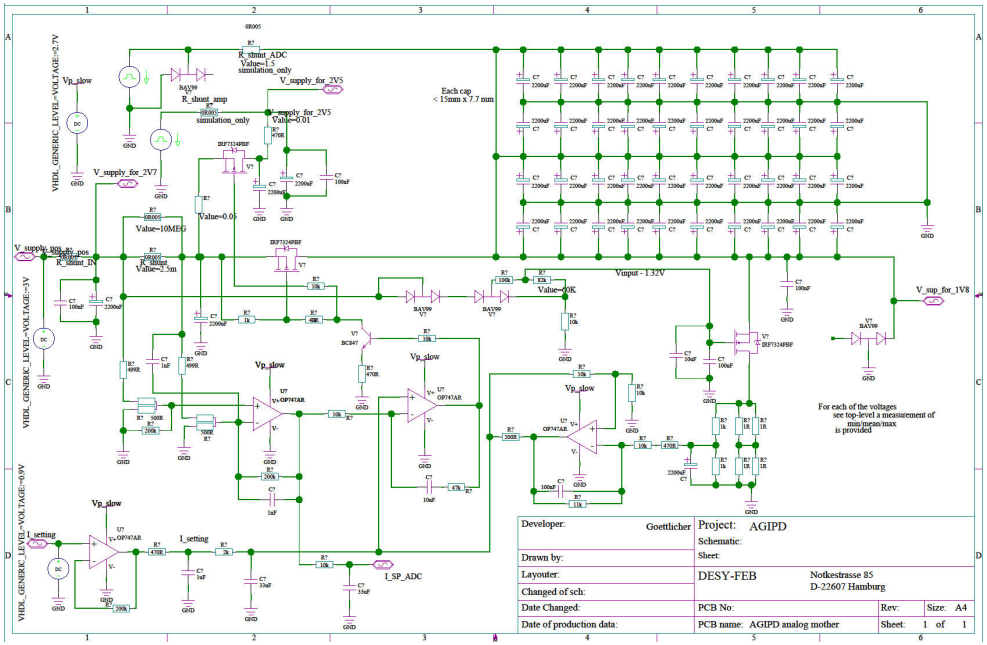
Module electronics: analogue part: Power

Trial to use duty-cycle

- Algorithm:

Power supply stabilize U
Consumer stabilize I

- Needs
  - Capacitor banks
    (Top + bottom)*(mother+daughter)
    ~ 40mm
  - I-regulator for charger
    + avoidance of U-saturation

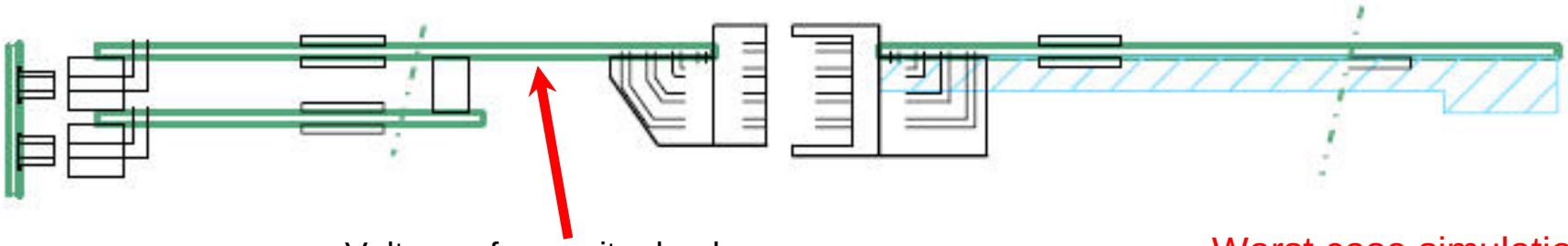


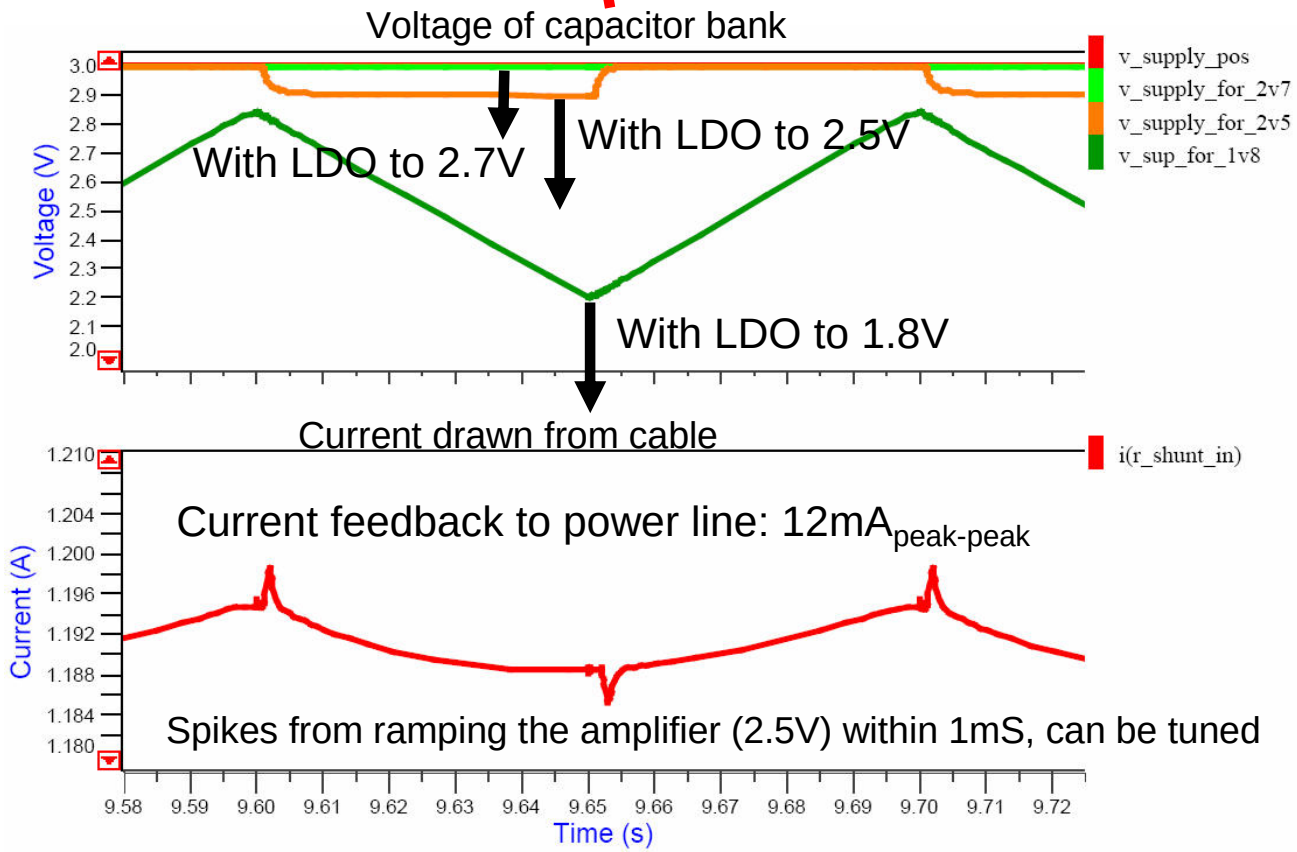
Following LDO-regulators not in drawing

- Nice and planned: Monitor for minimum/mean/maximum
- Symmetric negative part missing at the moment

Module electronics: analogue part: Power

Simulation !!!!





Worst case simulation

With 50% duty-cycle

400 picture*32*32 pixel

* (sample+gain)

*20ns/100ms= 16%

Settable operation point

via

quadrant-µC ⇒ I2C ⇒ DAC

Final remarks

- Idea for disentangled fast response to TPC/IP answers
- First view for galvanic isolation of control cables.
- Simulation of power for interface/analogue part

    Concept for low EMI-feedback,

        2 voltages for analog part

        1 digital part

        ASIC's?, quadrant not worked out

    Take it as rough idea!