

# Versatile AMC for XFEL Machine Control

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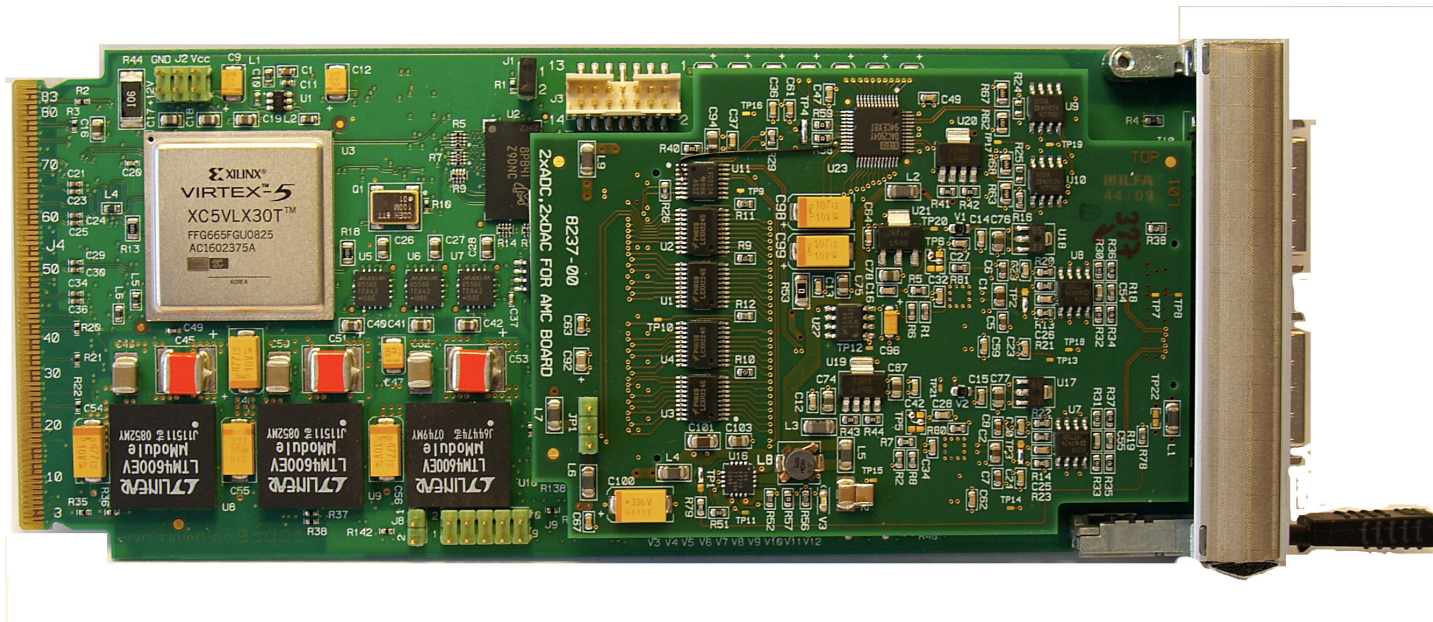
- Introduction
- Lessons learned from DESY AMC board DAMC1
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# Introduction

- Development is being done for the European X-Ray Free Electron Laser (XFEL) currently being built at Hamburg, Germany
- Central components of the XFEL accelerator control system are being developed according to the standards ATCA, AMC and  $\mu$ TCA.
- The DESY Advanced Mezzanine Cards (DAMC) are a compact and economical solution aiming at several applications for control and data acquisition systems at the XFEL accelerator.
- The DAMC1 board was developed as demonstrator to get experience with TCA related technologies
- The new DAMC2 board is based on the preliminary xTCA for Physics specification, which extends the functionality of the AMC standard and aims at applications in the field instrumentation



# First Generation of DESY AMC board



- Single size FPGA based board
- 256 MBit of DDR2 memory
- Custom made interface to an I/O Mezzanine Card (125 MHz ADC)
- 4 Lanes PCIe express to Backplane
- 1G Ethernet
- Intelligent Platform Management Interface (IPMI) with Hot Swap

Currently the DAMC1 boards are used in the control system of FLASH



# Lessons learned from DAMC1

Based on the experience at the FLASH accelerator

- $\mu$ TCA is suitable for applications in accelerator control systems
- All TCA related technologies are working successfully

But the DAMC1 has also some limitations

- Small form factor
- Non standard Mezzanine interface
- Printed edge connector (only few PCB manufactures)
- Limited external interfaces possibilities

New requirements and recommendations were collected from future users



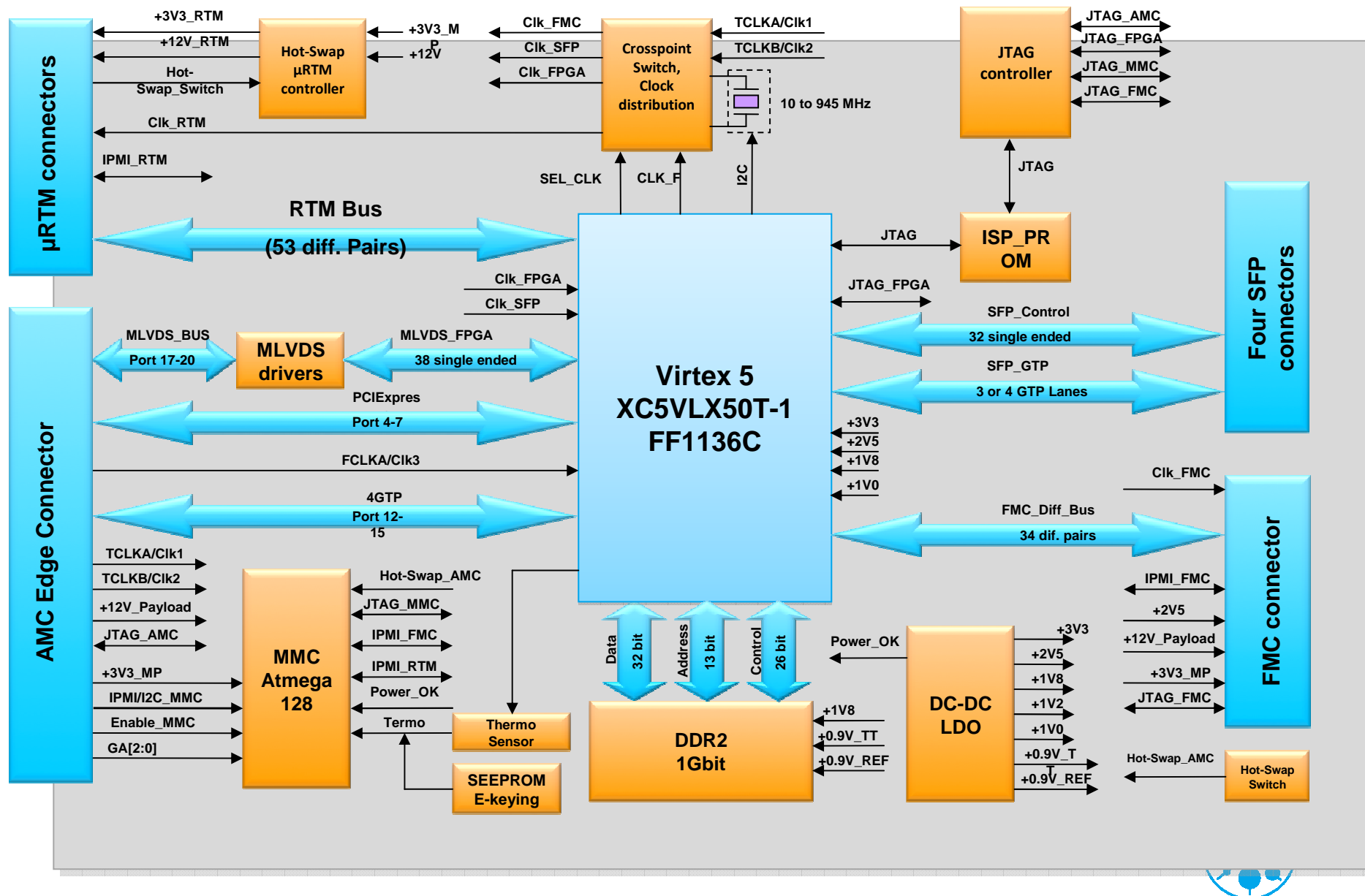
# DAMC2 Improvements

DAMC2 follows the preliminary xTCA for Physics Design specifications

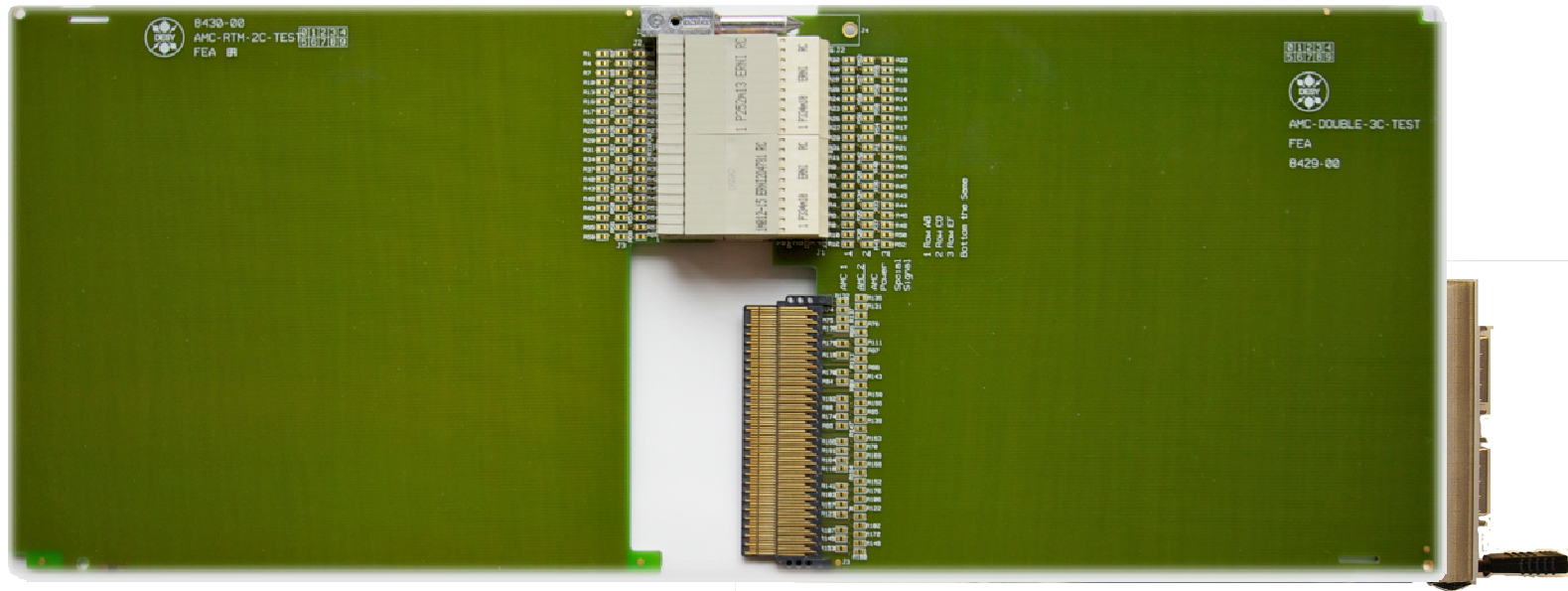
- Double size AMC-board extendable by a rear transition module ( $\mu$ RTM)
- VITA 57.1 compliant FPGA Mezzanine Card (FMC)
- Four optical links (SFP) at the front panel
- Extended DDR2 SDRAM Memory size of 1 Gbit (32 bit bus)
- Custom defined MLVDS interface to the backplane
- Flexible clock distribution scheme
- Sophisticated JTAG daisy chain



# Block diagram of DAMC2



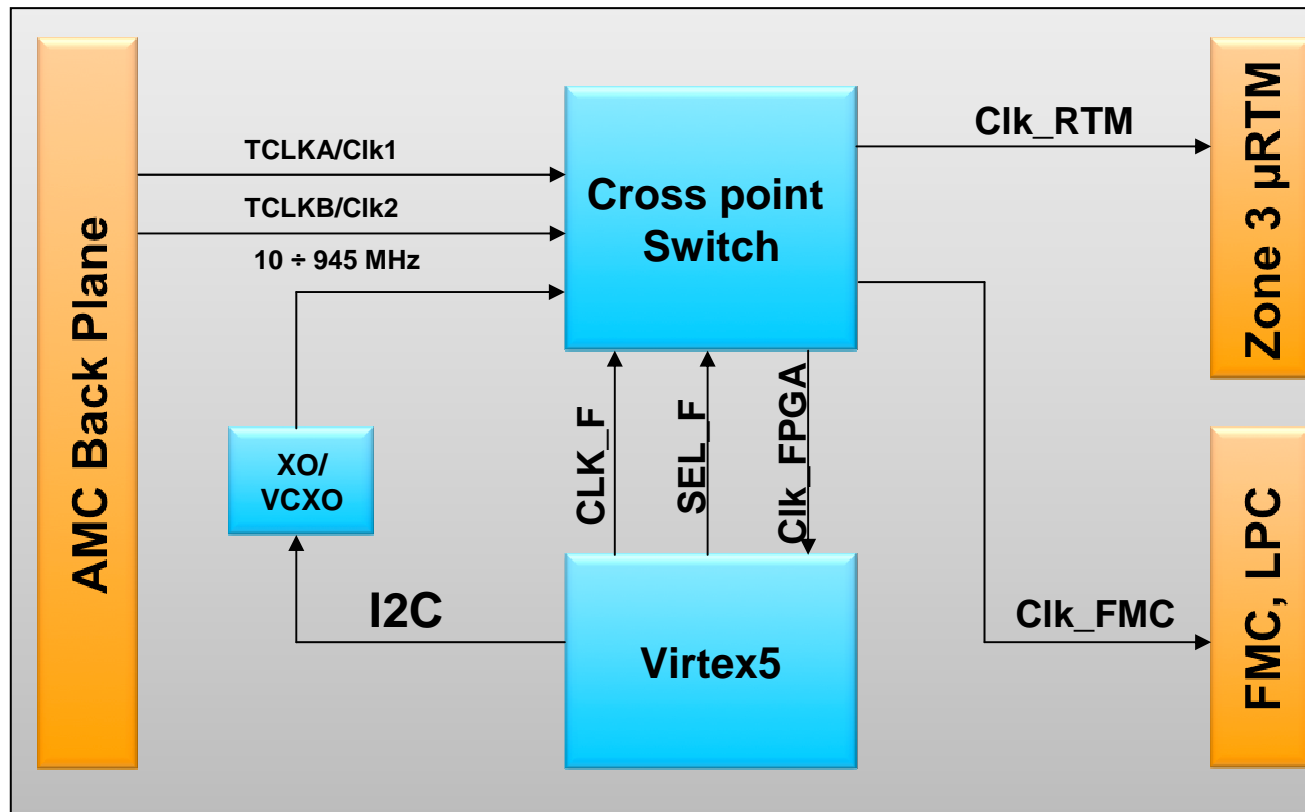
# Rear Transition module ( $\mu$ RTM)



- Doubles available space for development
- User defined 54 differential pairs (up to 1GBit/s)
- IPMI, Hot-Swap
- RTM Present Signal
- +12V and 3.3V Supply voltage



# Flexible Clock Distribution Scheme

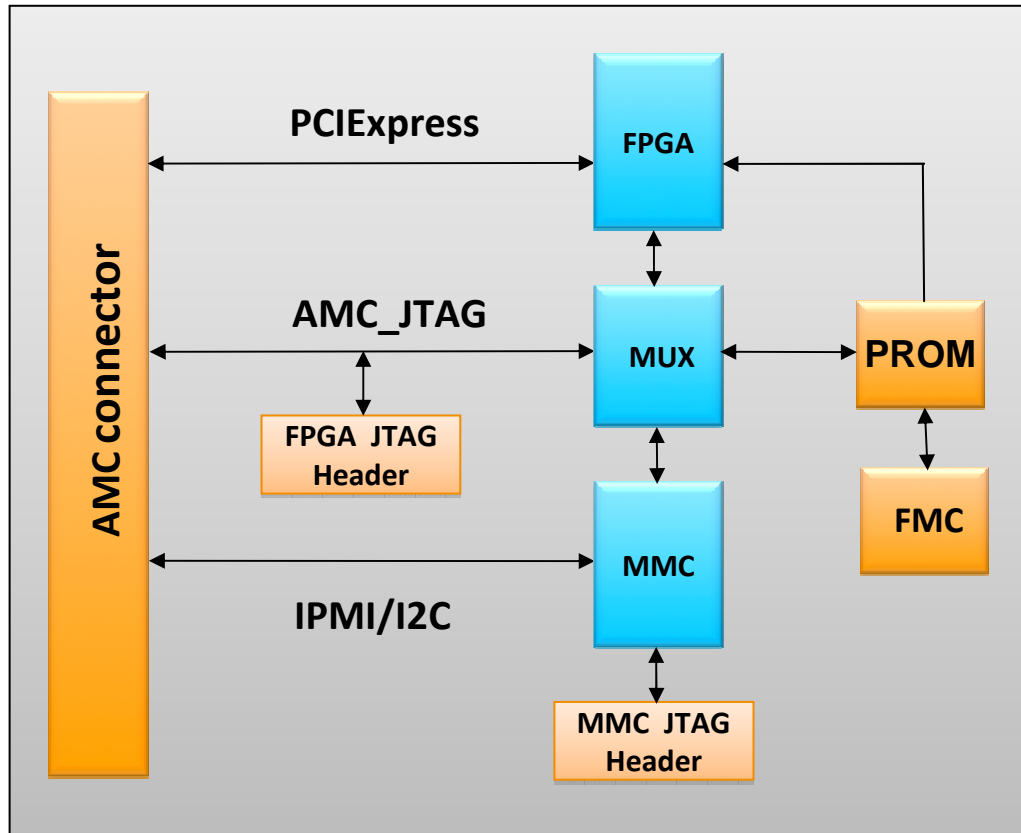


- 2 high quality clocks TCLKA / B from μTCA Backplane with low jitter
- High quality programmable oscillator (XO/VCXO)
- FPGA clock with wide frequency range for debugging purposes





# Flexible JTAG Daisy Chain

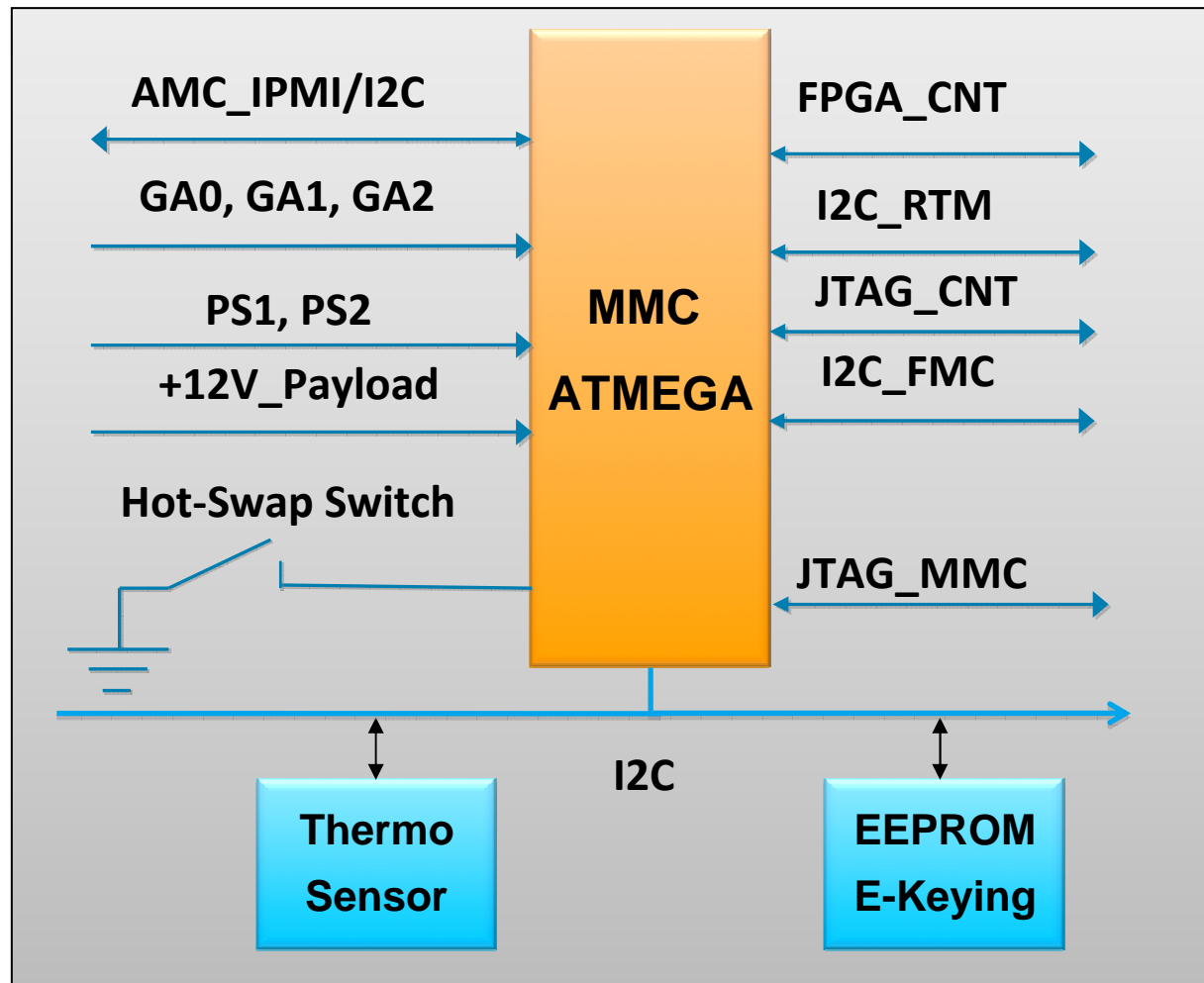


Several ways to configure PROM and FPGA

- Via the AMC JTAG Interface
- Via PCIeexpress and the JTAG ACE Player
- Via IPMI / I2C using the MMC as JTAG controller
- Via onboard pin header



# Module Management Controller - MMC



- IPMI for AMC-,  $\mu$ RTM- and FMC Boards
- Hot Swap for AMC - and  $\mu$ RTM Board
- Payload Power Control
- Management of the JTAG Daisy Chain for FPGA and PROM reconfiguration



# IO Resources of FPGA (XC5VLX50T-FF1136)

Task	Quantity of FPGA pins	Power Specs
DDR2 interface	120 (80)	1V8, 0V9
MMC interface	7	3V3
FMC interface (VITA 57.1)	72	12V, 3V3, 3V3_MP, 2.5 V
PCIExpress interface to Back Plane	4 GTP	1V2, 1V
User interface to uTCA Back Plane	4 GTP	1V2, 1V
SFP	28 + 4 GTP	3V3
uRTM interface	112	12V, 3V3_MP, 2.5 V
MLVDS interface to uTCA Back Plane	38	3V3
Clock, control, LEDs	23	3V3, 2V5
Total Number of pins	400 used of 480	



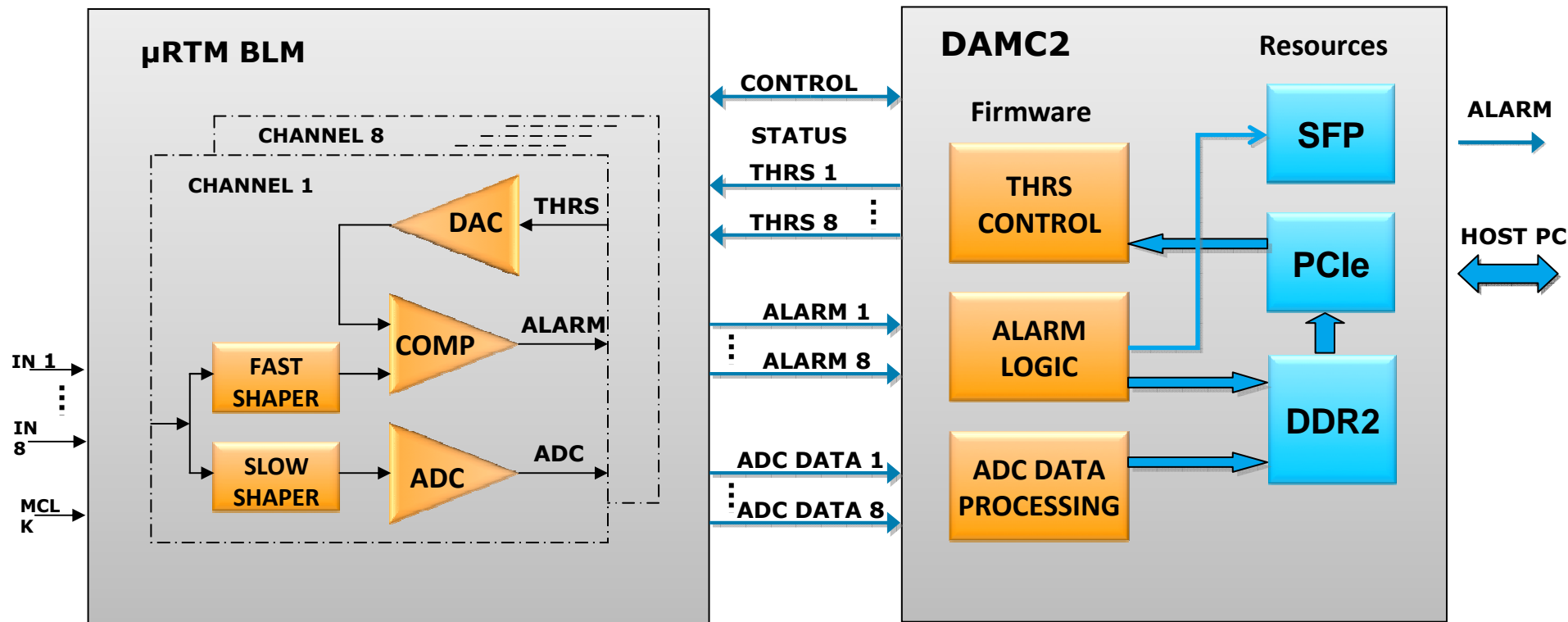
# XFEL Machine Applications for the DAMC2 Module

Application	RTM Type
Coupler Interlocks	ADCs,
Beam Position Monitor	ADC
Toroid	ADCs
Beam Loss Monitor	ADCs, etc.
Wire Scanner	Signal conditioning
Fs motors	Stepper card
Spectrometer	32ch ADC
MPS	Signal conditioning

- A wide range of requirements from several accelerator control subsystems - from fast DAQ to slow control system - are incorporated
- DAMC2 applications include a dedicated rear transition module ( $\mu$ RTM) as well as specific application firmware on the DAMC2 board.
- Typical tasks for the rear transition modules will be signal conditioning, data conversion and connector space for the input signals.



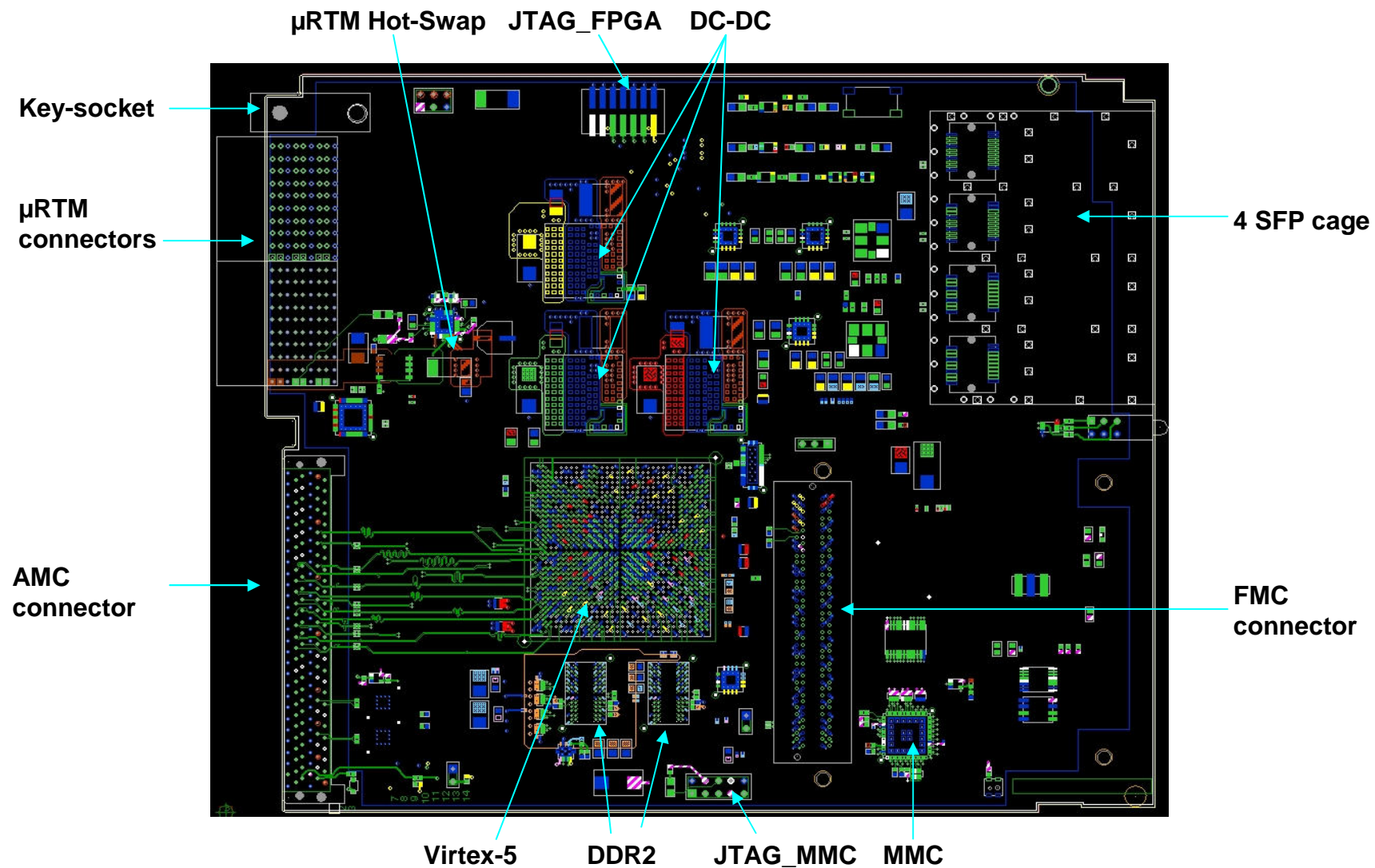
# Typical Application : Beam Loss Monitor System (BLM)



- Beam losses are detected by scintillators and PMs. If thresholds are exceeded alarm signal will be generated.
- 2 branches, one for fast alarm generation and one for more sophisticated analysis
- μRTM : 8 channels with pulse shaping and digitization at 50 MSamples/s.
- Analysis of digitized signals. Alarms will be distributed via SFP ports while control and monitoring is done via PCIe.



# Status of DAMC2 Layout



# Conclusion

- Schematic design is finished and board layout is in progress. A first prototype is expected this summer.
- Routing of more than 100 high-speed impedance controlled differential pairs from the FPGA to different interfaces is a challenging task.
- The xTCA for Physics specification, which extends the AMC standard by a rear transition module allows for cost effective, modular systems, where Input/Output as well as signal conditioning measures can be separated from the FPGA based front module.
- This approach is suitable for various control and data acquisition applications in different research fields

