Contents

Presentation about speed limit test between DAMC2 and uRTM (Qingqing)

- Please see the slides of the presentation for details
- Questions and comments:
  - The length of data and clock lines were optimized, to almost the same lengths, therefore no IODELAY was needed for lower frequencies
  - Higher datarates would be possible by using an external clock source (eg. not the internal PLL with 600MHz max. at Speed grade 1)
  - The data connection was DC coupled
  - Matthias ointed out, that a plot of the eye diagram of the data would be interesting

Presentation on uTCA Firmware upgrade infrastructure (Dariusz)

- Please see the slides of the presentation for details
- Questions and comments:
  - Olaf suggested to ask Gerhard to include the tools presented into a debian package
  - The tools to initiate hot-plug ups and downs require the correct PCI addresses, which could differe dependant on the used MCH and backplane; Dariusz would support us in preparing the tables for the crates we use
  - Lyudvig things, that there could be a direct way to read the correct PCI addresses without preparing a complete table -> needs to be checked/discussed
  - Petr Vetrov was asking, why the programming speed via SPI is still so low, as Xilinx presented numbers much faster -> Dariusz said, that the speed is limited by the FPGA internal programming clock speed
  - Only low resources are required to implement the additional programming blocks for JTAG Player or SPI programmer
  - Comment on Hot-Plug problem:
    - There is a time limit within the FPGA has to be programmed and PCIe is ready; otherwise the CPU is shutting down the PCIe channel
    - Some boards (especially with SPI FLASH) need too much time.
    - Therefore a rebbot on CPU side was required after reprogramming the FPGA.
    - The tools prepared by Dariusz could reinitiate a PCIe link via software
    - Therefore Hot-Plugging could be done even with those boards
  - A special page in the wiki will follow on that topic

Update on the FPGA course planning this November(Patrick)

- The course is now fixed and has the following details
  - Topics: PlanAhead, Timing Contraints and Partial Reconfiguration
  - Length: 4 days
  - Date: 14.11.2011 (Monday) - 17.11.2011 (Thursday)
- The registration procedure is the following:
  - The online registration form from IT has to be filled out and sent via the button (see links below)
  - After that, you have to print the upcoming page and let your superviser sign it

    - Send it to Maike Ermisch
- As written on the form, the final price depends on the number of participants, but my estimations were less than 1500Eur/person
- Please find the link to the registration form for the FPGA training course below:
    - In English: http://it.desy.de/e5/e49/e2024/e2259/anmeldung-training/index_eng.html
    - In German: http://it.desy.de/e5/e49/e2024/e2259/anmeldung-training/index_ger.html
- Further information could be found on the website of the company PLC2, who is giving the training: [[1]]
- As announced, the order of registration decides on priority of participation. We will check, if a second course might be an potion, if much more than the limit are interested.

Any other Business

- Update to newer Xilinx program suite
    - Frantisek asked about moving to newer version (eg. 13 series)
    - At latest, by the time of the training course in november we will move to the latest version available
    - At the mean time you have to deside, if you want already migrate