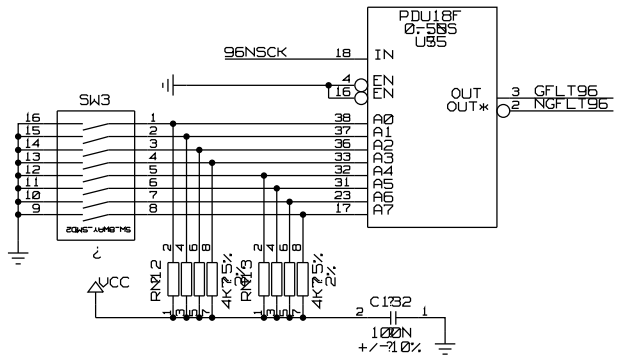
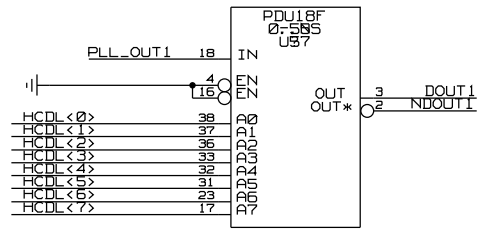
CLOCK DELAY LINES

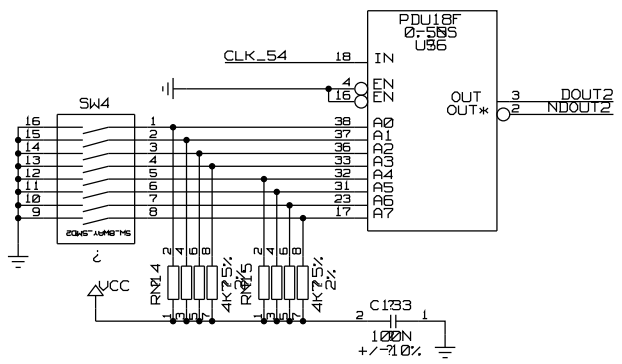
GFLT CLOCK PHASE DELAY LINE DL1



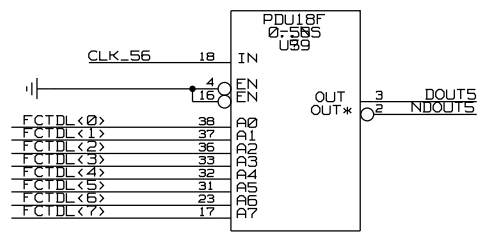
HELIX CLOCK PHASE DELAY LINE DL3



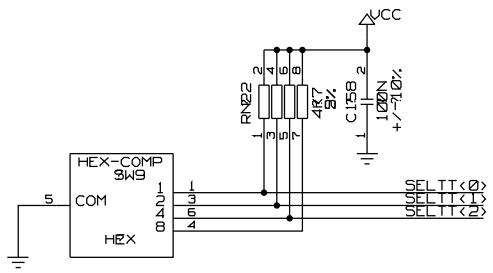
ADC - HELIX CLOCK FINE DELAY LINE DL2



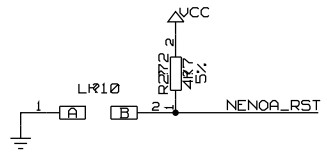
CALIB AND TEST PULSE CLOCK FINE DELAY LINE DL4



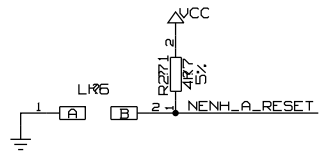
SELECT TEST TRIGGER 0-7



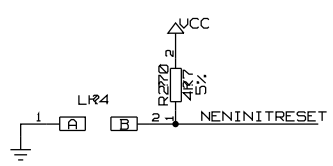
LINK 11 : INSERT LINK TO ENABLE "O/A RESET" TO "NOT_RESET"



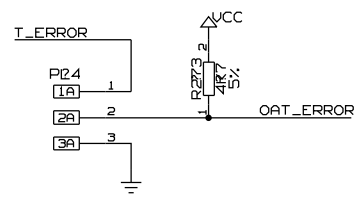
LINK 12 : INSERT LINK TO ENABLE "NOT RESET" TO "A_RESET"

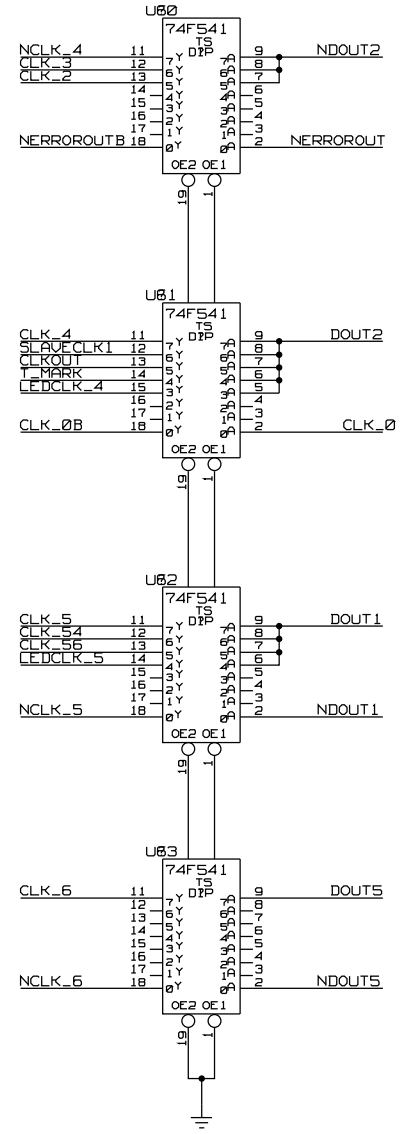


LINK 13 : INSERT LINK TO ENABLE "INIT_RESET" TO "NOT_RESET"



LINK 14 : SELECT ACTIVE OR GROUNDED "TERR" TO GFLT





DECOUPLING

ALL CHIPS IN DECOUPLED SOCKETS TO VCC

ISSUE	DATE	MOD NO.	DRN BY.	CHKD.	APPD.	STATUS
A	06-06-1999	- - - -	D. J. BECKETT	M. POSTRANECKY	M. POSTRANECKY	

USED ON ZEUS MVD

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CCLRC COUNCIL FOR THE CENTRAL LABORATORY OF THE RESEARCH COUNCILS — RUTHERFORD APPLETON LABORATORY, CHILTON, OXON OX11 0QX.

TITLE

PC3151M CIRCUIT

C+C MASTER

A | 2-TE-0103-001-08-A

TOTAL NO. OF SHEETS 11

A 2-TE-0103-001-08-A