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ABSTRACT

Today's high speed systems are encountering problems with clocking that were not considerations with lower speed clocks and systems. These problems are forcing the design community to rethink the task of clock distribution to avoid the consequences of the higher speeds. As a result, new products and new design techniques are being introduced which circumvent the complications of the older systems.

The consequences of poor clock design fall into two categories, skew and noise, each of which has its associated problems. Those related to skew include miss clocking (reverse clocking) of pipelined registers, duty cycle distortion, and erosion of the usable portion of the clock period. Noise related problems that can develop include signal reflections (termination problems), ground bounce, EMI, cross coupling of signals, and double clocking.

The solution to many clocking problems is to distribute the clock in a star pattern by taking a single clock signal and fanning it out with a low skew clock driver or buffer. This way each clock input or lumped load has its own individual clock line that is matched to every other clock line from the same source. By using a low skew clock driver/buffer, the designer can carefully distribute his clock while minimizing skew and controlling signal quality.

CLOCK SKEW PROBLEMS

Clock skew is defined as the difference in phase between two clock signals. The skew can be observed in several forms, all of which may or may not be of concern to the clock circuit designer. The first form, which is usually of greatest concern, is the difference between rising edges of two or more clock lines and is commonly referred to as "Same Edge Skew". This can also refer to two or more falling edges if the falling edge is used as the clocking edge. The second form of skew is the difference between the rising edge of one or more clocks and the falling edge of one or more clocks. This skew is commonly referred to as "Opposite Edge Skew". Clock skew can also be defined between packages, between banks switching and between other combinations as the devices and situations dictate. Some of the symbols for common skew specifications are shown in Table 1.

tsk(o)	Skew between two outputs of the same bank, package and transition
tsk(p)	Skew between opposite transitions of the same output
tsk(t)	Skew between two outputs of different packages at the same supply voltage and temperature

Table 1. Some Common Data Sheet Skew Specification Symbols

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PIPELINED REGISTERS

A common practice in logic design is to place registers in series so that upon the triggering of the clocks, the data will pass from register to register, passing only one register per clock cycle. If the Same Edge Skew becomes excessive to the point that the propagation delay through a register is shorter than the total skew of the clock, it is possible for data to be clocked into one register, pass through and be clocked into the second register during the same clock cycle. This would then create a system data error. A representation of this possibility is shown in Figure 1 where Data In could possibly appear at Data Out when Clock In toggles only once. Obviously the desired situation is to require two Clock In pulses to completely pass the data to Data Out. Tightening the Same Edge Skew of the clock signals, Clock 1 and Clock 2, will solve the problem of mis-clocking or reverse clocking of the registers and correctly clock the data through the registers, keeping the data in proper sequence.

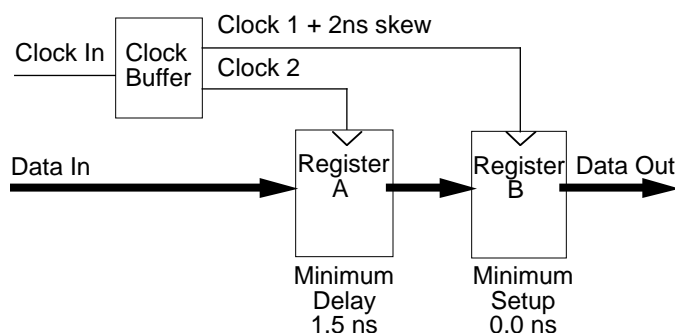


Figure 1. Clocking of Pipelined Registers with the Timing Parameters Shown it is Possible for Data In to Appear at Data Out with Clock In Toggling Only Once

Duty Cycle Distortion

An effect of Opposite Edge Skew is the distortion of the duty cycle of the clock as shown in Figure 2. If one edge of the clock occurs faster or slower than the other, the duty cycle will shift from an optimum point to something that may not function in the circuit. As an example, Figure 2 shows a 100MHz clock having a clock period of 10ns which can be divided into a 5ns high and 5ns low signal for 50% duty cycle. If this signal is used to drive a high speed register clock input, most high speed registers require at least a 4ns pulse width to properly clock. If the clock driver distorts the clock period by more than 10%, it is possible that the minimum pulse width of a 4ns register would be violated.

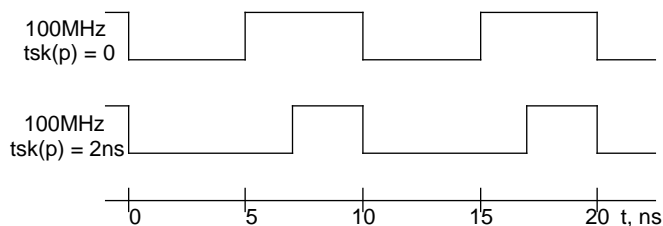


Figure 2. An Example Of Duty Cycle Distortion Due To Opposite Edge Skew. The Symmetry is Lost And Minimum Pulse Widths May Be Violated

If the clock is required to pass through several buffers in a large system, the duty cycle distortion can become significant unless steps are taken to insure that the Opposite Edge Skew of the clocking circuit is minimal and the duty cycle is preserved or corrected. If duty cycle distortion does occur, the use of a PLL clock driver such as IDT's FCT88915 can correct the distortion, as shown in Figure 3.

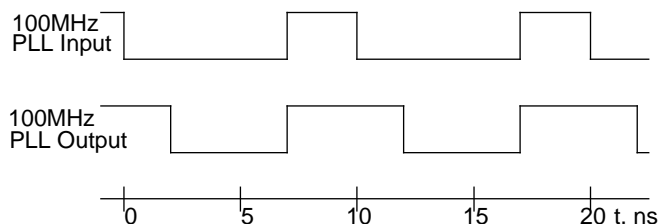


Figure 3. A PLL Clock Driver will Correct Duty Cycle Distortion

EROSION OF THE CLOCK PERIOD

Another anomaly that occurs because of clock skew is the erosion of the usable portion of the clock period. When performing a high speed design, a designer adds in all of the worst case propagation delays that are expected and then fits these into his clock period. With state of the art systems, the clock is usually run at the fastest speed possible to achieve the top performance levels and there is a minimum of time remaining in the clock period. If there is uncertainty in exactly when the clock will arrive, as shown in Figure 4, the designer must allocate some of his precious clock period to waiting for a clock which may arrive early or late. This has a direct influence on the performance of his system.

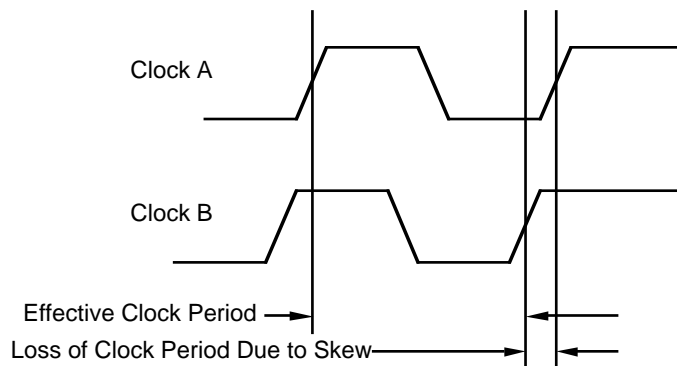


Figure 4. Erosion of the Clock Period. Any Clock Skew that Exits Decreases the Available Time During the Clock Cycle

By using clock drivers or other components with tight skew specifications (similar to IDT's Clock Drivers or Double Density Family) the uncertainty in the time of arrival of the clock will be narrowed, reducing the time allocated to clock uncertainty and preserving the clock cycle for other functions.

CLOCK SKEW CAUSES

Clock skew emanates from three sources. These three sources are the skew in the clock driver, the skew due to output loading of the clock driver, and the skew due to variations in the load/receiver. To arrive at a total skew figure for a circuit, the skew from these three sources must be added together. For effective skew management, the clock signal lines should closely match one another so that any signal distortion created by the clock line, load, or other source is seen equally by all clock lines causing all lines to receive the same distortion.

CLOCK SKEW DUE TO THE DRIVER

The skew in the clock driver is an effect of the manufacturing processes of the clock driver and is characteristic of the part as it comes from the manufacturer. Some of the causes of clock driver skew are the output pin location on the die, the variations in the inductance of the lead frame in the package and variations in the bond wires from the die to the package. Skew will come from any non uniformity in the device. The board designer should be aware of the sources of skew so that the optimum device is chosen when selecting a component.

Placement of the output pins on the die directly affects skew. The output pins should be in close proximity to and equally distributed around the ground pads on the die. Any outputs appearing at the corners of the die or on the opposite side as the ground pads will probably have a longer propagation delay and a resulting increase in skew.

Bond wires must be fairly well matched in length. If the bond wires vary in length, the longer wires will have a higher inductance and a longer delay.

The lead frame should be uniform. In some packages such as PGAs the pins have widely varying lead frame distances between pin and bond point. This has a direct effect on pin inductance which influences skew.

Some of the best packages for minimum skew are IDT's SSOP and TSSOP packages. These packages have multiple VCCs and Ground pins near the device outputs. The corner pins of the package are usually allocated to input only signals avoiding any package inductance problems. Other good packages include the SOIC and PQFP provided the pins are properly arranged. DIPs, PGAs and PLCCs are less desirable selections.

An additional form of skew in clock driver components is skew due to the technology used. Unless very tight tolerances can be maintained, skew will develop. IDT's 0.5u CMOS technology is one of the best available for tight tolerances. Older 0.8u and 0.6u technologies, particularly BiCMOS technologies, have proportionately looser control on skew.

UNEVEN LOADING

When using a high speed clock buffer or PLL, care must be taken to equally load the outputs of the device to insure that tight skew tolerances are maintained. Inherent in each output of the clock driver is an output impedance that is mostly resistive in nature (along with some inductance and capacitance). When each of these resistive outputs are equally loaded, the tight skew specification of the clock driver is preserved. If the loads become unbalanced, the RC time constants of the various outputs would be different, and the skew would be directly proportional to the variation in the loading.

Figures 5 and 6 show the effects of capacitive loading on a clock distribution circuit. Because of this effect, the loading on clock lines should be balanced. The difference between T1 and T2 in Figures 5 and 6 is skew, generated by loading, which can be very significant in unbalanced signal lines.

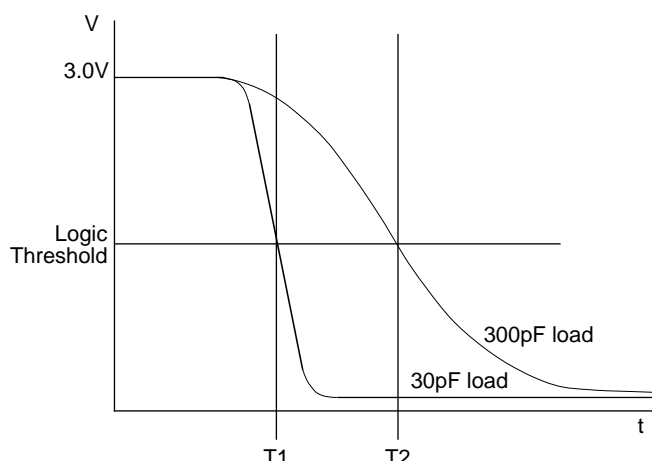


Figure 5. Effects of Capacitive Loading on a Clock Buffer (Falling Edge)

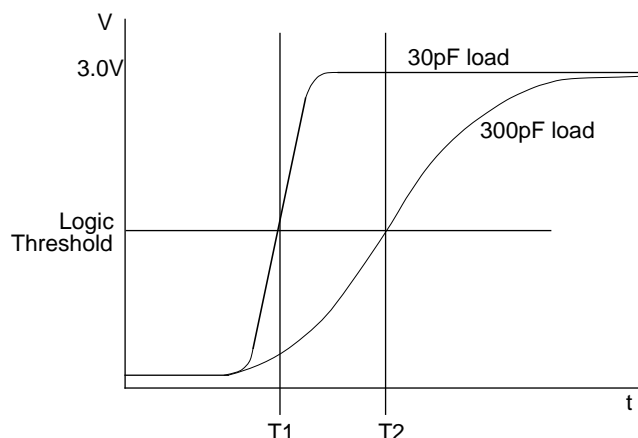


Figure 5. Effects of Capacitive Loading on a Clock Buffer (Rising Edge)

VARIATIONS IN SIGNAL LINES

Uneven loading on the clock driver or variations in the time of arrival of the clock pulse may be caused by varying trace lengths. In the case of a short trace, the load would appear as simply the capacitance (or other characteristic) of the load being driven. If the trace is long, the load at the far end of the trace will not be immediately “visible” to the clock driver during the logic transition due to transmission line delays. Because of this, the driver will see only the transmission line until the signal can travel down the transmission line, reflect off of the far end and return. The transmission line impedance of a board trace is typically in the 70 ohm region, while the short trace with a load will have a very high impedance (depending upon the load input impedance, trace capacitance etc.) The short and long traces will have very different effects on the clock driver; therefore, skew will develop between the two signal lines.

A secondary effect that occurs with varying trace lengths is the skew due to the propagation delay in the trace itself. This delay is approximately 1.5 to 1.7ns per foot of trace, but depends upon the trace characteristics. Again, the signal travels from the source to the far end of the trace, where it reflects and returns to the source. Variations in the trace length will affect the travel time and cause variations in the signal waveform.

INPUT THRESHOLD VARIATION

After the clock signals have been distributed with low skew, the clock receivers must accept the clock input with minimal variations. If the input threshold levels of the receivers are not uniform, the clock receivers will respond to the clock signals at different times creating clock skew. Most manufacturers (including IDT) center the input threshold level of their devices near 1.5 volts nominal for TTL input devices. This input threshold will vary slightly from manufacturer to manufacturer, especially as conditions (such as voltage and temperature) change. The TTL specification for the input threshold level is guaranteed to be a logic high when the input voltage is above 2.0 volts and a logic low when the input voltage level is below 0.8 volts. This leaves a 1.2 volt window over voltage and temperature. Components with CMOS rail swing inputs (such as the AC family) have a typical input threshold of $V_{CC}/2$ or about 2.5 volts which is much higher than the TTL level. If the threshold levels are not somewhat uniform, clock skew will develop between components because of these variations.

Figure 7 shows how two devices with different input thresholds will trigger at different times with a slow input edge rate. For example if the input thresholds for the two devices are 1.25 volts and 1.75 volts respectively, there will be a difference in the time at which the devices will trigger. For a clocked input, this represents a skew of 0.5ns between the two parts with different thresholds. As mentioned previously, 0.5ns can be a significant skew for high speed clocked systems.

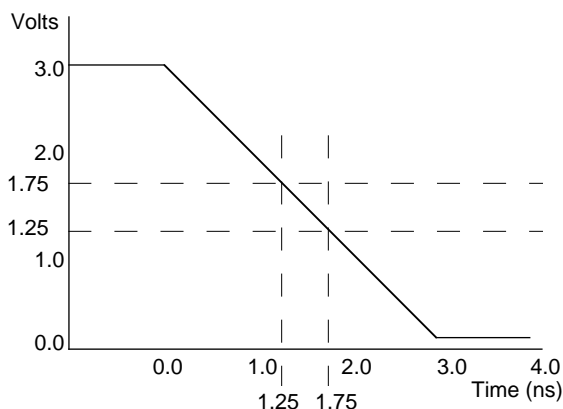


Figure 7. How a Change in Input Threshold from 1.25 volts to 1.75 volts will Cause a Corresponding Delay in Switching Time

To correct the problem, Figure 8 shows how a fast edge rate on the clocking device will minimize the skew due to variations in input thresholds. Comparing the two examples of Figures 7 and 8 for two devices with 1.75 volts and 1.25 volts logic thresholds, the skew is reduced from 500ps to less than 150ps because of the faster edge rate. To insure that the logic thresholds are as tight as possible it is important to use logic that is capable of maintaining tight thresholds over process variations, temperature, VCC levels and other circuit conditions.

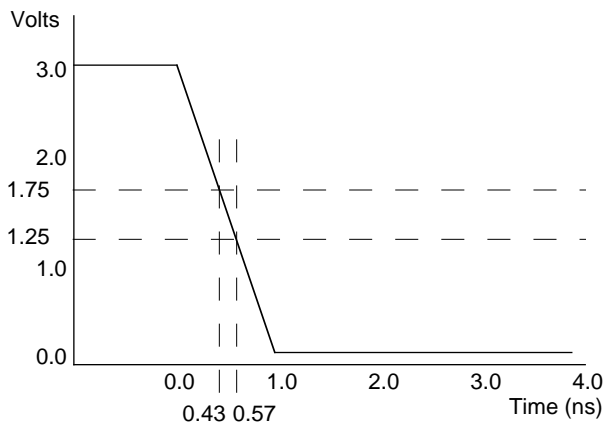


Figure 8. Increasing the Edge Rate Reduces Skew Due to Variations in Input Thresholds

CLOCK NOISE

In the design of high speed logic, the clock circuit is usually the worst offender for generating noise and also the most difficult to control. The noise problems in clock circuits emanate from several causes among which are the high frequency of the clock, the need for fast edge rates, and possibly the need to distribute the clock to remote locations on the board or in the system. Noise problems that can develop include double clocking, false clocking and waveform distortion. Double clocking as shown in Figure 9 can occur if a valid clock causes a glitch allowing the clock edge to transition through the logic threshold more than once,

possibly toggling the clock input with each transition. False clocking can occur if a signal reflects in the transmission line or if a noise pulse couples into the transmission line from an adjacent source, causing the clock input to transition through the logic threshold and toggle. Waveform distortion from noise can occur if noise is generated by, or couples into, the clock circuit, adding itself to the clock signal and interfering with the tight skew specification of the clock circuit, making the edge position indeterminate.

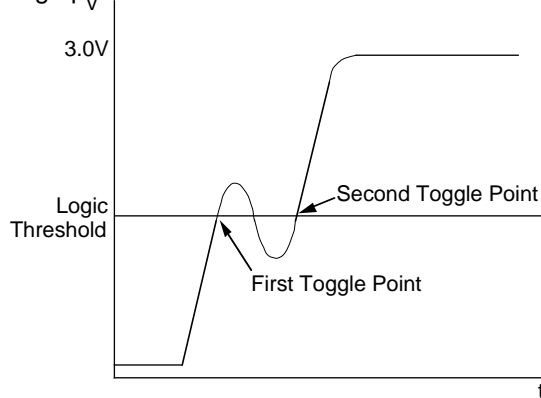


Figure 9. An Example of How a noise Spike can Cause Double Clocking

SOURCES OF CLOCK NOISE

Clock noise has many origins, some of which have already been mentioned. These sources interactively include mismatched line impedances, ground bounce, cross coupling of signals, fast edge rates and reflections.

As the speed of the clock circuit increases, the designer must utilize clock drivers with faster edge rates in order to maintain tight skew tolerances and clean edges. To achieve the faster edge rates, clock drivers typically have low output impedances which increase the current drive of the device. The low impedance causes mismatched line driving and the associated termination problems. A second effect of the fast edge rates is ground bounce internal to the clock driver due to the lead inductance of the device.

Line Termination

To avoid reflections, overshoot, undershoot and other transmission line associated problems, it may be necessary to utilize effective line termination. The decision to utilize line termination and what type to use should be based upon the circuit characteristics and allowable cost. In clock driver circuits, series termination should be avoided (unless used for tuning) because of its effects on skew and edge slowing of the clock signal. A better termination scheme is AC termination which uses a capacitively coupled series resistor to ground at the far end of the transmission line. An example of AC termination is shown in Figure 10, where a low impedance clock driver is driving a typical board trace. The AC termination consists of a 75 ohm impedance coupled with a 100pF capacitor. The resistor is selected to be slightly

larger than the trace impedance to allow for leakages such as the input impedance of the receiver, and to generate a full signal level transition on the received pulse. The capacitor is selected to allow the rapid transition of the clock edge to be properly terminated in the 75 ohm resistor, but then quickly cut the DC current drain. Higher capacitor values will allow heavier current levels to pass, increasing power dissipation, but giving cleaner signal waveforms, while lower capacitor values will reduce power dissipation, but also reduce the effectiveness of the termination. In selecting capacitor values, it should be kept in mind that the incremental effectiveness of capacitor values higher than 200pF is diminished while the power dissipation may continue to rise (depending upon the clock frequency). Capacitor values of less than 47pF will significantly cut the termination effectiveness of the resistor.

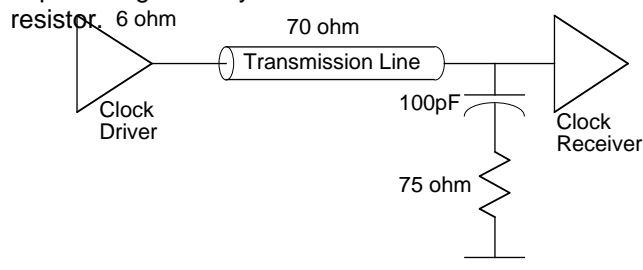


Figure 10. An AC Termination Example for a Standard Clock Line

Other termination schemes such as Thevenin, AC coupled Thevenin or series may be used with clock circuits with varying attributes and drawbacks. These are discussed in IDT's Logic Application Notes AN50 and CP10.

Ground Bounce

When selecting a clock driver component, it is important that the clock driver has a relatively low ground bounce. Most clock drivers are controlled to the point that the clock driver itself will not toggle due to internal ground bounce (where the die bounces high or low enough for an input to pass through a logic threshold). Despite this, many clock drivers experience an undershoot in their output waveforms, which may be partially caused by ground bounce. When a user sees an undershoot in the clock signal, the first suspicion should be improper line impedance matching and then ground bounce. To correct the problem, the designer should attempt better impedance matching or loading. If the problem is ground bounce, it may be necessary to select a different clocking device.

Ground Bounce causes two problems with clocking. The first is the false clocking of the input to the clock driver, itself, which may cause the clock driver to erratically toggle. The second (and more likely problem) is that the output waveform, with its severe undershoot, may cause false clocking in the devices the clock driver is driving, as shown in Figure 11. A

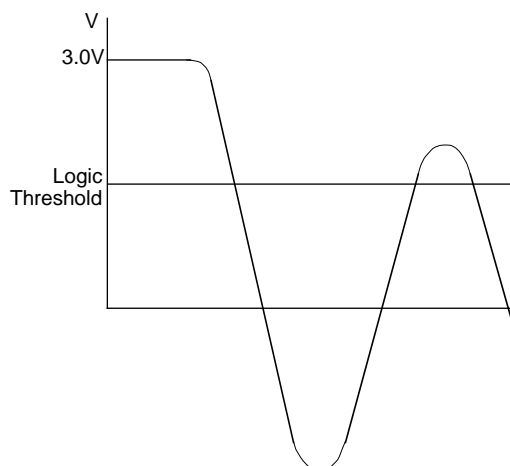


Figure 11. If the Effects of Ringing and Ground Bounce are Severe, False Clocking May Occur

severe undershoot on a clock input may cause the ground on the die of the receiving device to be pulled down, lowering the logic input threshold. When the undershoot rebounds, the input signal to the receiver may exceed the input threshold on the die and cause false clocking. If the rebound on the input signal is high enough to exceed the normal logic threshold, the receiver is likely to switch, regardless of any undershoot.

Because of the adverse effects, undershoot should be avoided on clock lines, particularly if it causes a strong rebound of the clock signal.

SELECTING A HIGH SPEED CLOCK DRIVER

The clock circuit is usually critical to the operation of the system. If the clock circuit fails, the system fails. Because of this, the proper selection of the clock driver/buffer is usually critical to the success or failure of the design. When selecting the clock driver/buffer there are several parameters and characteristics for which the designer can watch to insure the correct and reliable operation of his system.

Since clock drivers tend to operate at high frequencies, it is important to insure that the clock driver has low power dissipation. Unlike a buffer or latch that changes state only when one of the inputs changes, every output on the clock driver changes state every clock cycle at the fastest rate available in the system. This means that the clock driver is probably switching more power in a smaller package than any other component in the system. While heat sinks and other cooling methods will help, it is best to start with a clock buffer/driver that inherently dissipates low power.

Some of the lowest power parts available today are the 0.5u CMOS components. These components will tend to dissipate less dynamic power than any larger technology including the 0.8u BiCMOS processes. An additional advantage of the 0.5u CMOS process is that the static power dissipation is almost zero. There are no large current leakages that are inherent in the bipolar process. Older CMOS processes have a disadvantage over the new CMOS processes in dynamic switching current and, as a result, are

usually unavailable as clock drivers.

The output swing of the parts should be TTL level to avoid the swing all the way to the rail. This helps to tighten the skew specifications since the component has less distance to switch. The lower switching levels also reduce power dissipation by not forcing the load and device output to drive all the way to the VCC rail. TTL output levels are available on most component types including high speed CMOS components like several of IDT's FCT clock drivers.

Choosing between a clock buffer or PLL is usually dependent upon the need for zero delay in the driver or the need to increase the clock frequency. If zero delay or increased frequency is needed, a PLL is the obvious choice. An advantage of a PLL over a buffer is the ability to correct the duty cycle in the clock line if there is distortion. An example of a good clock buffer would be the 74FCT807T, which is a one to ten buffer with 250ps skew (tsk(0)). An example of a good PLL clock driver is the FCT88915, which contains 5Q outputs, Q/2, 2xQ and /Q. The PLL allows the clock driver to double the input frequency at the Q output if the Q/2 output is tied into the feedback. With this configuration, the 2xQ output will be four times the clock input.

When selecting the output drive capability of the clock driver, sufficient drive capability is needed to drive the load or transmission line with a fast edge, but not so high that severe undershoot and overshoot are created. The designer needs to examine his load and distribution technique to arrive at a drive level.

Most clock driver data sheets specify output edge rates, propagation delay, skew and other parameters with a 50pF, 500 ohm standard load. This "standard" has been carried forward from the days of bipolar logic and does not accurately reflect the conditions of newer clock circuits which typically have a very light capacitive load with no resistance. A typical clock line load has between 15pF and 30pF loading with no resistance. Some clock driver manufacturers are adding new loading conditions to their data sheets to allow the designer to more accurately determine how the components will respond in his circuit. Care must be taken when comparing

clock driver specifications to insure that identical conditions are being compared. Clock drivers are faster, dissipate less power, and are more uniform when driving the lighter load.

THE FUTURE OF CLOCK DRIVERS

Clock drivers/buffers have taken gigantic progressive leaps in the last year in speed, low power, low skew and small packaging. It is not difficult to find specifications of 100MHz with <250ps skew in a minuscule surface mount package. PLLs have become common and will probably be present in the majority of very high speed clock drivers in the near future. The 0.5u component technologies of today and smaller technologies of tomorrow will allow a continued narrowing of skew specifications. The new CMOS technologies have proven to be the leaders in clock drivers, overshadowing older CMOS and bipolar technologies.

As system speeds advance and demand newer and better clock management, the clock drivers will continue to keep pace with tight system requirements, leading the way to more product innovations.

CONCLUSIONS

As system clocking speeds increase, the issues of skew and noise begin to receive primary consideration. Future gains in system performance will be achieved by increasing the clock frequencies and requiring tighter tolerances in the clocking circuits. Low skew clock buffers and PLL clock drivers will assist the designer in meeting his system requirements for speed, skew, and noise; but, the clock circuit must be designed as a clocking system with consideration given to all aspects of the clock distribution network, including driver, receivers, transmission lines, and signal routing. If the designer is aware of the problems that can develop, the difficulties can be avoided.

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